Together ahead. RUAG

SAVOIR

space avionics open interface architecture

UART I/F and protocol publication

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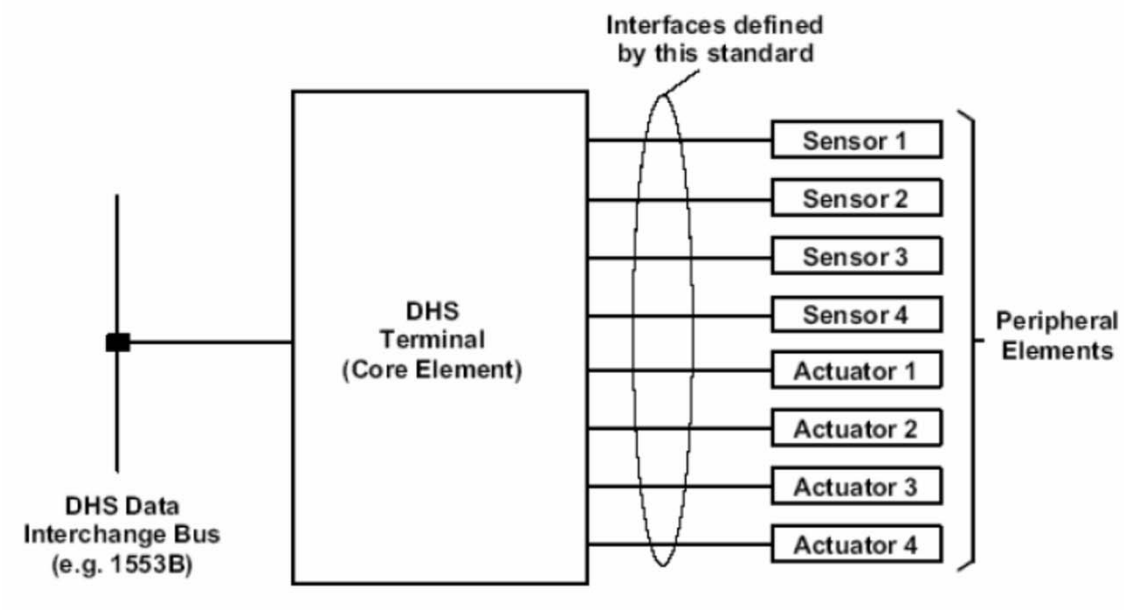
UART interface and protocol

- A proposal for a standard including an independent verification on a hardware test bench was prepared within an ESA study and completed in spring 2014.
- A user needs survey was performed and user requirements and draft physical and data link layer requirements were reviewed by the survey responders interested in following the work.
- First results presented at ADCSS 2013 as part of a generic presentation on recommendations for use of communication links within SAVOIR
- The intention was to later include the proposal as part of the ECSS-E-ST-50-14 Spacecraft Discrete Interfaces standard
- After many discussions it was finally decided to issue a dedicated SAVOIR document, SAVOIR TM-002, to guide future UART implementations

Guidelines for when to use a UART

- Used when data rates are below 100 kbps for a single device
- Used when the total quantity of platform sensors/actuators having a UART interface is less than about 20
  - UARTs are point-to-point links and require more hardware in the RTU and more harness for each device
  - Typical spacecraft usage today is less than 5 units.
- Used for devices where low power consumption and low mass is required
- Note: A UART link is controlled by the RTU in the SAVOIR architecture. The OBC is not required to have any UART links.
- Beware of: Total UART capacity depends on the C&C link used to the RTU. If 1553 is used the total UART traffic must be included in the overall 1553 traffic.

The UART in a system

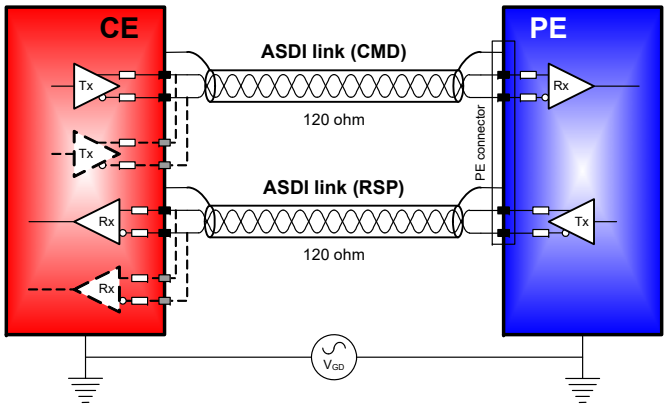


According to Figure 1 in ECSS-E-ST-50-14C

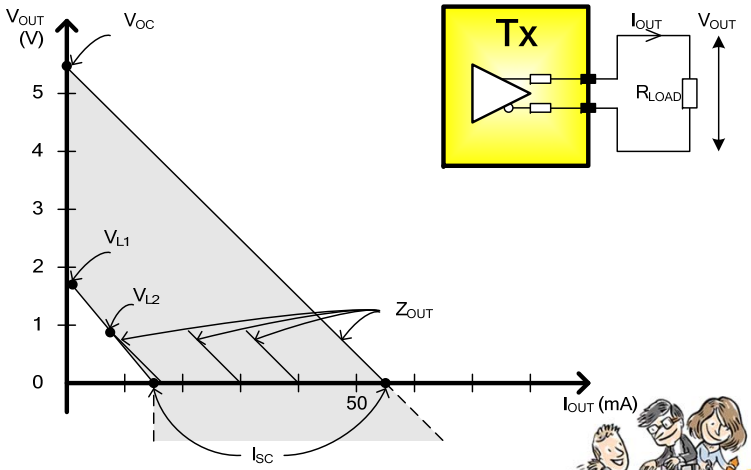
The names CE (Core Element) and PE (Peripheral Element) are used extensively in the specification.

UART physical layer

- Based on ECSS-E-ST-50-14C terms and clause 8.8 physical layer:
  - Relaxed impedance matching and ground displacement voltage requirements (±1 V)
  - Drive current characteristics more detailed
  - Up to 16 m cable
  - Recommend to use a 9-pin connector at PE side
  - Optional cross-strapping at CE side to simplify sensor/actuator design



CE = Core Element
PE = Peripheral Element
ASDI = Asynchronous Serial Digital Interface



Transmitter characteristics

TRANSMITTER Tx CIRCUIT				
Ref	**Characteristics**	**Value**	**AD**	**Note**
Tx1	Electrical characteristics	Differential	=AD1 =AD2	
Tx2	Differential output voltage open circuit, V_{OC}	$\|V_{OC}\| \leq 5,5$ V	<AD1 <AD2	Note 1 and 9
Tx3	Differential output voltage at 2kΩ load, V_{L1}	$\|V_{L1}\| \geq 1,70$ V	≠AD1 ≠AD2	Note 1, 2 and 10
Tx4	Differential output voltage at 120Ω load, V_{L2}	$\|V_{L2}\| \geq 0,90$ V	≠AD1 ≠AD2	Note 1 and 10
Tx5	Output current at output short circuit, I_{SC}	15 mA ≤ $\|I_{SC}\|$ ≤ 55 mA	≠AD1 <AD2	Note 1 and 10
Tx6	Differential output impedance, Z_{OUT}	$Z_{OUT} \geq 100$ Ω	>AD1 ≠AD2	Note 1, 3 and 10
Tx7	Common mode output voltage at 120Ω load, V_{OS}	$V_{OS} \leq 3$ V	≠AD1 <AD2	Note 10
Tx8	Output voltage TRUE and COMP lines, Ve	0 V ≤ Ve ≤ 5,5 V	<AD1 <AD2	Note 9
Tx9	Short circuit output current, I_A	$\|I_A\| \leq 150$ mA for each terminal to ground	=AD1 =AD2	
Tx10	Rise (and fall) time, t_R	$t_R \leq 0,1 \times t_B$ if $t_B \geq 200$ ns $t_R \leq 20$ ns if $t_B \leq 200$ ns CE: $1/t_B$ = max baud rate PE: $1/t_B$ = selected baud rate	=AD1 =AD2	Note 4
Tx11	Output leakage current in power off, I_O	$\|I_O\| \leq 100$ µA	=AD1 =AD2	Note 5
Tx12	Fault voltage emission, V_{SFE}	0 V ≤ V_{SFE} ≤ 7 V (through 50 Ω minimum series resistance)	=AD1 ≠AD2	
Tx13	Fault voltage tolerance, V_{SFT}	-1,5 V ≤ V_{SFT} ≤ 7 V (applied through 1 kΩ series resistance R_{IS})	=AD1 ≠AD2	

AD1 = ECSS-E-ST-50-14C
AD2 = ANSI/TIA/EIA-422-B

Receiver characteristics

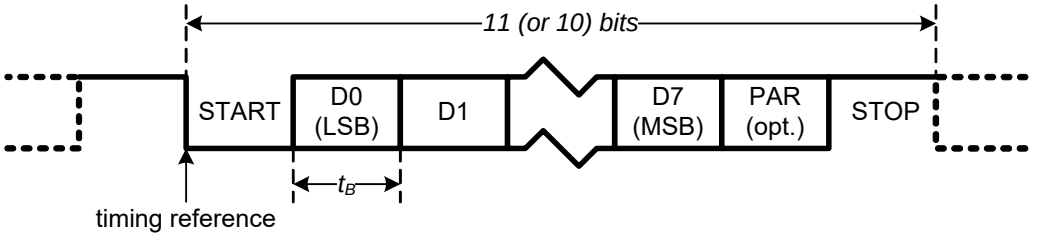
RECEIVER Rx CIRCUIT				
Rx1	Electrical characteristics	Differential	=AD1 =AD2	
Rx2	Discrete series protection, R_{IS}	2 * 1 kΩ	=AD1 ≠AD2	Note 6
Rx3	Max input voltage (each input w.r.t. ground), V_I	-1 V ≤ V_I ≤ +6,5 V	>AD1 >AD2	Note 11
Rx4	Common mode acceptance (V1+V2)/2, V_{CM}	-1 V ≤ V_{CM} ≤ +4 V	>AD1 >AD2	Note 11
Rx5	Differential input voltage, V_{DI}	600 mV ≤ |V_{DI}| ≤ 5,5 V each ± voltage in this range must be interpreted as valid signal	>AD1 ≠AD2	Note 7 and 9
Rx6	High voltage input load, I_{INHV}, at V_I = 6,5 V	0 mA ≤ I_{INHV} ≤ 1,625 mA	≠AD1 <AD2	Note 8 and 9
Rx7	Low voltage input load, I_{INLV}, at V_I = -1 V	-1,25 mA ≤ I_{INLV} ≤ 0 mA	≠AD1 >AD2	Note 8
Rx8	Unconnected input voltage, V_{INUL}	0 V ≤ V_{INUL} ≤ 4 V	≠AD1 >AD2	Note 8
Rx9	Fault voltage emission, V_{RFE}	0 V ≤ V_{RFE} ≤ 5,5 V (through 1 kΩ series resistance R_{IS})	=AD1 ≠AD2	
Rx10	Fault voltage tolerance, V_{RFT}	-1,5 V ≤ V_{RFT} ≤ 8,5 V	=AD1 ≠AD2	

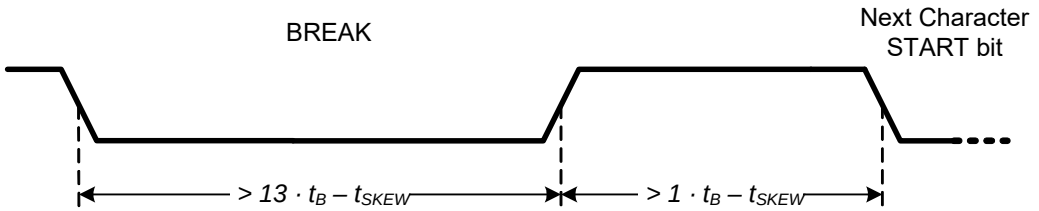
AD1 = ECSS-E-ST-50-14C
AD2 = ANSI/TIA/EIA-422-B

±1,5V ground potential difference allowed

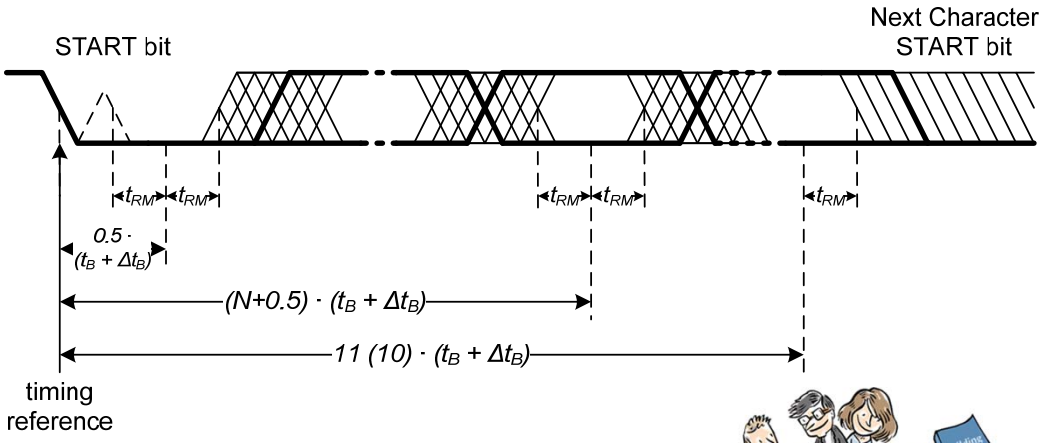
UART character layer
(part of data link layer)

- Characters and BREAK defined.
- Even parity recommended
- Baud rates of 19,2k, 115,2k and 460,8k recommended. 9,6k, 38,4k, 57,6k and 230,4k allowed



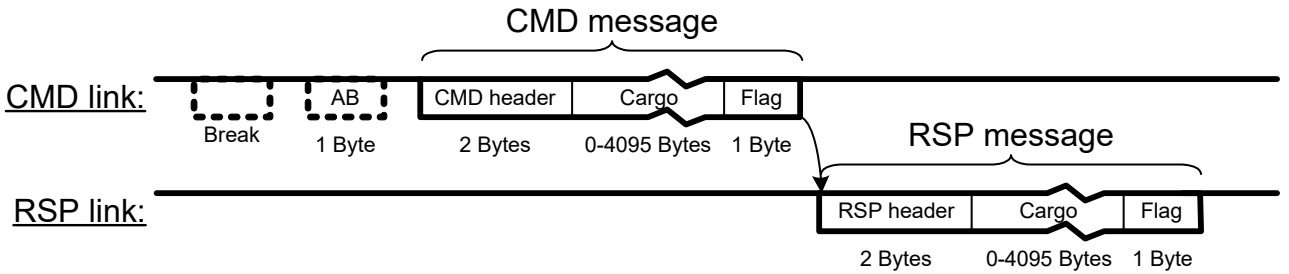


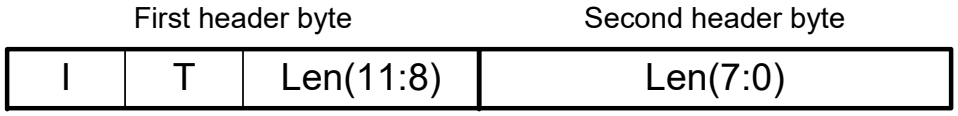
- Baud rate tolerances, start bit transients, skew, signal transition oscillations and receiver margins defined in detail. The figure shows the receiver character timing.



UART frame layer
(part of data link layer)

- Master/slave communication
- Delimited by header and end flag (FE_H)
- BREAK used as communication synchronisation





I = Instruction/information code

	CMD	RSP
00:	Command	Normal response
01:	Not used	Error response
10:	Reserved	Reserved
10:	Reserved	Reserved

T = Transaction ID, copied from CMD to RSP

UART frame layer - upper layer interface

- The CE Frame Layer interface to upper layer includes the following:
  - Cargo of CMD messages for transmission
  - Transaction ID for transmission
  - Cargo of RSP messages received
  - Received Transaction ID
  - Frame Layer RSP error events
  - Command communication synchronisation (BREAK)
  - Command Autobaud Sequence (including BREAK)
  - Command Autobaud Character only
- The PE Frame Layer interface to upper layer includes the following:
  - Cargo of CMD messages received
  - Cargo of RSP messages for transmission
  - Frame Layer CMD error events

UART frame layer options

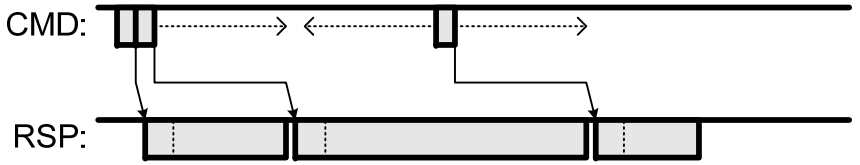
- Pipe-lining allows full bandwidth utilisation with relaxed timing constraints for instance when loading or dumping PE memory

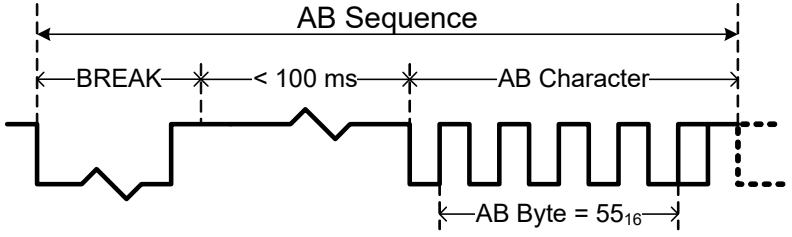
- Future protocol extensions using the reserved I-field values 10_B and 11_B are e.g.:
  - Addressing multiple PEs on a single RS-485 link
  - Adding data field headers

- Auto-baud function using BREAK + 55_H character allows for simple oscillators in the PE

Load memory:

Dump memory:





Contact

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