CORA RDHC

Compact Reconfigurable Avionics – Reconfigurable Data Handling Core

ESA contract 4000121650/17/NL/LF

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Main objective and consortium

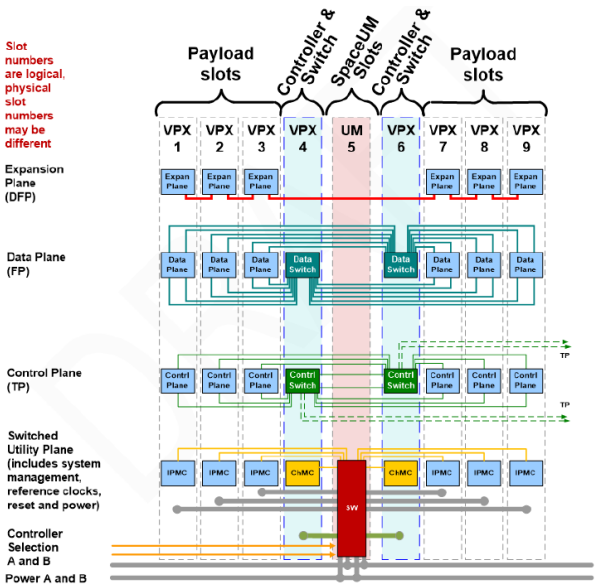
To design and manufacture a module hosting a high performance microprocessor and high capacity reconfigurable FPGA(s). The module shall be developed as an Elegant Bread Board (EBB) and will support standardised interfaces (Mil1553B, CAN[1)], SpaceWire) and lower level digital interfaces (sensor buses) used natively or as a bridge to Analog interface devices. This module acts as the execution platform for the "Compact Reconfigurable Avionics" cross sectorial activity.

1) CAN has been agreed to be excluded.

- Cobham Gaisler, Sweden, prime for the activity and responsible for the VHDL design and hardware deliverables.
- Thales Alenia Space France, responsible for middleware software design.
- Thales Alenia Space España S.A., Spain, responsible for FPGA reconfiguration code and HW/SW validation
- Airbus Defence & Space, France will contribute to the systems analysis and trade-off, requirements and system architecture.
- External service provider(s) used for circuit board development.

Main concept

- Provide a hardware platform that allows model based avionics SW development to be readily deployed on different avionics modules
- GPP based on GR740 – high-performance processor
- Utilise the BRAVE NG-Medium – reconfigurable FPGA – for AOCS sensor processing as well as other tasks.
- System hardware architecture – based on OpenVPX (VITA 65) backplane for module development.
- Develop modules to be forward compatible with Space VPX, VITA 78.
- Inter-module communication links – are based on SpaceWire RMAP.
- **Data plane** links will also be based on SpW-RMAP due to lack of high speed serial interfaces in the selected FPGA and GPP.
- RTEMS environment, boot loader and PUS terminal software.



Complete with SCOE and EGSE

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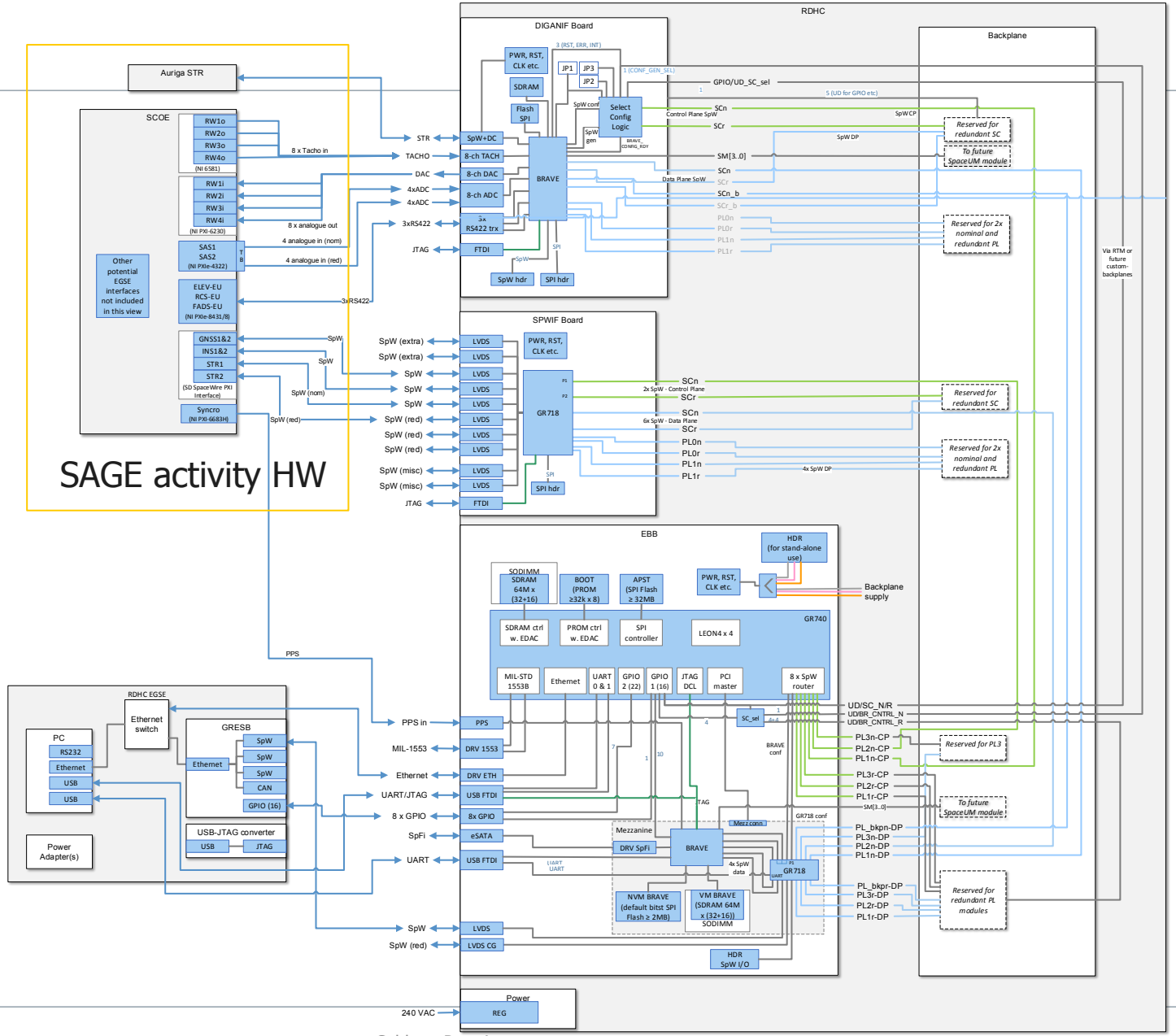
CoRA – Hardware Overview

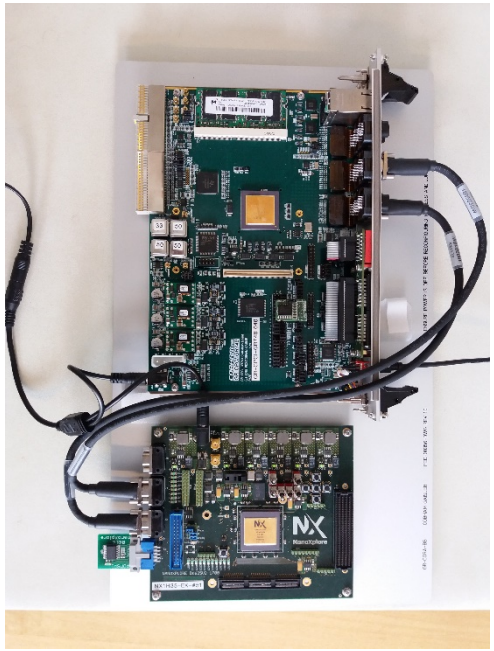


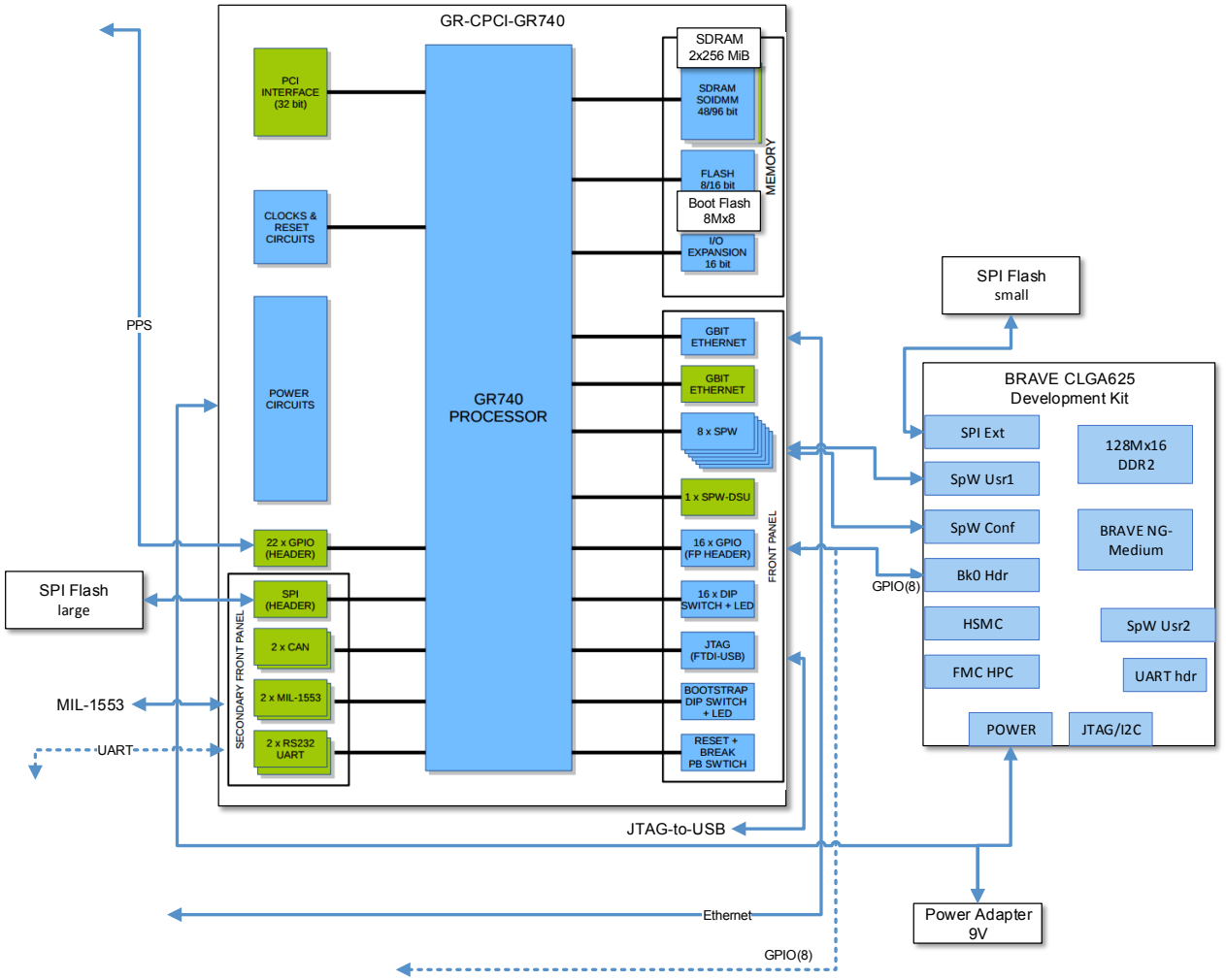
Cobham Proprietary

COTS BB configuration

Delivered to neighbour activities in relation to PDR

- GR-CPCI-GR740 Development Board
- BRAVE NG-Medium Development Kit
- Misc. parts and cables





- Used with SCOE and EGSE and parts of RDHC for SW development

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RDHC configuration

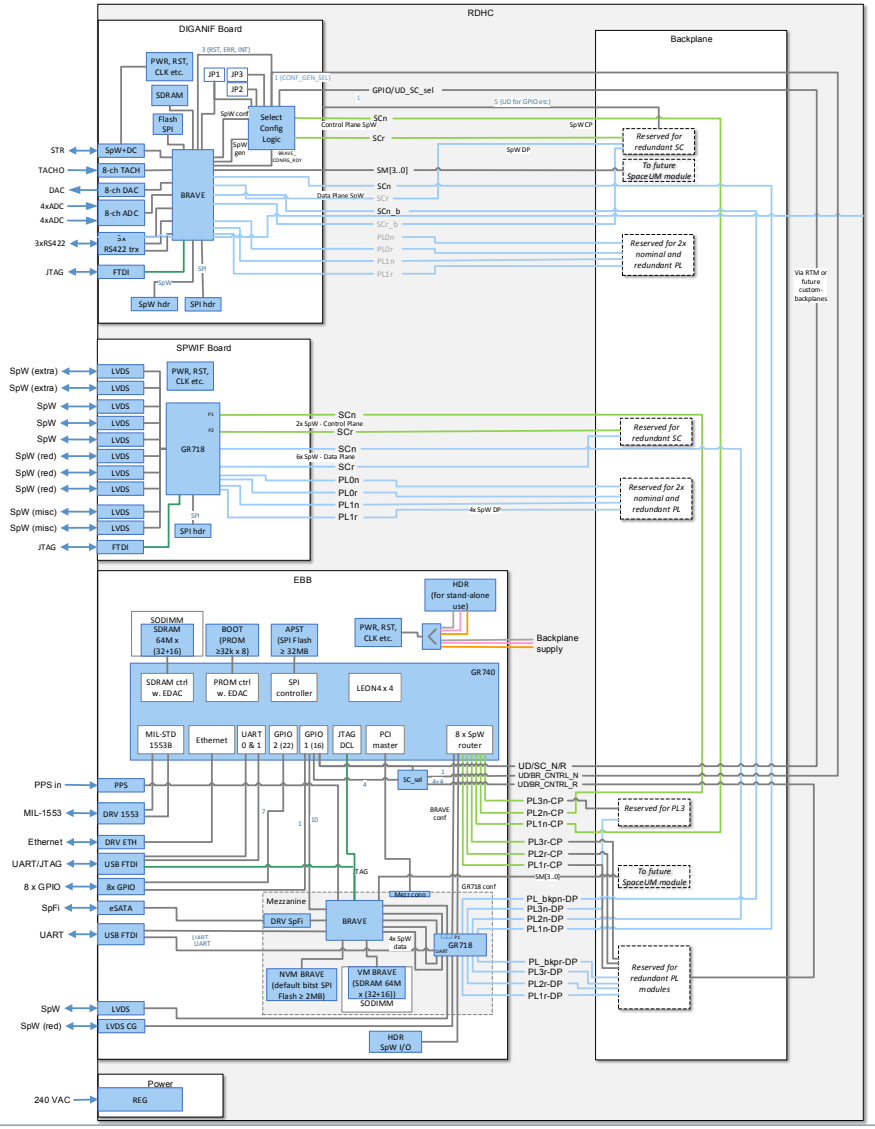
6U OpenVPX designed with SpaceVPX compatibility in mind

Two OpenVPX Payload Modules:

- General I/O Board (DIGANIF)
- SpaceWire I/O Board (SPWIF)

One OpenVPX Switch Module:

- GPP and FPGA Board (EBB with mezzanine)
- Upgradable
- Dataplane would need to be adapted for SpaceVPX compatibility



OpenVPX Backplane (COTS)

COTS chassis and Power module

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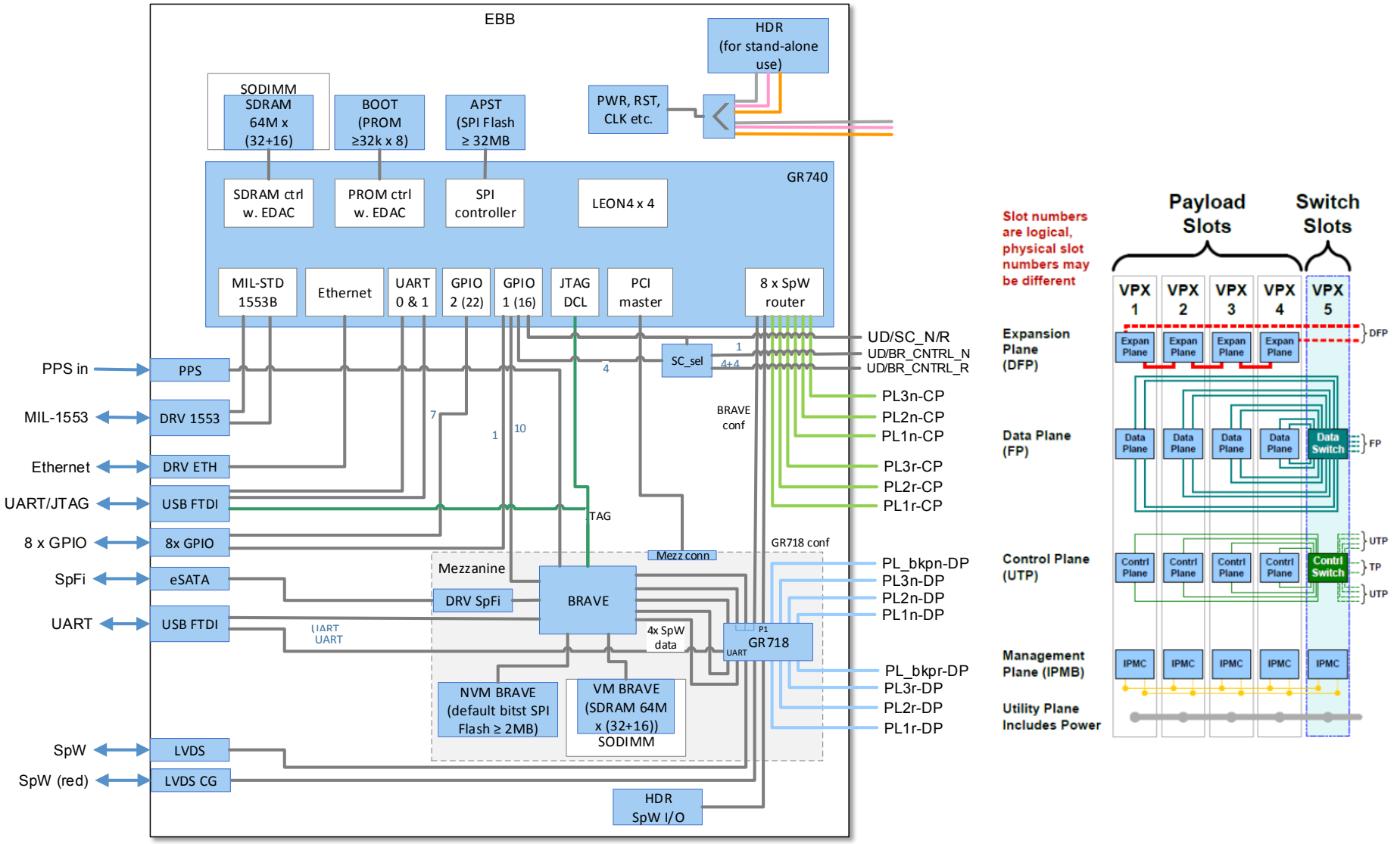
RDHC configuration

EBB – GR-VPX-GR740



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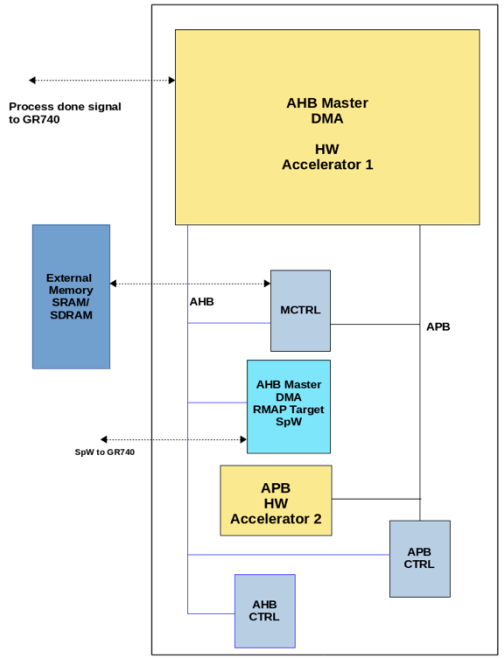
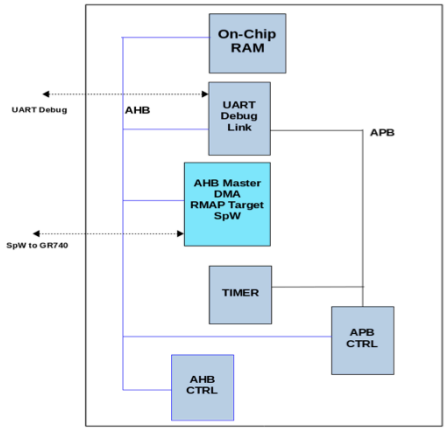
BRAVE as accelerator for GR740

FPGA design architecture

- The processing steps for a set of data to be processed by an accelerator:
  - GR740 using RMAP commands fills the external memory connected to FPGA with the data.
  - The GR740 commands the accelerator to process the data (GR740 RMAP to APB of accelerator).
  - The accelerator process and store it to the external memory.
  - After the process is completed, the accelerator can trigger a process done signal (interrupt) to the GR740 via a GPIO.
  - Based on the "process done" signal, the GR740 can send RMAP read commands to fetch the processed data.



- The first evaluation has been performed with IP's from ESA's IP core portfolio using the BRAVE NG-MEDIUM CLGA625 DevKit V2.
- The design consists of an AMBA bus with SpaceWire RMAP Target, UART debug link, on-chip RAM (128 Kbytes) and other peripheral devices connected on an APB bus.
- Model Based Avionics Development (MBAD) team SW development to "auto generate" FPGA programing files, RDHC team supplies VHDL example design with interface IP from ESA IP core portfolio.



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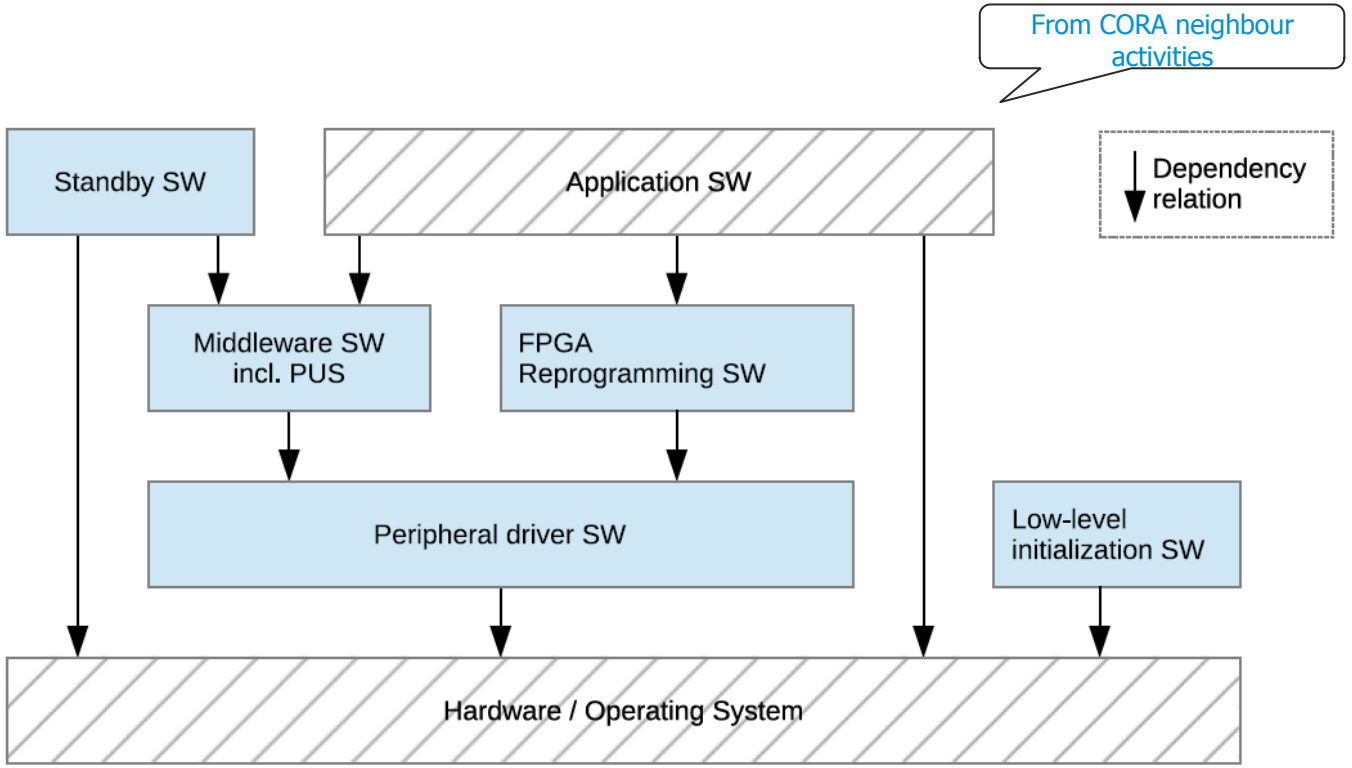
GR740 software architecture

- RDHC platform will be provided with the following software:
  - RTEMS environment including drivers for EBB interfaces
  - Boot loader including self-test and support for in-flight patching of application SW
  - PUS terminal software (middleware) for accepting commands over SpaceWire
  - Driver software for FPGA reconfiguration over SpaceWire (allowing to upload bitstreams through PUS)



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COBHAM

Thank you for listening!