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Overview of the CoRA MBAD activity

Overview of the Compact Reconfigurable Avionics – Model-Based Avionics Design (CoRA-MBAD) activity



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Overview of CoRA MBAD Activity

Separallel to CoRA-MBAD activities : CoRA RDHC and SAGE

- Serime Contractor : Thales Alenia Space in France
- Study Manager : Patricia Lopez Cueva
- SFrom October 2017 to April 2019

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Objective of CoRA MBAD activity



To develop a Model Based Avionics Design Environment and Process permitting the HW/SW co-design at a high abstraction level, and intensively relying on automatic code generation to optimize the development and the performances of compact Reconfigurable Avionics



CoRA MBAD Team



Overview of MBAD System

- SAMBAD System will allow to model the mission phase transitions in the form of state machines
- Solution State Machines will drive the reconfiguration of the system
 - Sky notifying a change of mission phase to SW functional blocks
 - Subscripting the FPGA
- SAMBAD System will automatically generate:
 - All data types and functional blocks interface
 - All functional blocks skeletons
 - So that users only have to worry about implementing functional code
 - Code for communicating SW functions running on the CPU between them and with HW functions executing on the FPGA

- SMBAD System will automatically build
 - The binary to be deployed on the CPU
 - Same the terms of the second s

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Overview of MBAD System



MBAD Use Case Architecture

TM/TC Proxy

- **%**TM/TC Communication via LVCUGEN PUS Library
- **FPGA** Reconfiguration
 - In charge of driving the reconfiguration of the FPGA and informing other blocks of the status of the FPGA, i.e. reconfiguring, active, error.

Equipment

Dedicated blocks will deal with communication with equipment such as the Star Trackers

Mission Phase Manager

- In charge of managing the current mission phase and any mission phase transition
- SA mission phase transition might require reconfiguring the FPGA

HW-only or HW/SW components (VHDL, C or Simulink)

- Set HW-only can be activated only on certain FPGA configurations
- HW/SW can be deployed on CPU or on FPGA depending of the FPGA configuration

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Challenges

Scode generators and build system need to manage the variability in FPGA configurations in order to

- Correctly generate the mapping of HW accelerators so that all parameters are correctly placed in FPGA internal memory
- Correctly synthesize a unique bitfile per FPGA configuration with all functional blocks declared as active on that FPGA configuration
- Correctly generate the inter-functional block communication code taking into account the current FPGA configuration and whether the functional block is deployed in CPU or FPGA for that configuration
- Suture vision
 - MBAD System has been designed and is being developped with future support for partial reconfiguration in mind

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What has been done?

Search Analysis of the Domain of the study has been completed

- Needs and constraints related to target hardware architecture => CoRA RDHC
 - * HW requirements related to interfaces (I/O and between CPU and FPGA) and memory needed
 - Reconfiguration requirements
 - Sasic Software and IP Library requirements.
- Needs and constraints related to modeling tools and coding languages => CoRA SAGE
 - Needs of CoRA SAGE Use Cases as requirements for MBAD System
 - Constraints related to selected tools (TASTE, Bambu, Simulink for autocoding, etc.), coding languages (coding standards) as input for CoRA SAGE Use Cases

Constraints related to Simulink for autocoding were based on outputs of ESA studies on code generation for AOCS Flight Software

- Specification and Architectural Design of MBAD System has been completed
 - Necessary modifications to TASTE Toolset
 - Architecture of a CoRA Use Case
 - SEGSE Architecture

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What is left to do?

Sevelopment activities started in July

- Seartial development of code generators iteratively being tested on Bread Board of Target Platform
- ***** TASTE Template Project for CoRA Use Cases currently being developed => CoRA SAGE

Internal Use Cases (ADS and TAS-F) currently being developed for internal validation of MBAD System once development activities are finished

- SFPGA Reconfiguration
- Sexternal Interfaces
- STR Based Safe Mode
- Salmage Compression algorithm (CCSDS 122.1-B-1) €
- Installation of MBAD System on Elegant Bread Board of Target Platform to be done on the last month of the activity

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Questions?





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