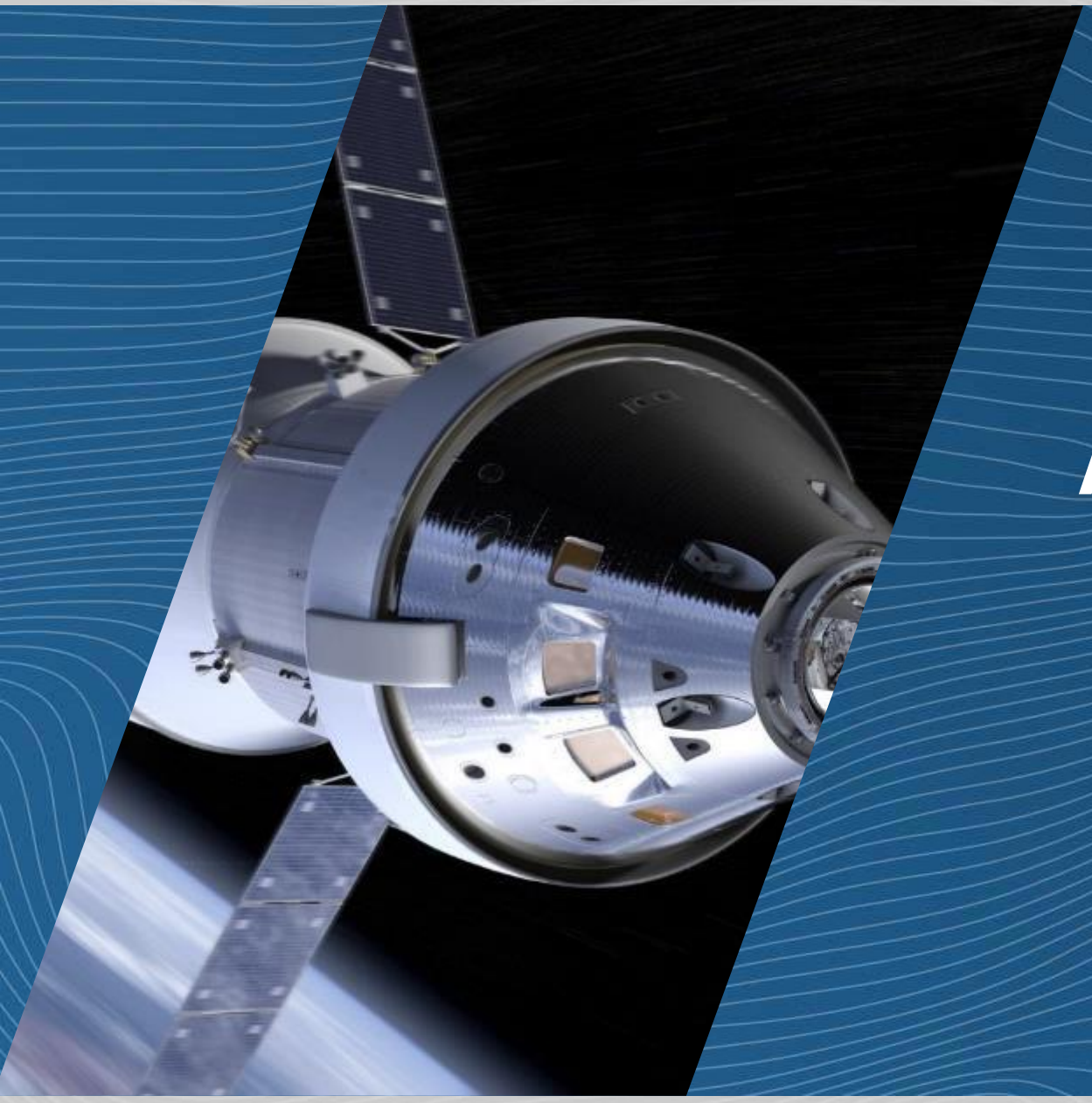

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Application of SpaceWire and SpaceFibre in GR765

Joaquín España Navarro

Cobham Gaisler AB

2022-10-19

International SpaceWire and SpaceFibre Conference 2022

Contents

Background: GR740

Quad-Core LEON4FT Processor

GR740 - Quad-core LEON4FT Processor

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Value proposition

- High performance, wide range of interfaces
- SPARC V8 compliant, Radiation-hard and Fault Tolerant
- Designed as ESA's Next Generation Microprocessor, NGMP
- LEON Technology – re-use of Development and Software ecosystem
- Low risk, off-the-shelf product, QML Q/V qualified
- Excellent performance/watt ratio
  - Very low power, < 3 W (core typical)
  - Performance 1700 DMIPS (1000 MIPS)

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** https://www.dla.mil/LandandMaritime		
	CHECKED BY Phu H. Nguyen			
	APPROVED BY Muhammad A. Akbar	MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 22-04-18			
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DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

esa LEON SPARC Compliant SCD V8

GR740 - Quad-Core LEON4FT Processor

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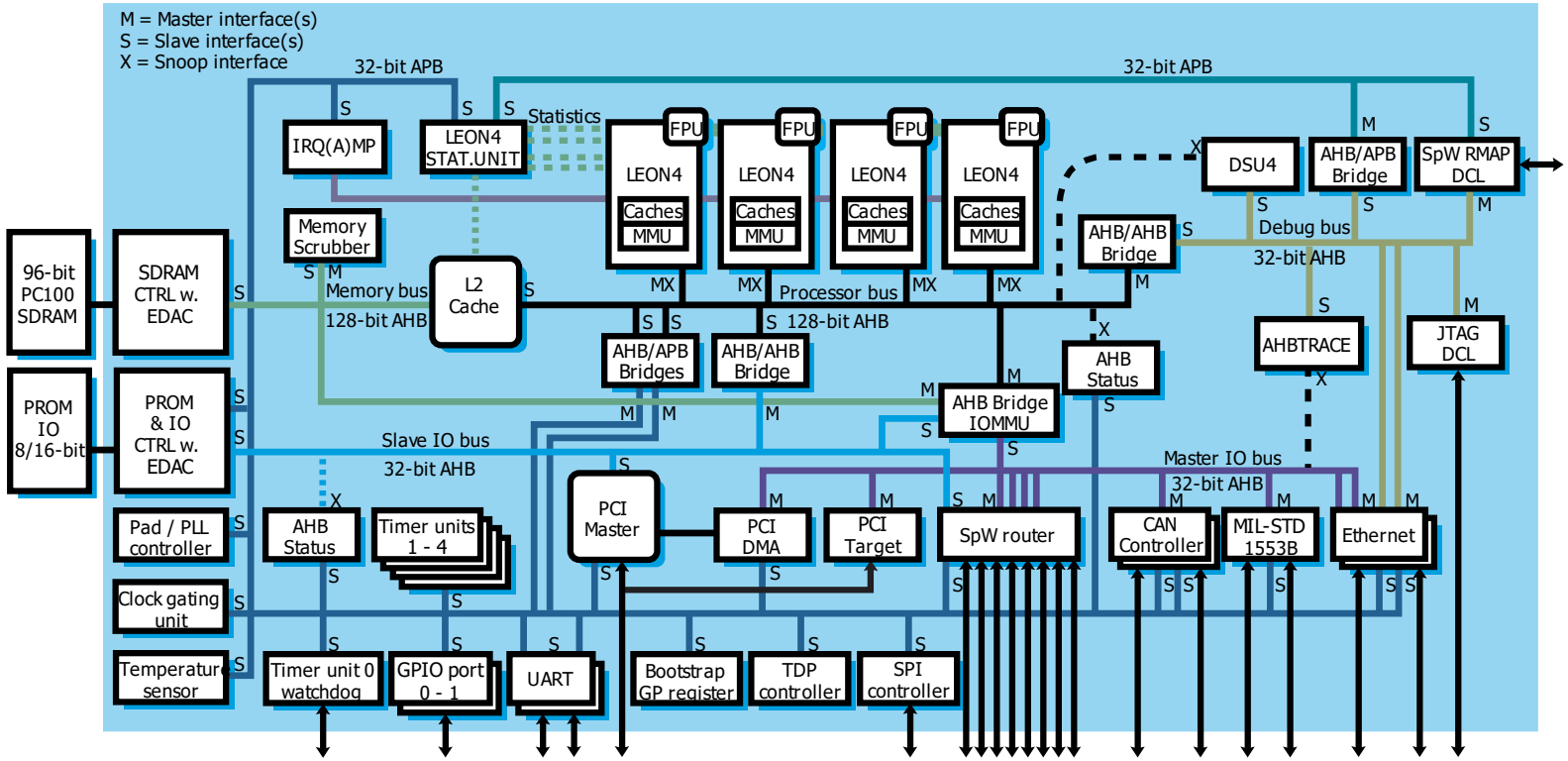
Features

- Fault-Tolerant Quad-processor SPARC V8 integer unit with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches.
- Double-precision IEEE-754 FPU (1 FPU/Core)
- 250 MHz
- >1700 DMIPS
- Power consumption < 3W (core, typical)
- 2 MiB Level-2 cache
- 64-bit PC100 SDRAM memory interface with Reed-Solomon EDAC
- 8/16-bit PROM/IO interface with EDAC
- CPU and I/O memory management units
- Multi-processor interrupt controller with support for asymmetric and symmetric multiprocessing
- SpaceWire TDP controller and support for time synchronisation



Interfaces

- SpaceWire router with 8 SpaceWire links (200 MHz)
- 2x 10/100/1000 Mbit Ethernet interfaces
- 2x MIL-STD-1553B interface
- 2x CAN 2.0 controller interface
- 2x UART, SPI, Timers and watchdog, 16+22 pin GPIO
- PCI Initiator/Target interface
- JTAG

GR765

Next-Generation SoC

GR765 – Overview

- **Phase 1A (funded): DARE65 Demonstrator** – Downsized implementation of GR765 architecture. Availability TBD for eval board with plastic parts in 2023.
- **Phase 1B/2A/B (funded): GR765-XX** – GR765 implementation. Goal is 2024 component availability. Projects started.
- **Phase 3A/B: GR765-CP/MP/MS** – GR765 product (same design as GR765-XX) with Qualification & production flows/temperature ranges available as per other CAES standard products. Availability (flight models) is TBD.
- **Phase C: GR765-*-C(C/L)GA** – Ceramic package development
- **Complemented by:** ESA Fifth Generation Space Microprocessor development

GR765 is a new component development based on an extended GR740 SoC design

The development of the demonstrator and the updates of the SoC design to form the GR765 are undertaken in ESA GSTP and NAVISP EL2 activities with funding from the Swedish National Space Agency and CAES.

Disclaimers:

GR765 Effort is on-going & subject to change without notice. Currently there is no guarantee of a product launch.

Contact CAES Gaisler to receive the latest available information.

Computing Roadmap – 2022, September

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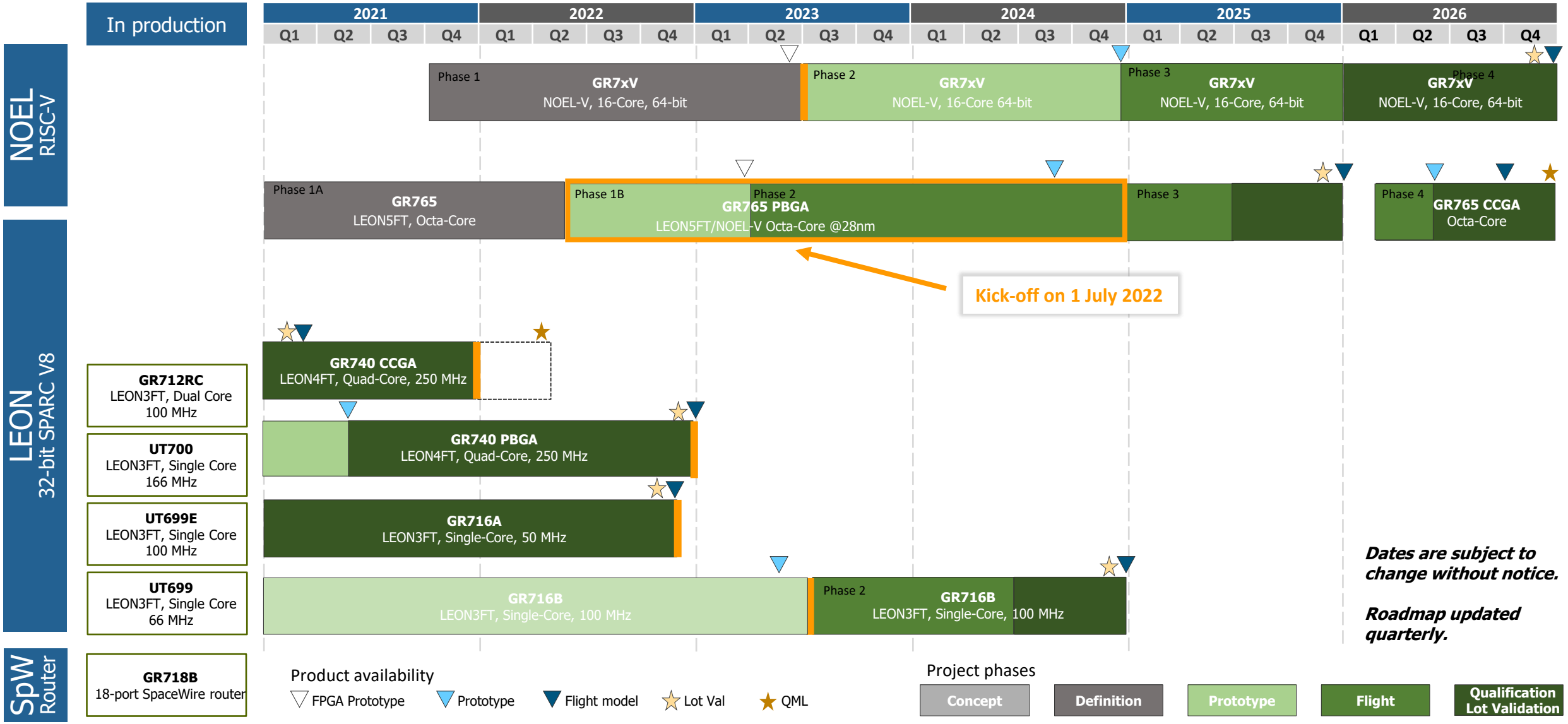


Instruction Set Architectures

Why RISC-V?

- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain
- Hardware and software potential for future space applications: A new class of processors requires a modern architecture

Why SPARC?

- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

GR765 provides RISC-V and SPARC

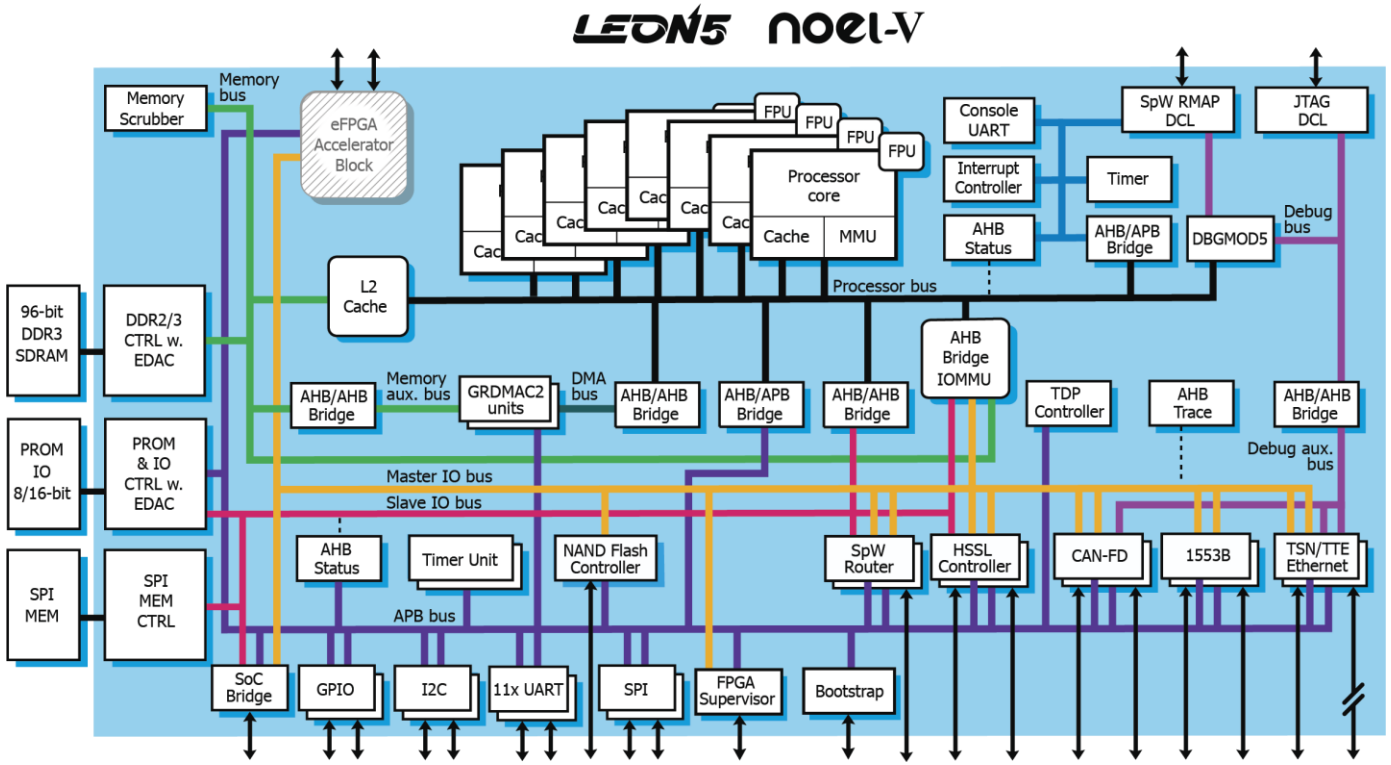
- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC - single component development investment and qualification effort
- Minimal silicon overhead - sharing of resources on chip - User will select CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.
- De-risking early stages of new application development
  - The architectural choice can be evaluated easily

GR765 – Octa-Core Processor

In development
No guarantee of product launch

Baseline Features

- Fault-tolerant **octa-core, user selectable CPU core**
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- LEON5FT provides backward compatibility with GR740 and earlier LEON implementations
- NOEL-V/GR765 provides RISC-V compatibility through conformance to the OS-A (Base) RISC-V Platform Specification
- **1 GHz processor frequency - 26k DMIPS**
- 2+ MiB L2 cache, 256-bit cache line, 4-ways
- **DMA controllers**
- **DDR2/3 interface with dual x8 device correction capability**
- **(Q)SPI and NAND memory controller interfaces**
- **eFPGA ~30k LUT (TBD)**
- **High-pin count – LGA1752**
- **Reduction of pin sharing**
- **Target technology: STM 28nm FDSOI**

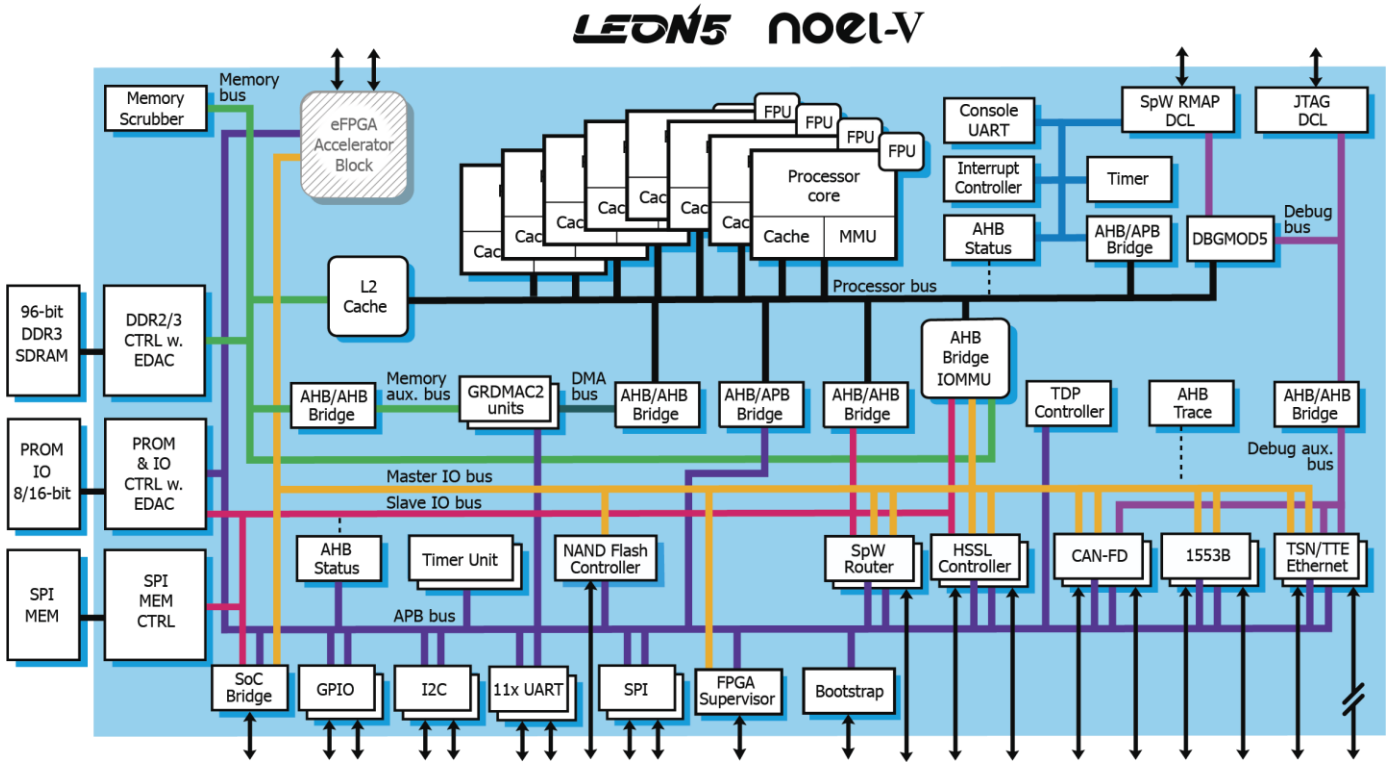


GR765 – Octa-Core Processor

In development
No guarantee of product launch

Interfaces

- **SpaceFibre x4+ lanes 6.25 Gbit/s, simpler protocols**
- **12-port** SpaceWire router with +4 internal ports
- 2x 10/100/1000 Mbit Ethernet
- **2x or 3x TT / TSN Ethernet support**
- **2x** MIL-STD-1553B
- **2x CAN-FD**
- **2x I2C interface**
- **12** x UART
- **2x** SPI master/slave
- **SoC Bridge interface**
- **FPGA Supervisor interface**
- Timers & Watchdog, GPIO ports
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, SpFi, Ethernet

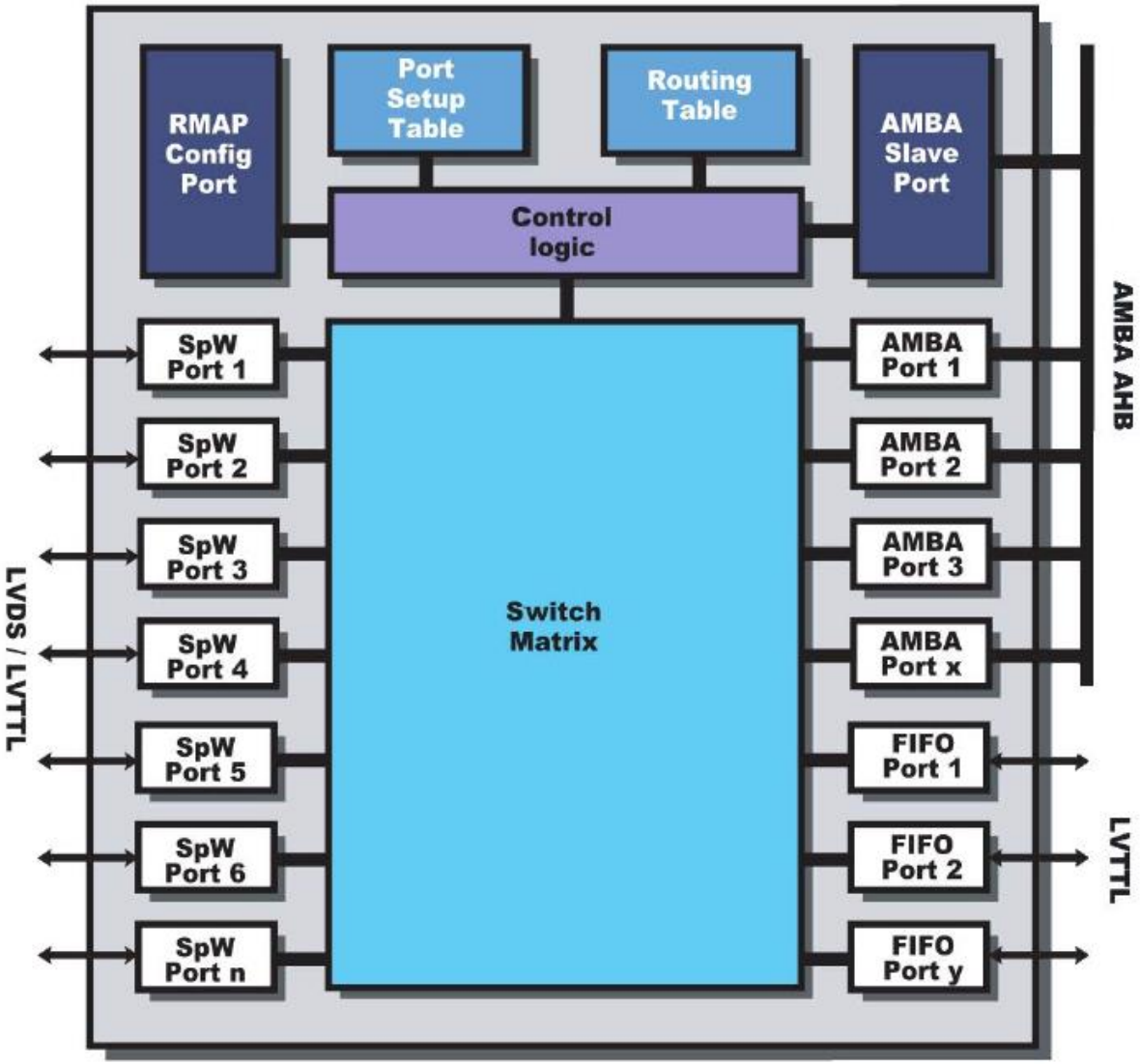


GR765

SpaceWire and SpaceFibre support

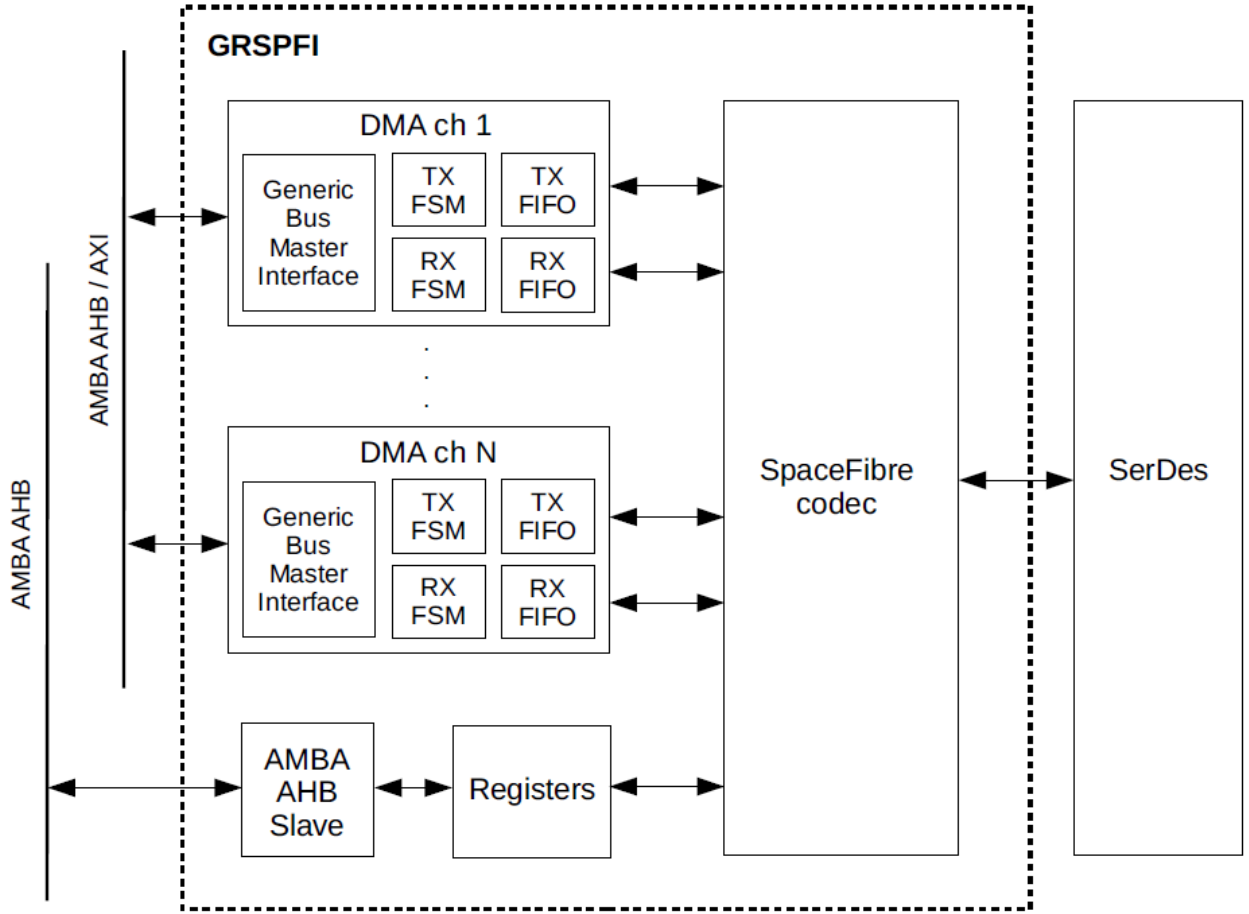
GR765 – SpaceWire router

- GRSPWROUTER implemented as per ECSS-E-ST-50-12C specification
- Features three types of ports:
  - SpaceWire ports (external ports)
  - FIFO ports (internal ports)
  - AMBA ports (DMA)
- GR765 extends the number of external ports from 8 to 12 and keeps 4 internal ports
- AMBA ports include an RMAP target and several DMA channels
- Configuration port with RMAP target to allow independent operation from the processor / software
  - The router can be configured by SpaceWire nodes without processor intervention
- Two main applications:
  - SpaceWire connectivity for the processor cores
  - Routing capabilities for external SpW nodes



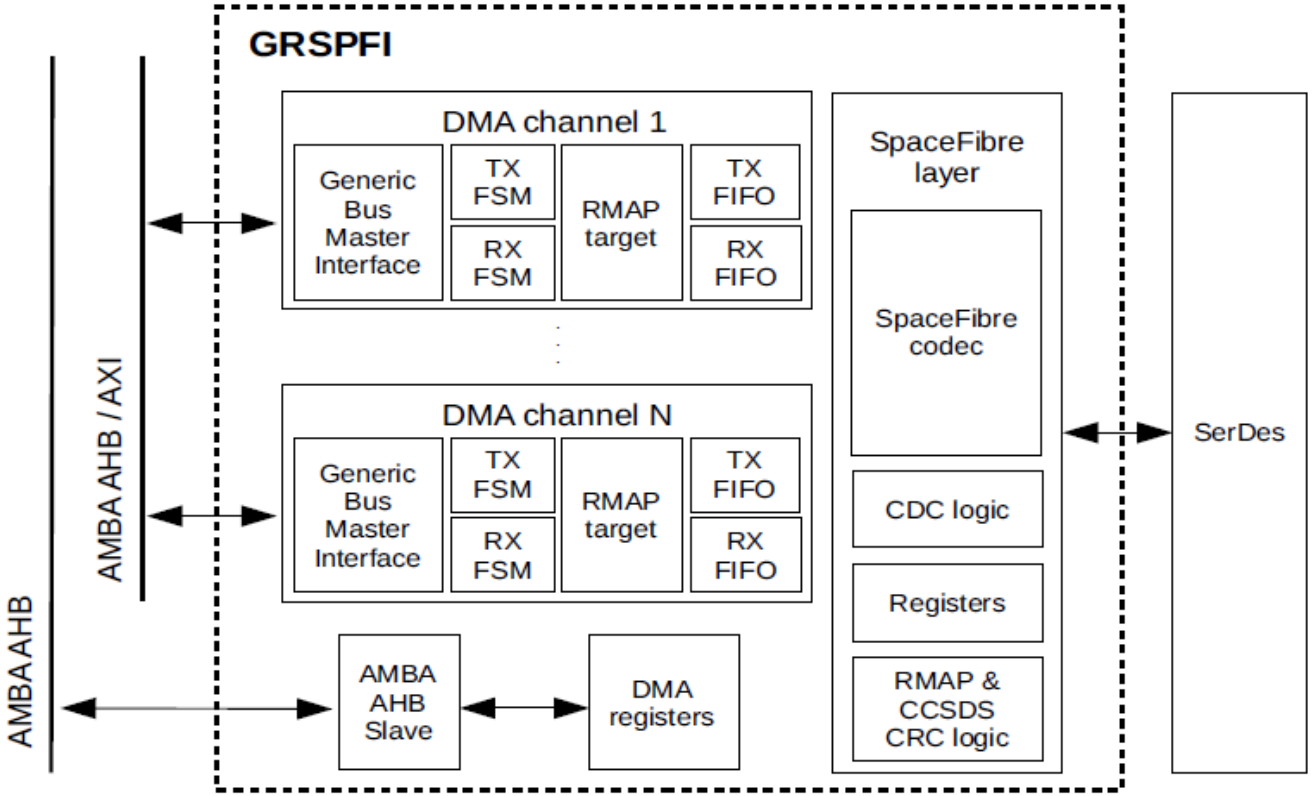
GR765 – SpaceFibre interfaces

- GR765 will include 4 SpaceFibre interfaces supporting up to 6.25 Gbps
- SpaceFibre codec designed according to the ECSS-E-ST-50-11C standard
- Single lane implementation
- Flexible DMA engine with multiple DMA channels
  - Each channel has its own AHB master i/f
  - DMA channels operate in parallel and are assigned a subset of Virtual Channels and/or the Broadcast Channel
- AHB slave interface for configuration and control
- On-chip SerDes: STMicroelectronics 28nm FDSOI Rad-hard IP
- Required extensions for the GR765:
  - RMAP support
  - Integration with GRSPWROUTER
  - ST SerDes integration
  - Companion WizardLink controller



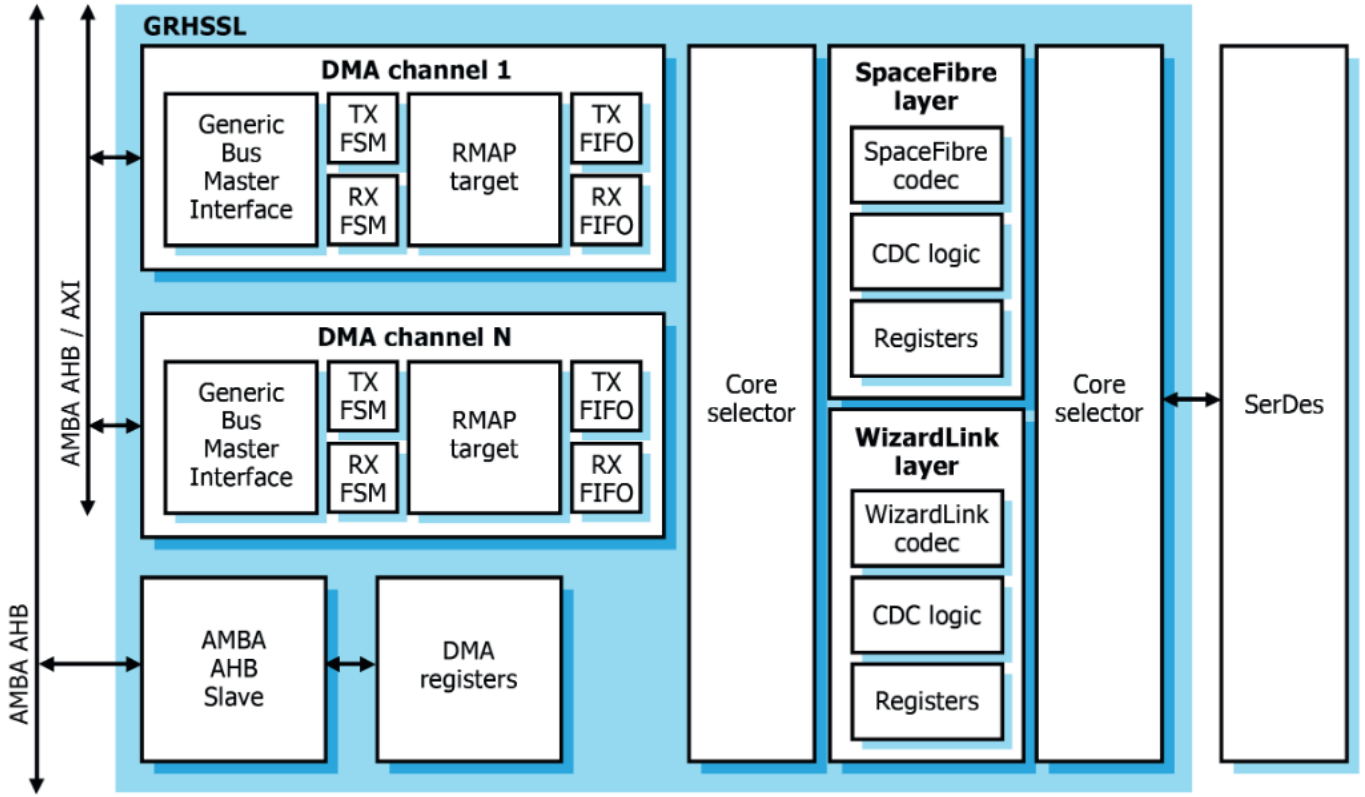
GR765 extensions: SpFi RMAP support

- RMAP support added to the SpaceFibre DMA engine as per ECSS-E-ST-50-52C
- Same level of support as in GRSPW2, the SpaceWire controller in GRLIB:
  - DMA ports in GRSPWROUTER
  - Features may be extended, e.g., verify buffer size, alignment restrictions, etc.
- Dedicated RMAP target per DMA channel
  - Make use of the dedicated AHB master interface of every channel
- RMAP can be separately enabled/disabled and configured in run time for each virtual channel
  - Each VC has a dedicated node address and destination key register
- Standalone RMAP CRC-8, CCSDS CCITT CRC-16 and 16-bit Checksum (J.G. Fletcher, ISO 8473-1:1998) logic for generic packets



GR765 extensions: WizardLink

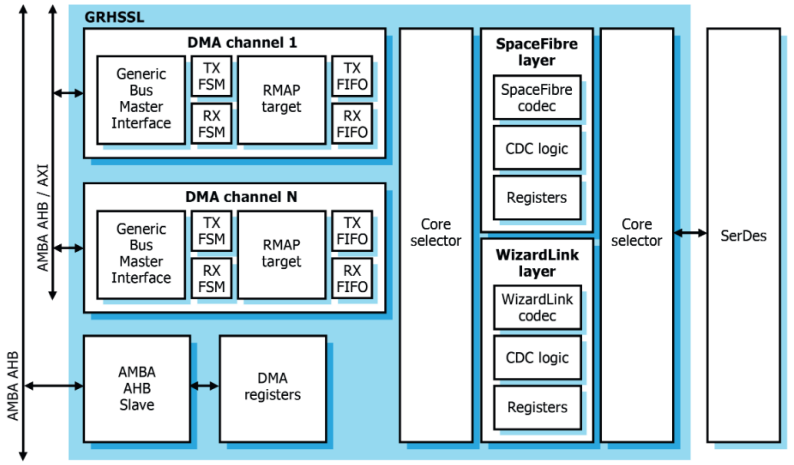
- Companion WizardLink controller designed to interoperate the TLK2711 transceiver
  - Compatible also with other SerDes
- Enable the communication with legacy equipment using custom protocols over WizardLink
- Minimal hardcoded functionality, high degree of configurability
- Transmission and reception of packets handled via hardware descriptors
  - Control characters need to be handled by software
- Configurable commands via AHB registers to automatically insert or extract control words
  - IDLE characters are mandatory
  - Other control words are optional
- Only one controller (SpaceFibre or WizardLInk) can be active at a time, selectable at run-time via AHB registers

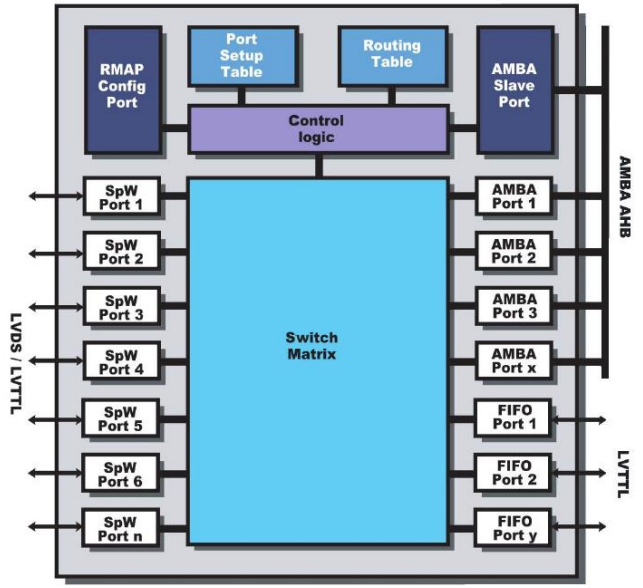


GR765 extensions: SpW/SpFi & SerDes

Integration of SpaceFibre with the SpaceWire router

- Bridge between SpaceWire and SpaceFibre traffic
- Configurable number of FIFO interfaces directly exposed to the output of GRSPFI
- Dynamic assignment of Virtual Channel to external FIFO interfaces at run-time via AHB registers
- Exposed Virtual Channels bypass the DMA engine
- External SpaceFibre ports can then be connected to the SpaceWire internal FIFO ports
- Minor adaptations in GRSPWROUTER required
  - Word to byte conversion
  - Handling of EOP, EEP and FILL characters





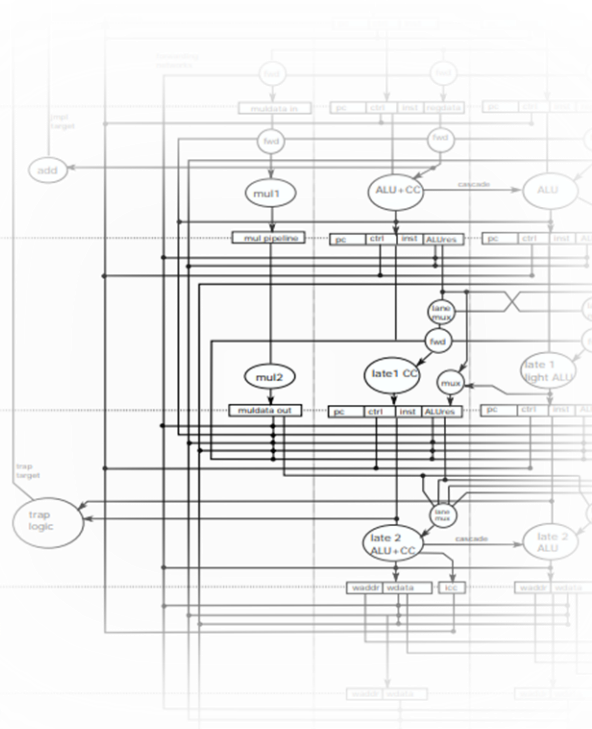
Integration with the ST 28nm SerDes macro

- Ongoing effort to ensure interoperability with the on-chip SerDes
- Rad-hard macro supports up to 23 Gbps
- Aim is to support the full SpaceFibre range including 6.25 Gbps
- Exploit configurability of the SerDes IP

Conclusions

Conclusions

- The GR765 development builds on the successful GR740 quad-core LEON4FT component
- The GR765 includes an **octa-core** LEON5FT. Users can enable NOEL-VFT RISC-V 64-bit processor cores instead of the LEON5FT cores
- GR765 supports DDR3 SDRAM, high-speed serial link controllers and several other extensions
- SpaceWire router expanded: 12 external and 4 internal ports
- Four SpaceFibre links with on-chip SerDes supporting up to 6.25 Gbps
- SpaceFibre DMA engine with RMAP target based on GRSPW2 to facilitate SW migration
- SpFi / SpW bridging by mapping Virtual Channels to SpW router FIFO ports
- Companion WizardLink controller to enable communication with legacy equipment
- GR765-XX (prototype) components are planned to go into manufacturing within 2023



Progress to be reported via www.gaisler.com/GR765

CAES

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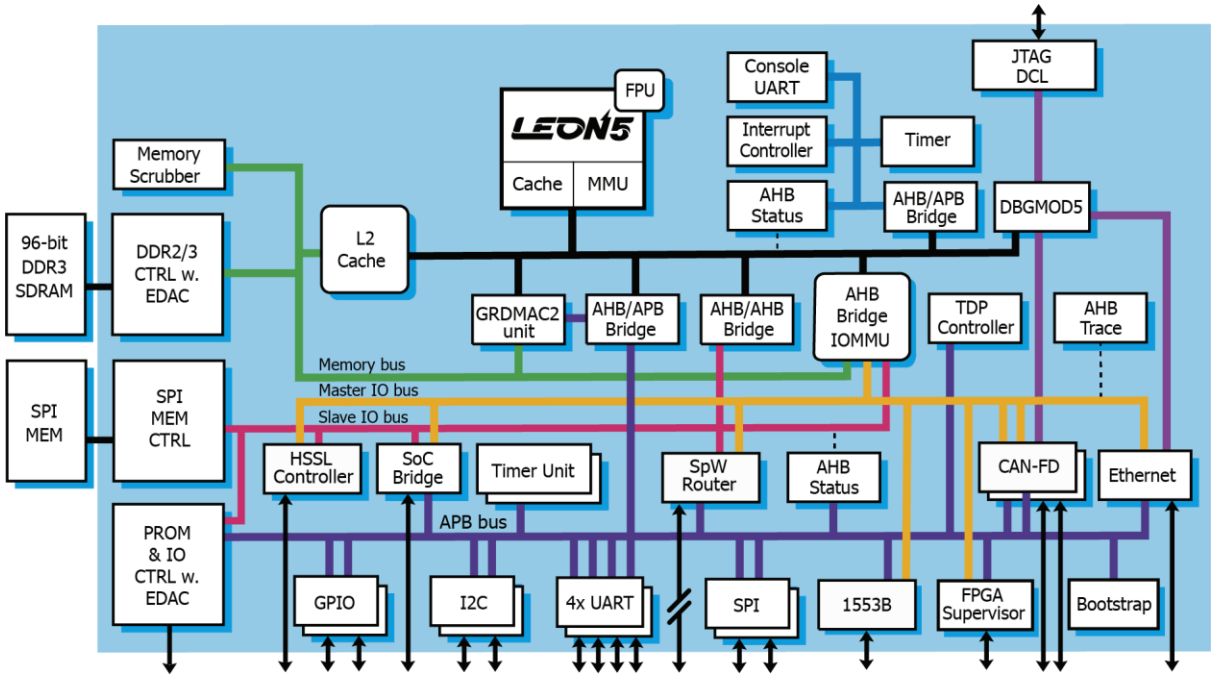
EXTRA

D65D – Rad-Hard LEON5FT Processor

In development
No guarantee of product launch

Baseline Features

- Fault-tolerant SPARC V8
- **LEON5FT** with dedicated FPU and MMU, 32 KiB per core L1 cache, connected to 128-bit bus
- 200 MHz processor frequency
- 128 KiB L2 cache, 256-bit cache line, 2-ways
- Standalone DMA controller
- High pin-count PBGA
- Technology: DARE65 / TSMC 65 bulk CMOS



Memory interfaces

- DDR2/3 interface with dual x8 device correction capability
- SPI memory controller interface
- Parallel boot/IO interface (8/16-bit)

Interfaces

- SpaceFibre 2.5 Gbit/s
- 4-port SpaceWire router with one internal port
- 10/100/1000 Mbit Ethernet
- MIL-STD-1553B, 2x CAN-FD, 2x I^2C interface
- 4 x UART, 2x SPI master/slave, Timers & Watchdog, GPIO ports
- SoC Bridge interface
- FPGA Supervisor interface

GR740 vs DARE65 Demo vs GR765

Parameter	GR740	DARE65 Demo	GR765
Technology	ST C65SPACE (65nm bulk CMOS)	imec DARE65 (TSMC 65nm)	STM 28nm GEO P2
Availbility	CCGA now, PBGA in devel	TBD	Prototypes 2023 FM 2024/2025
Temp range	MIL	MIL	MIL
Quality	QML-V	Vendor class S / ESCC9000 lot validation	QML or equivalent for plastic QML-V target for ceramic
Rad tolerance (SEL)	125 MeV.cm²/mg	TBD	TBD
Rad tolerance (TID)	300 krad	300 krad (TBC)	50 krad (TBC)
Rad tolerance (SEE)	1E-5 events/device/day	Target GR740	Target GR740
Operating frequency	250 MHz (WC corner)	200 MHz	1 GHz
Power (core)	< 2 W @ room, < 3 W	4 W (TBC)	Target < 3 W
Processor core	LEON4FT SPARC V8	LEON5FT SPARC V8	LEON5FT SPARC V8 & NOEL-V RV64
Number of cores	4	1	8
Performance, peak, MIPS	1000	1200	16000
Performance, peak, DMIPS	1900	1938	25840
Performance, estimated, in CM	1970	2712	28k9

GR740 vs DARE65 Demo vs GR765

Parameter	GR740	DARE65 Demo	GR765
Primary memory interface	SDRAM	DDR3 SDRAM	DDR2 SDRAM DDR3 SDRAM
L2 cache size	2 MiB	256 KiB	2 MiB
eFPGA	No	No	TBD - Target 32k LUT eFPGA
High-Speed Serial Link	No	2.5 Gbps SpFi, external TLK2711	6.25 - 12 Gbps, 4 lanes SpFi, Wizlink, PCIe (TBD) on-chip SerDes
SpaceWire router	8 external ports	4 external ports	12 external ports
Parallel PCI	Yes	No	No
Ethernet	2x 10/100/1000	1x 10/100/1000	2x 10/100/1000 3x TSN/TTE (TBD)
MIL-STD-1553B	1	1	2
CAN	2.0B	FD	FD
UART	2	5 + 1	11 + 1
SPI	1	2	2
I2C	No	2	2
NAND Flash i/f	No	No	Source sync NV-DDR2 TBD NV-DDR3 TBD
Package	CCGA625 / PBGA625	PBGA	LGA1752 plastic first, ceramic later