A LOW-OVERHEAD AXI BRIDGE ON SPACEWIRE FOR MULTI-DEVICE SPACECRAFT SYSTEMS

Authors: Claudio Rubattu[1], Walter Errico[1] and Kostas Marinis[2]

Presenter: **Luca Meucci**[1]

[1]SITAEL S.p.A. (ITA), [2]ESA - ESTEC (NL)

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Outline

- **Introduction**
  - Context
  - Background
  - Motivation

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- **System Overview**

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  - Read Transaction
  - Write Transaction

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  - Response Time Evaluation

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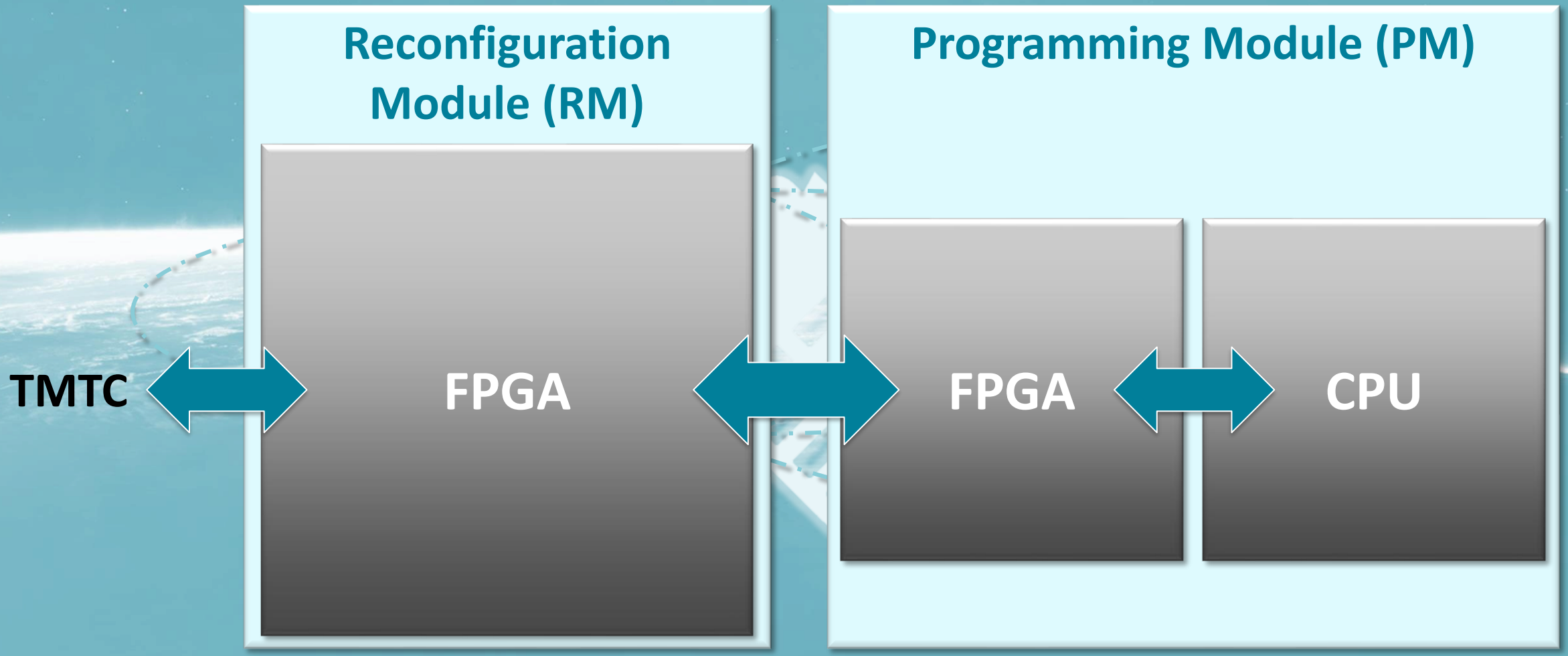
Context



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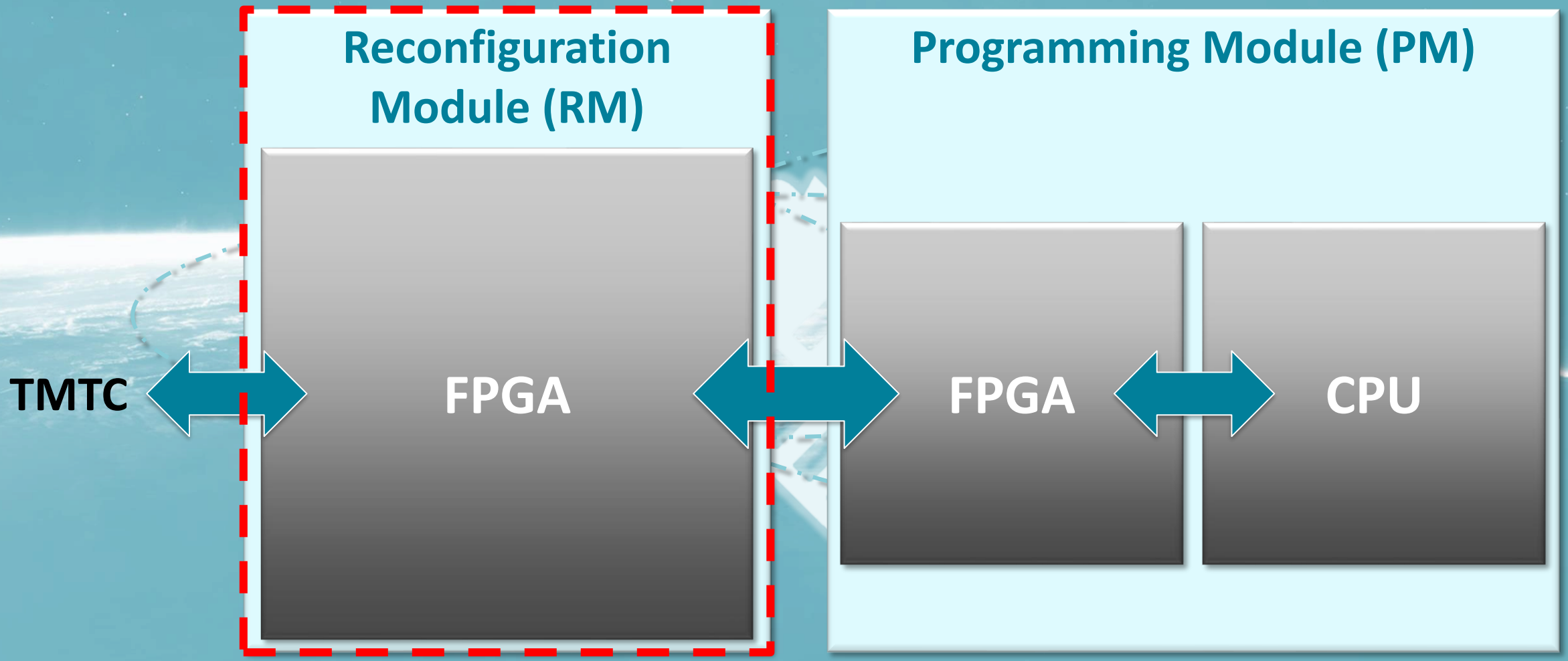
Context



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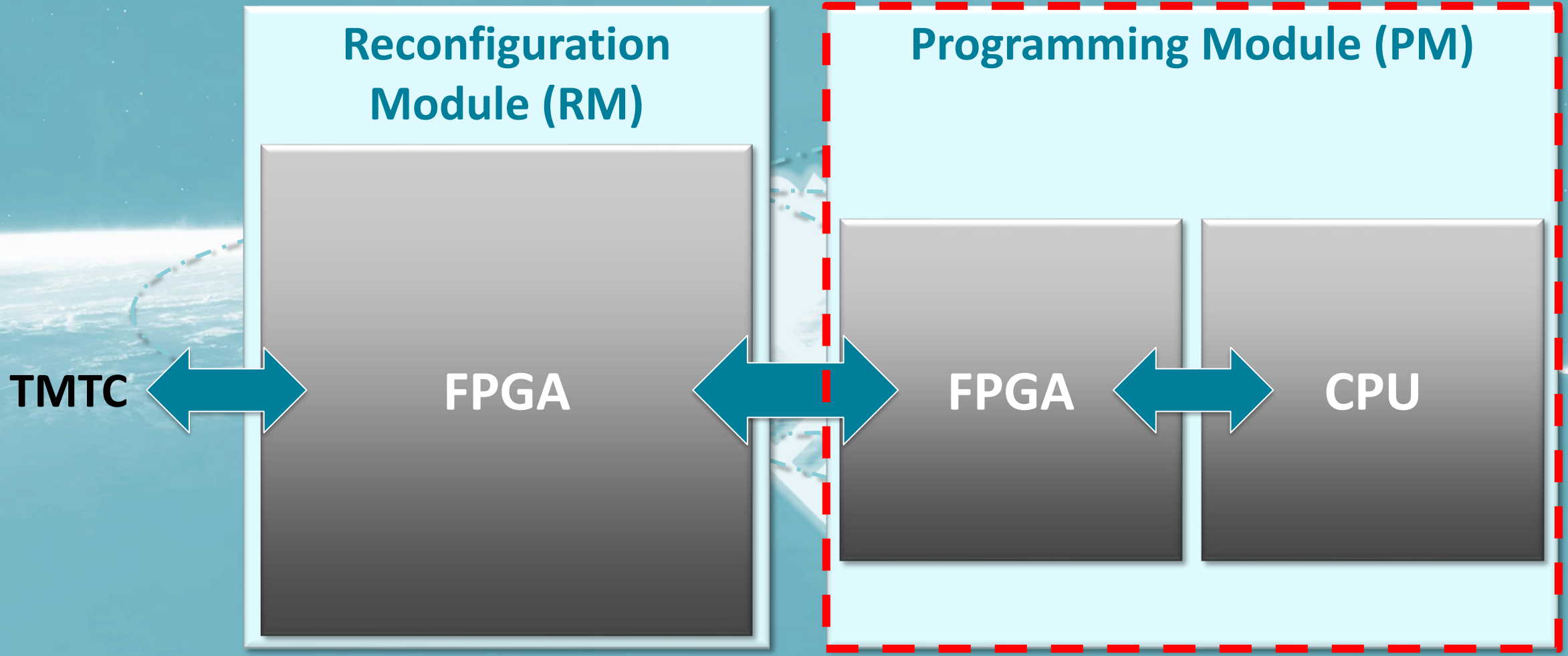
Context



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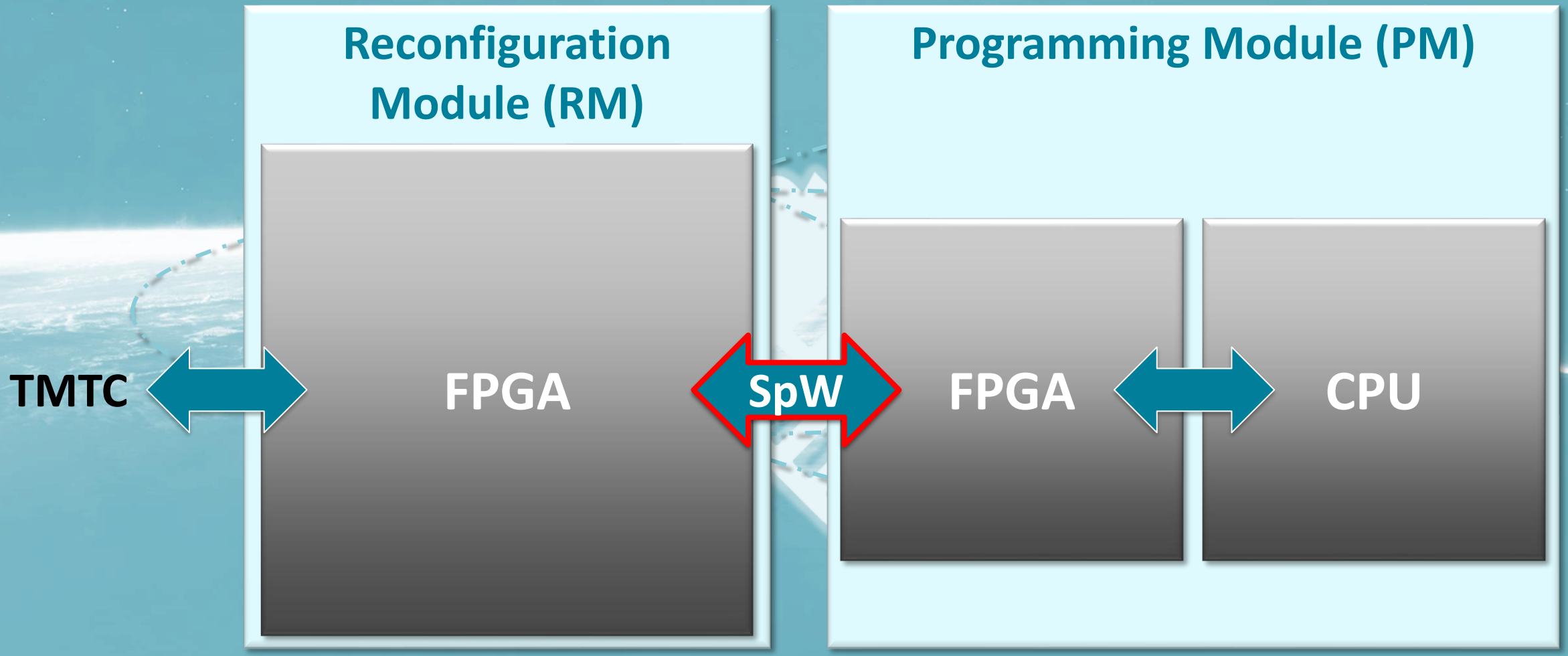

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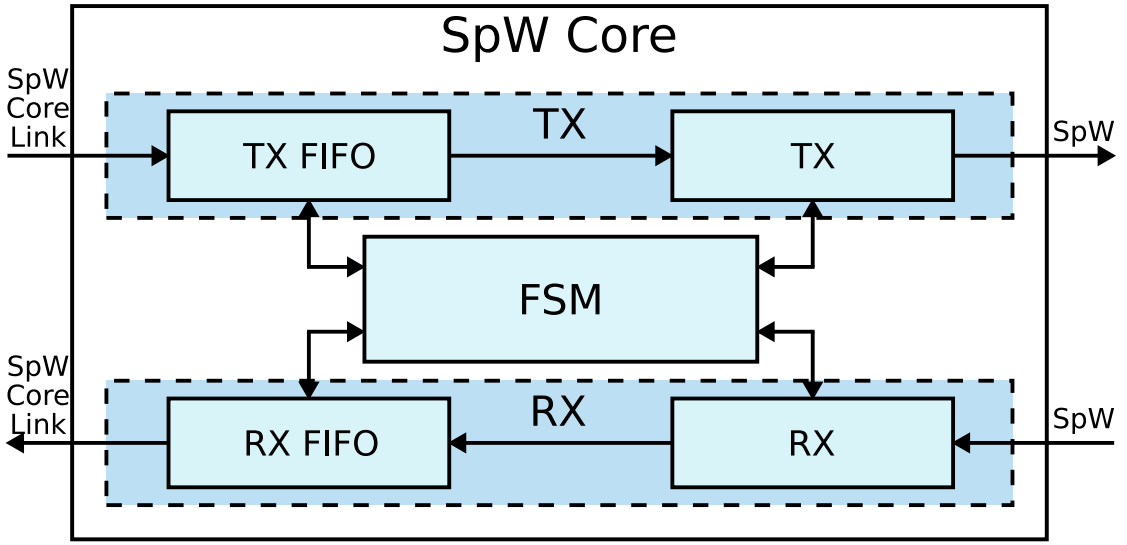
Background: SpaceWire (SpW) Core



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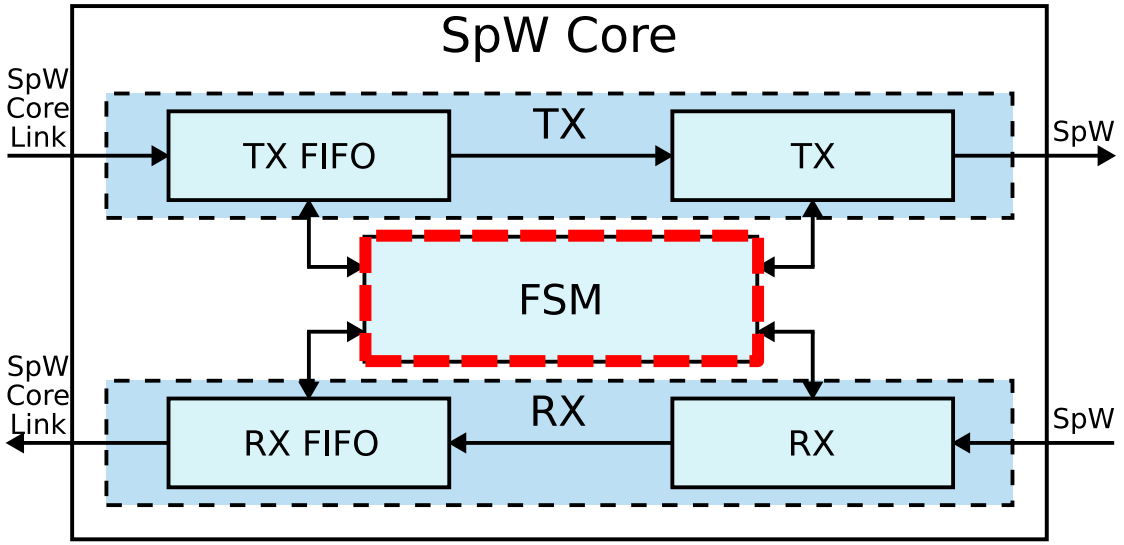

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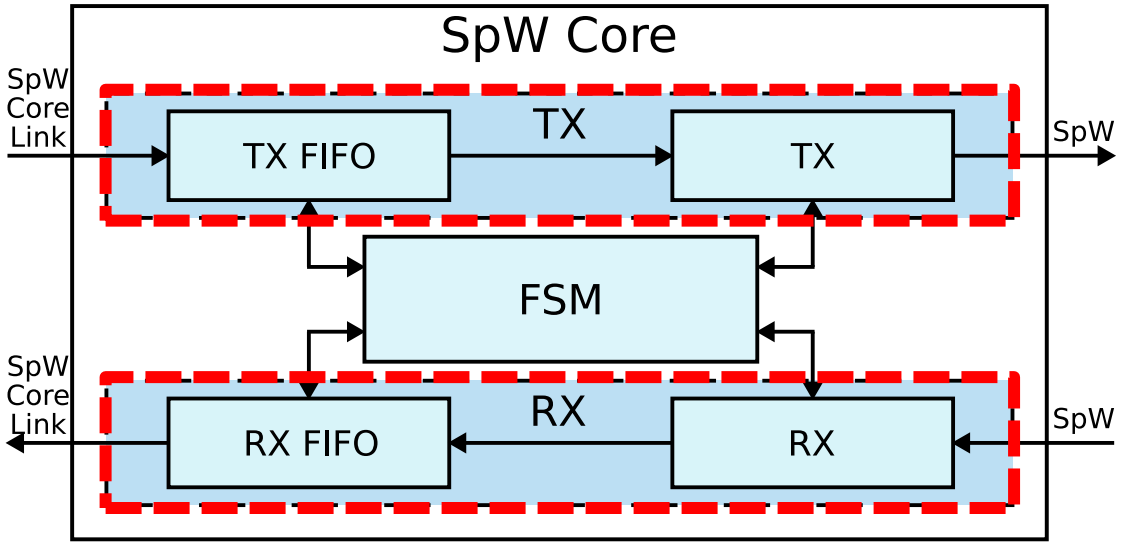

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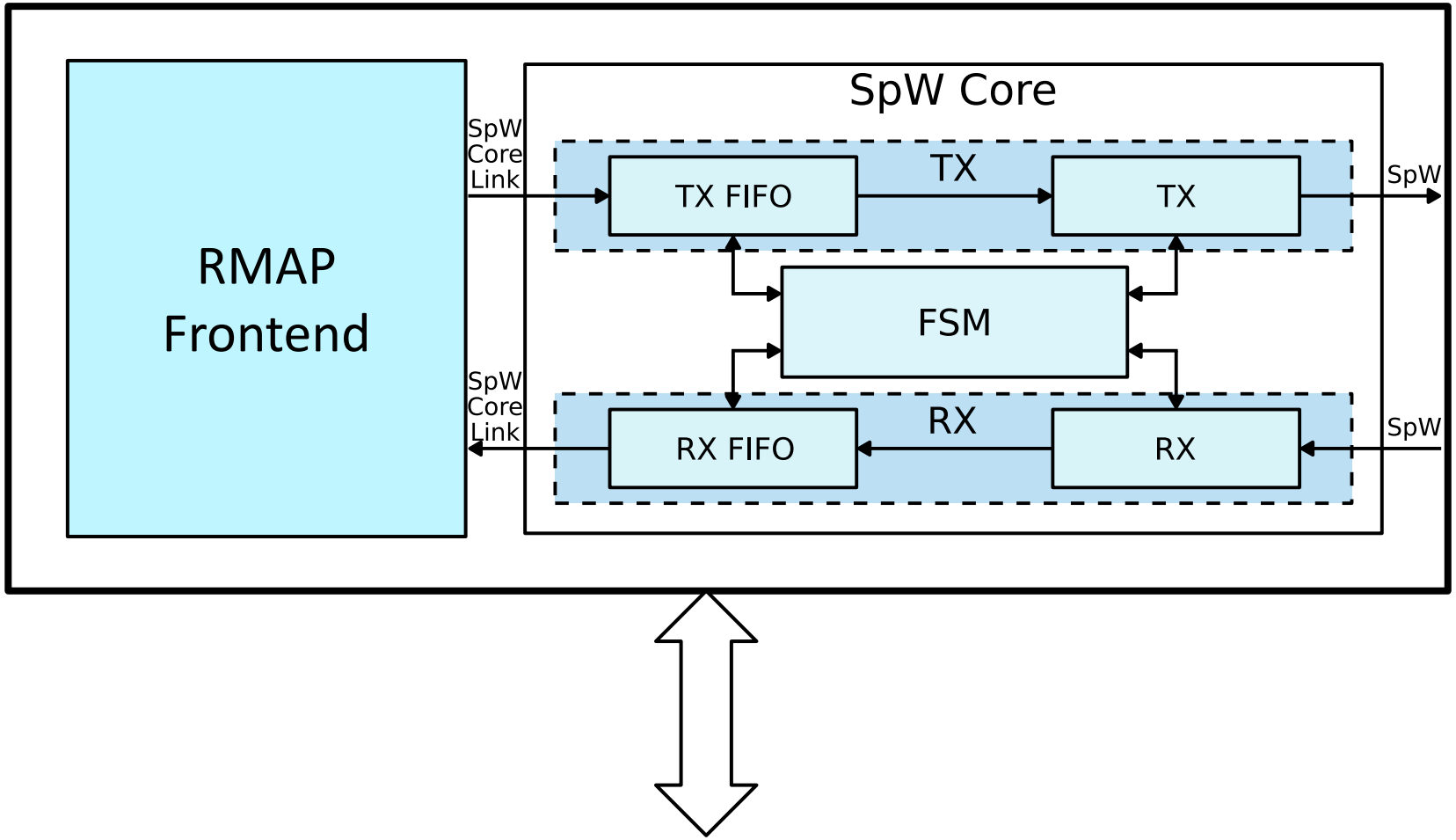

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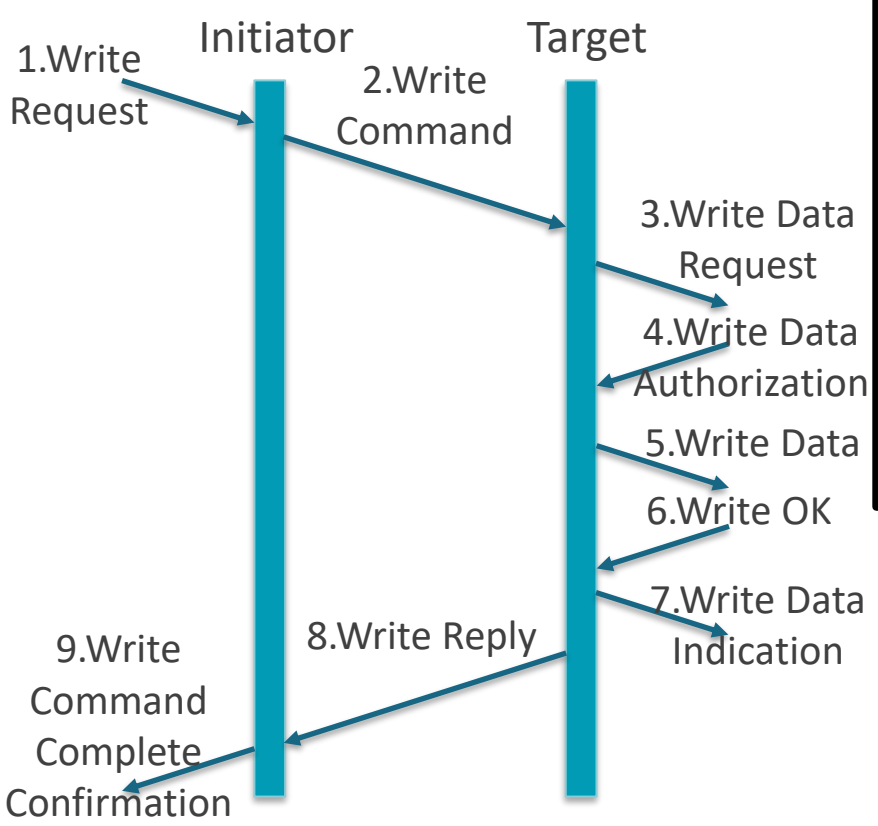
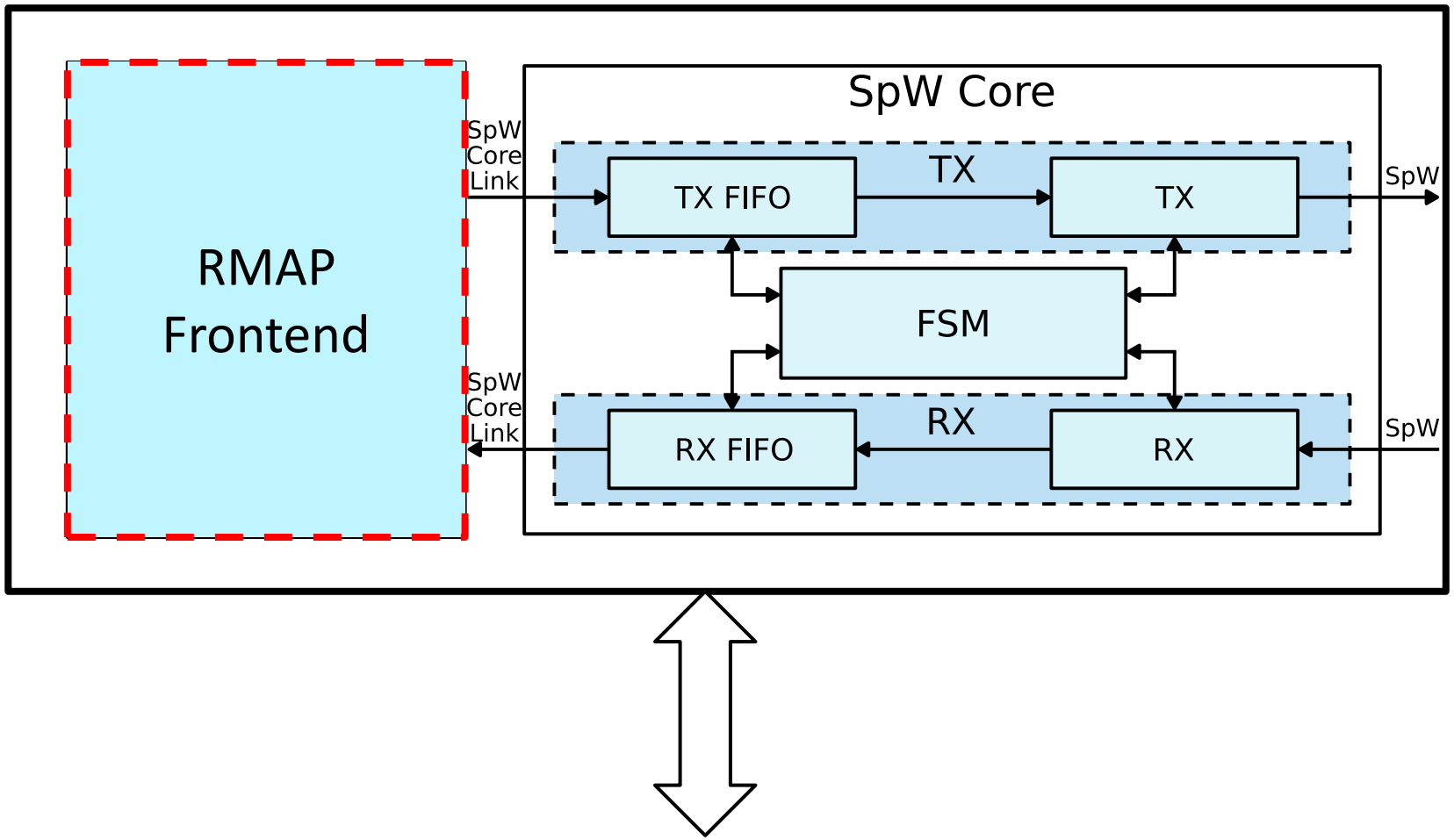
Background: SpaceWire (SpW) Core

Remote Memory Access Protocol (RMAP)





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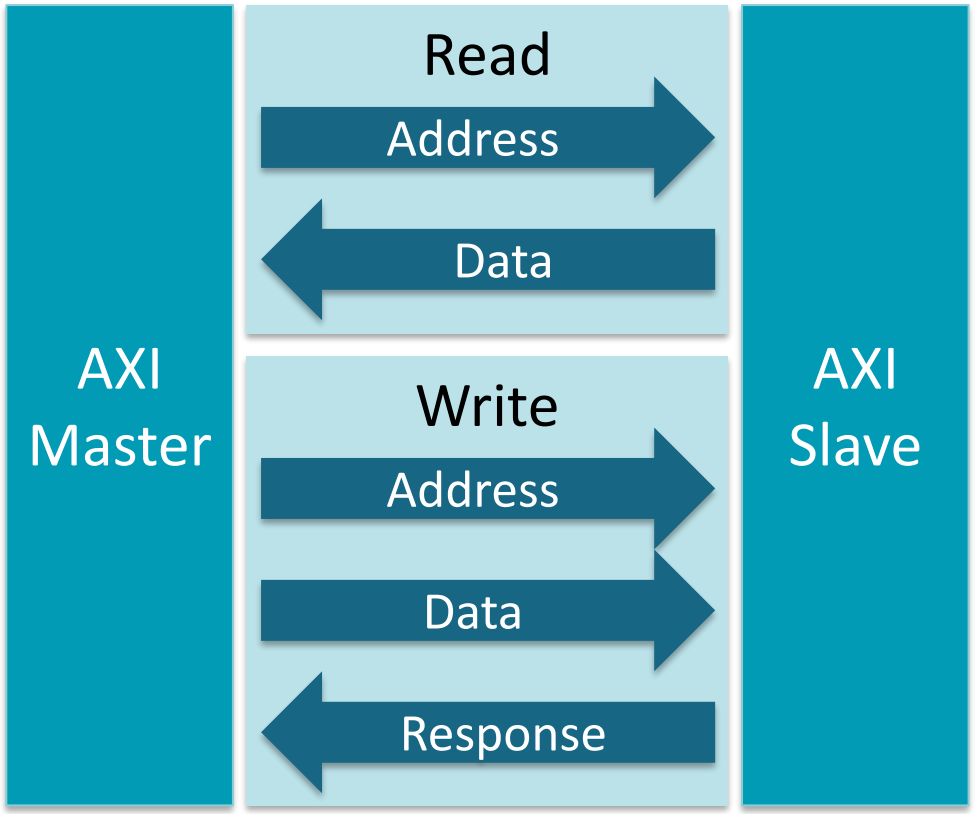
Background: Advanced eXtensible Interface (AXI)

AXI Transactions

arm



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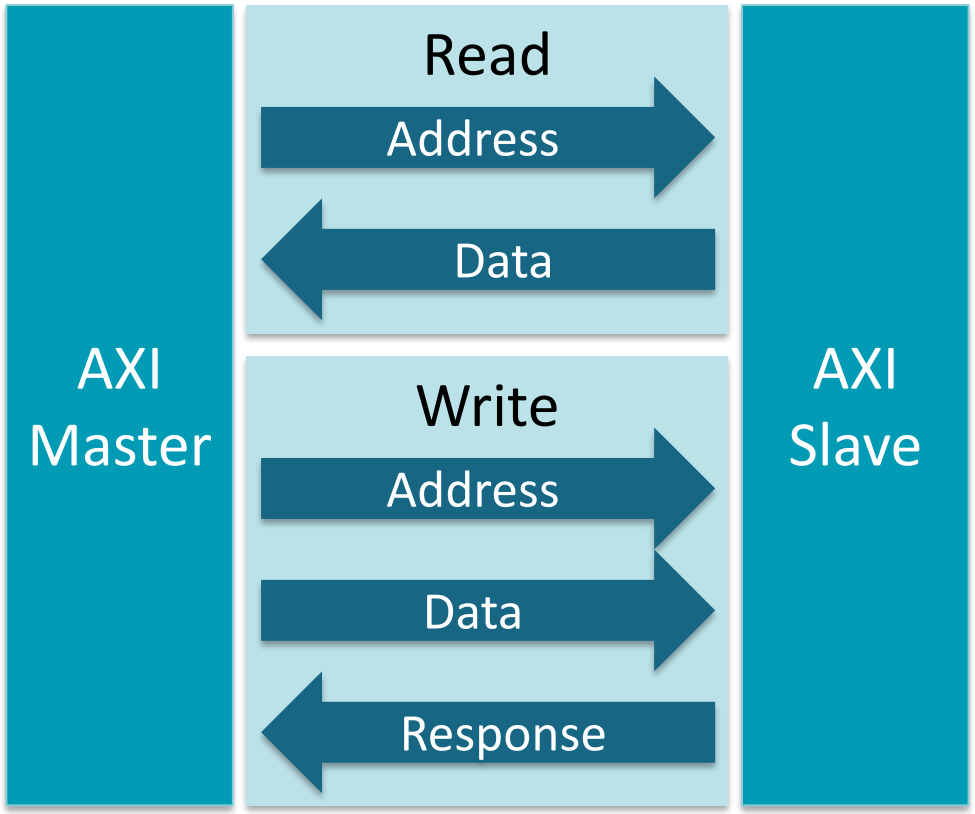
Background: Advanced eXtensible Interface (AXI)

AXI Transactions



AXI Interfaces

AXI Full	**AXI Stream**	**AXI Lite**
↓	↓	↓
memory-mapped data	data streaming	control register handling

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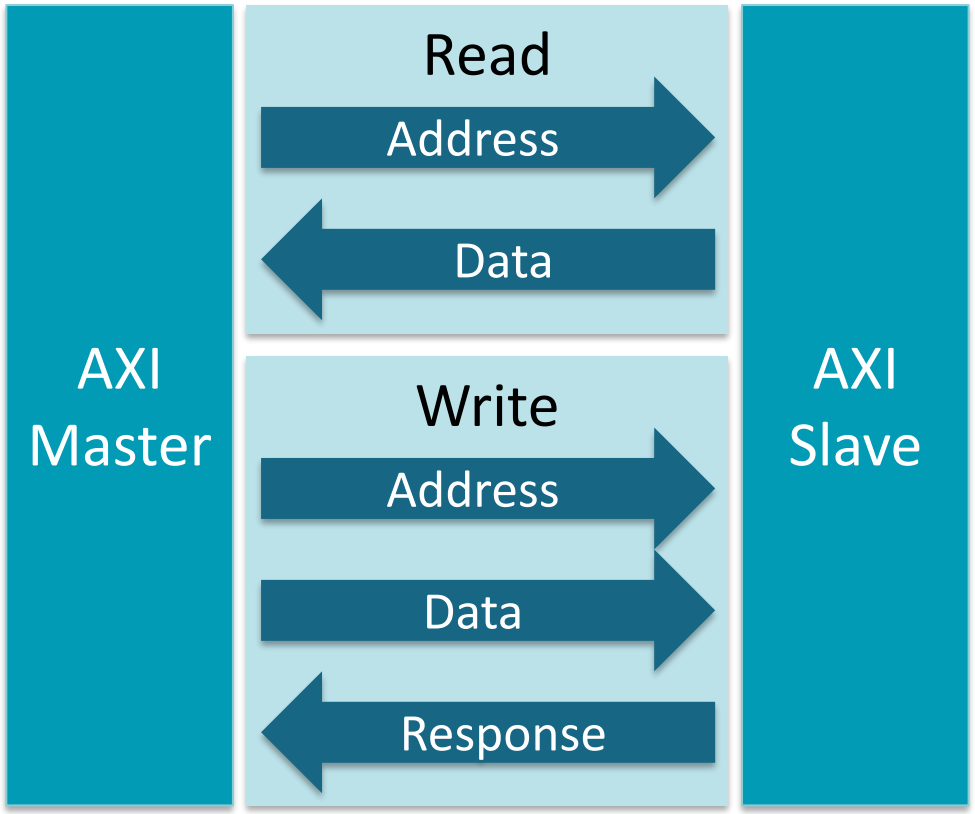
Background: Advanced eXtensible Interface (AXI)

AXI Transactions



AXI Interfaces

AXI Full	AXI Stream	AXI Lite
↓	↓	↓
memory-mapped data	data streaming	control register handling

flexible access

↓

burst-based and register-like access

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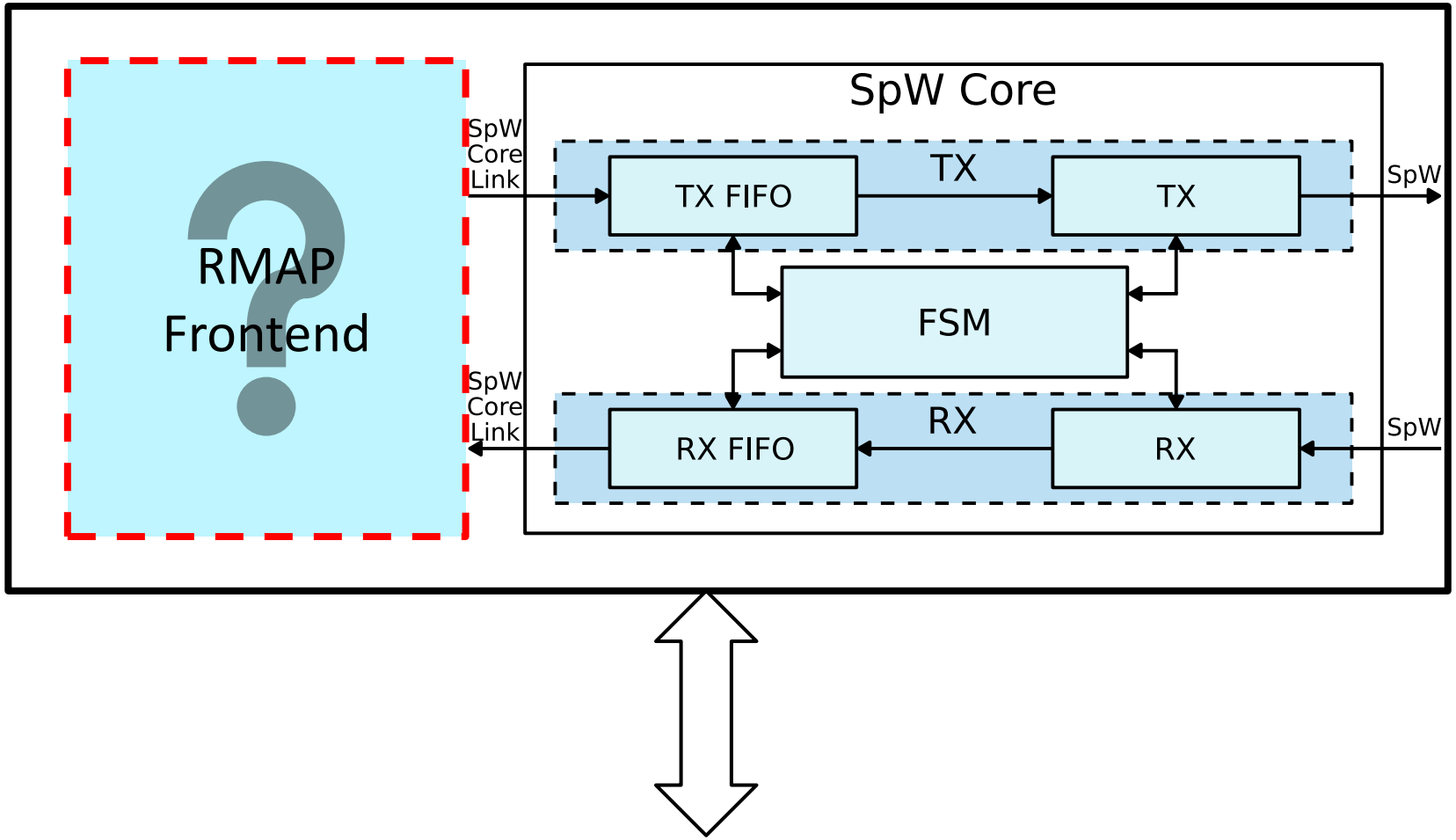
Motivation



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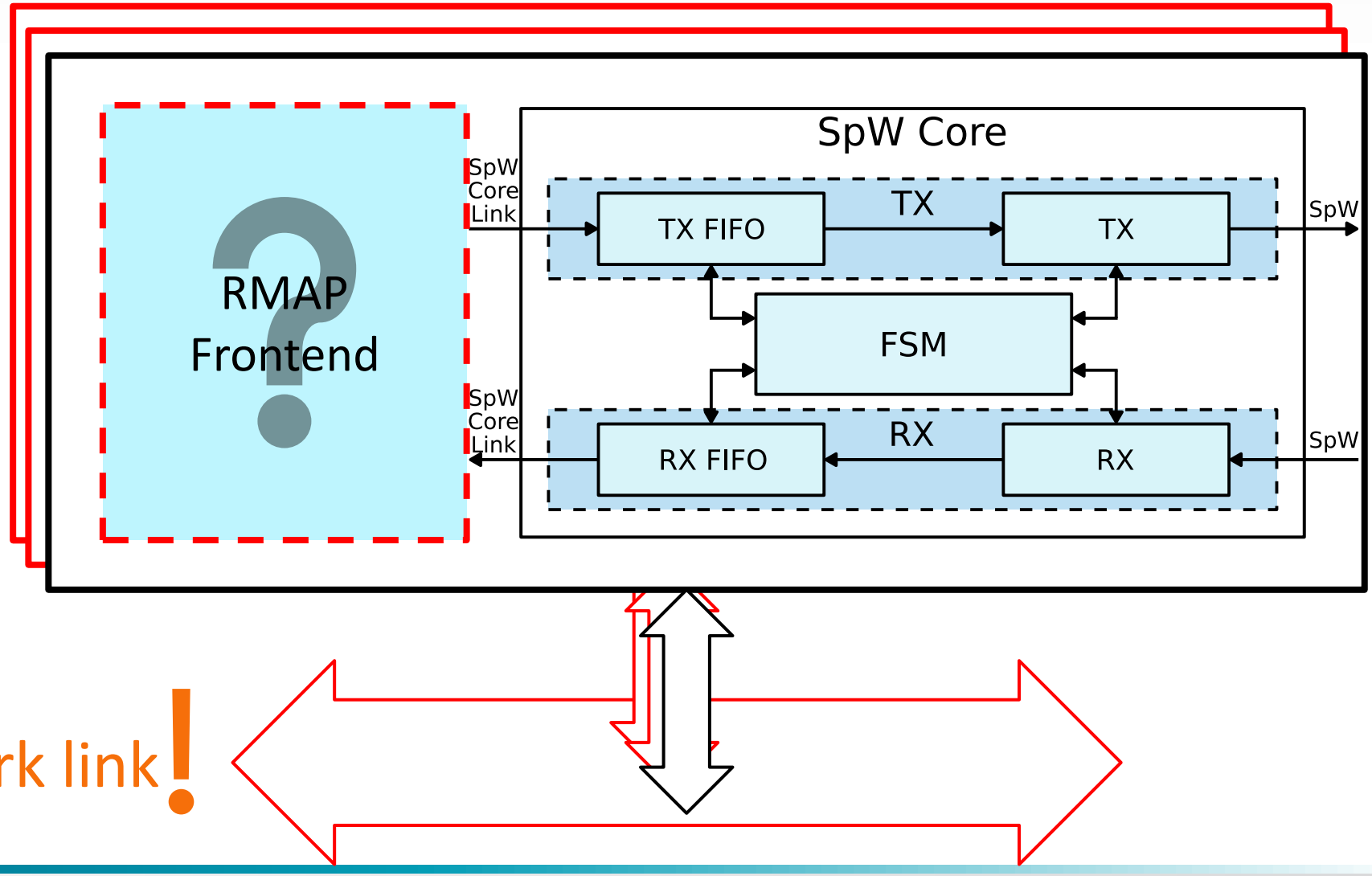
Motivation



network link!

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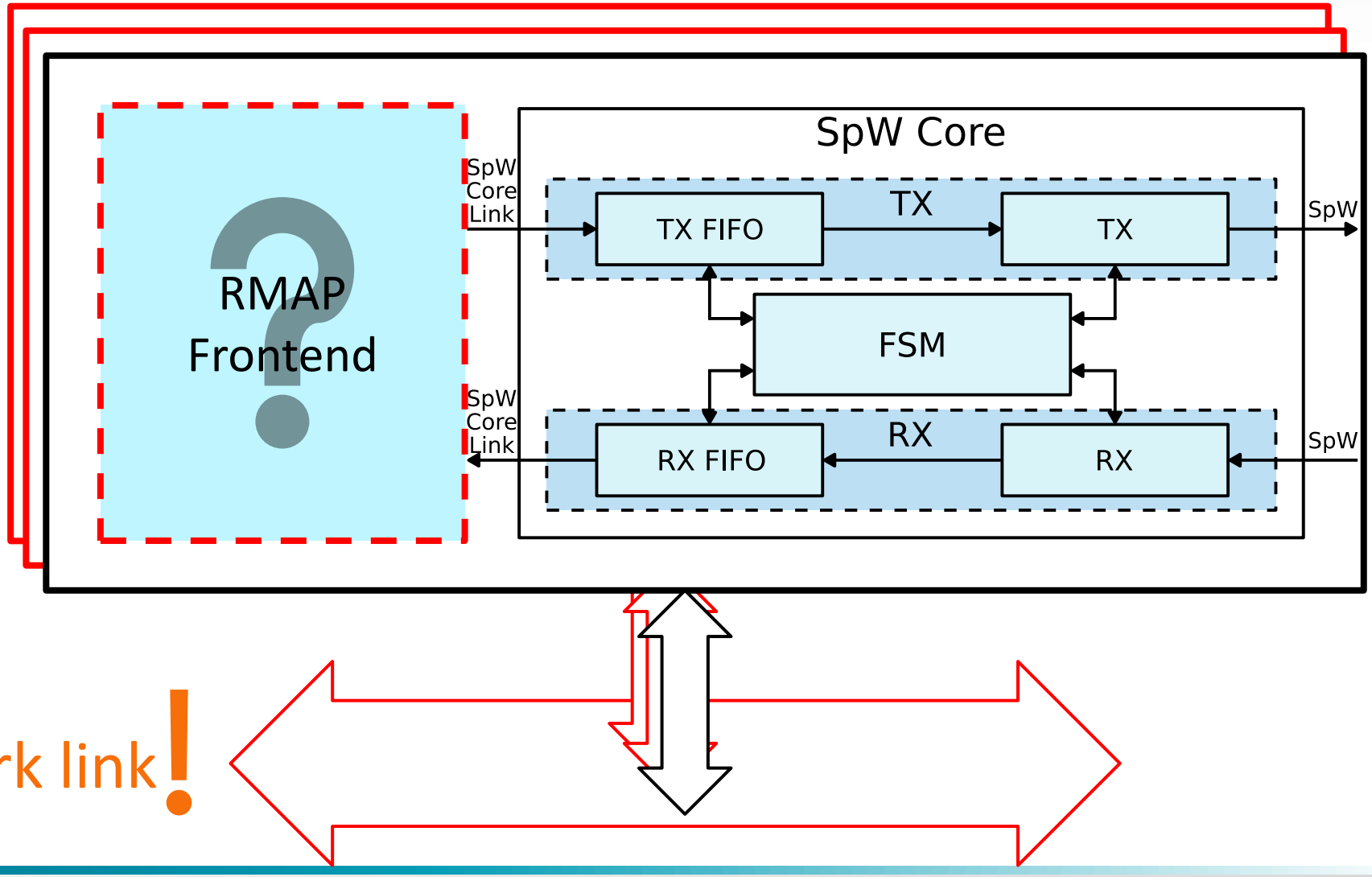
Motivation

customization!



network link!

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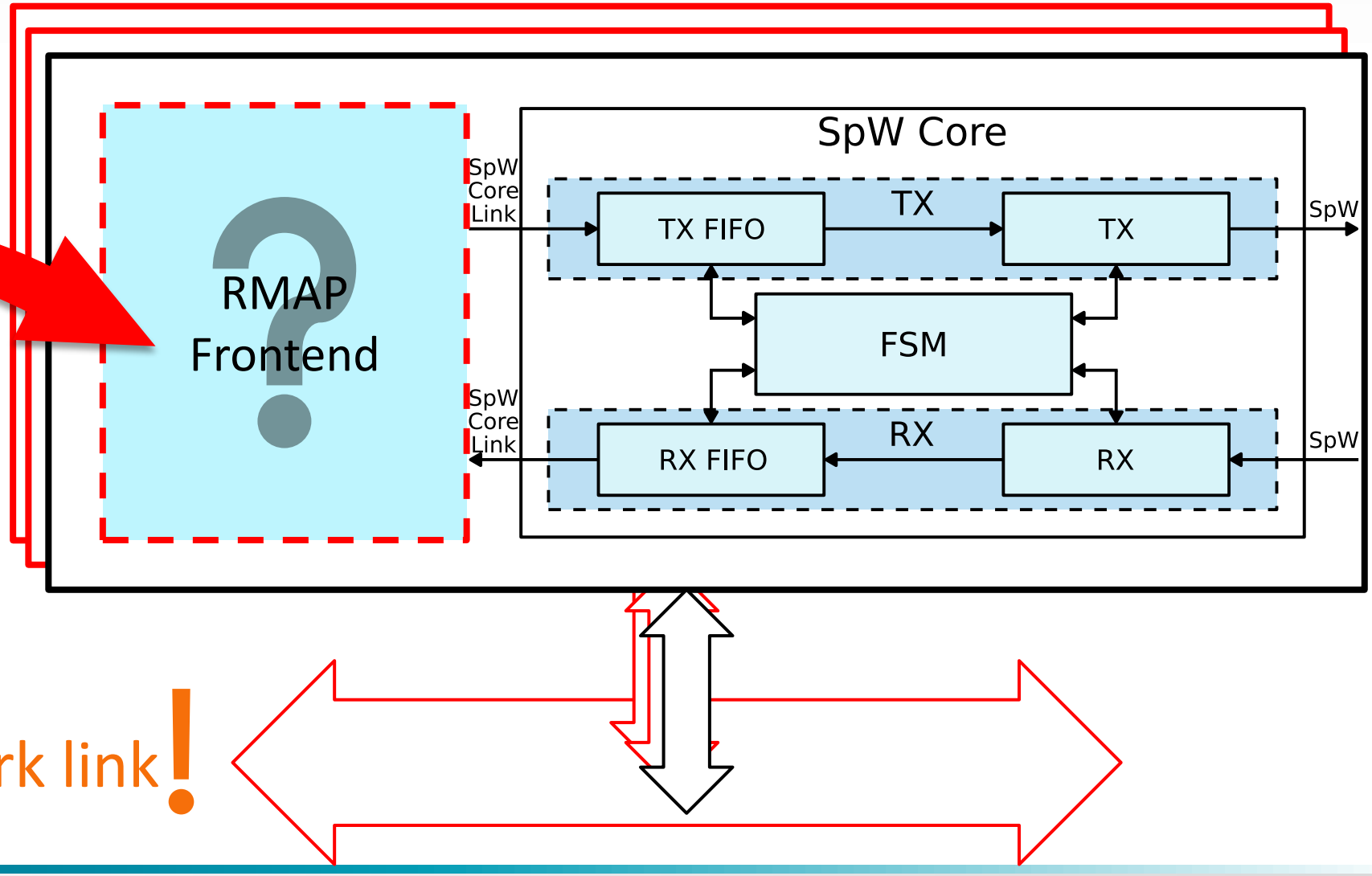
Motivation

design effort !

customization !

network link !



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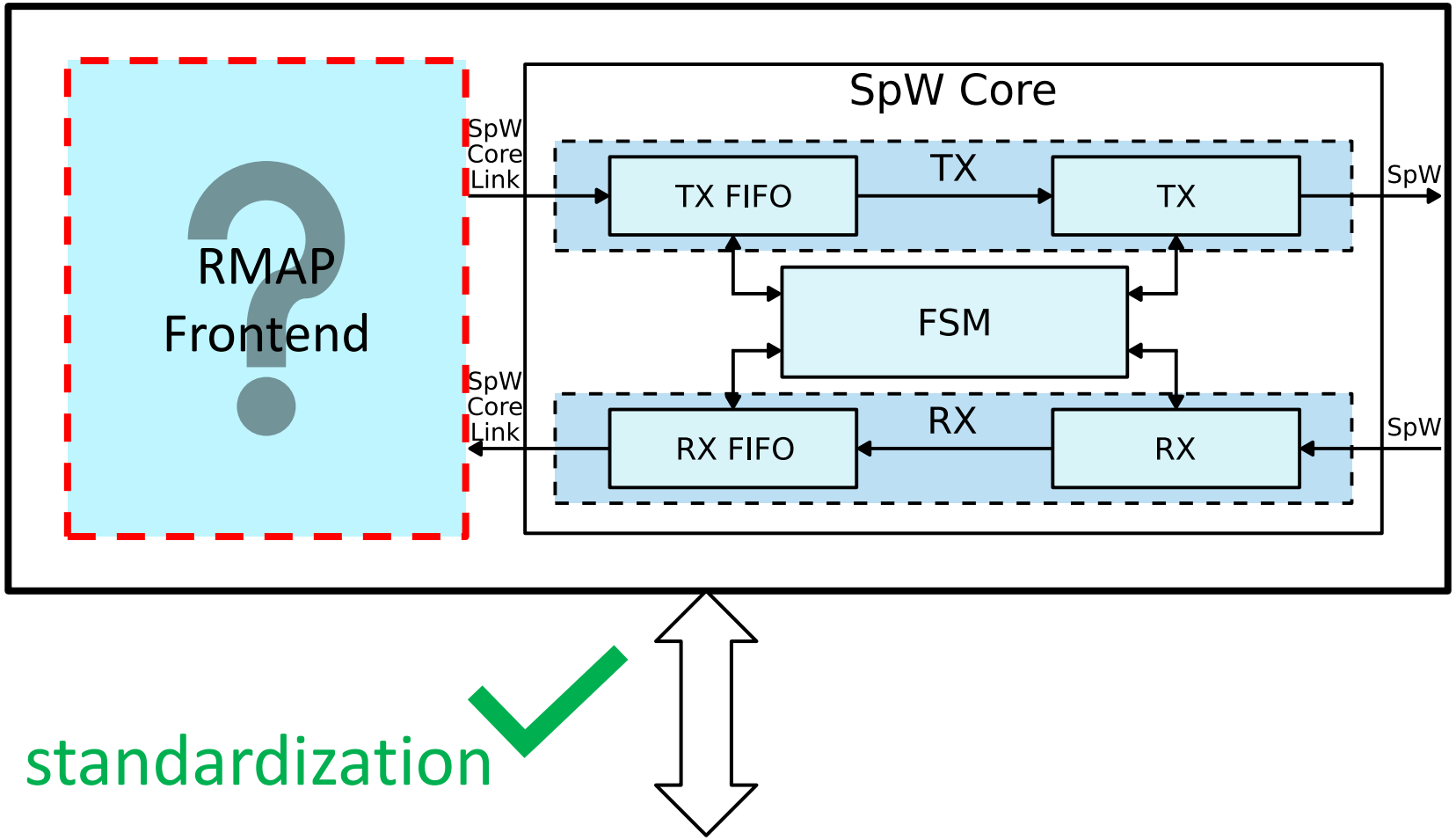

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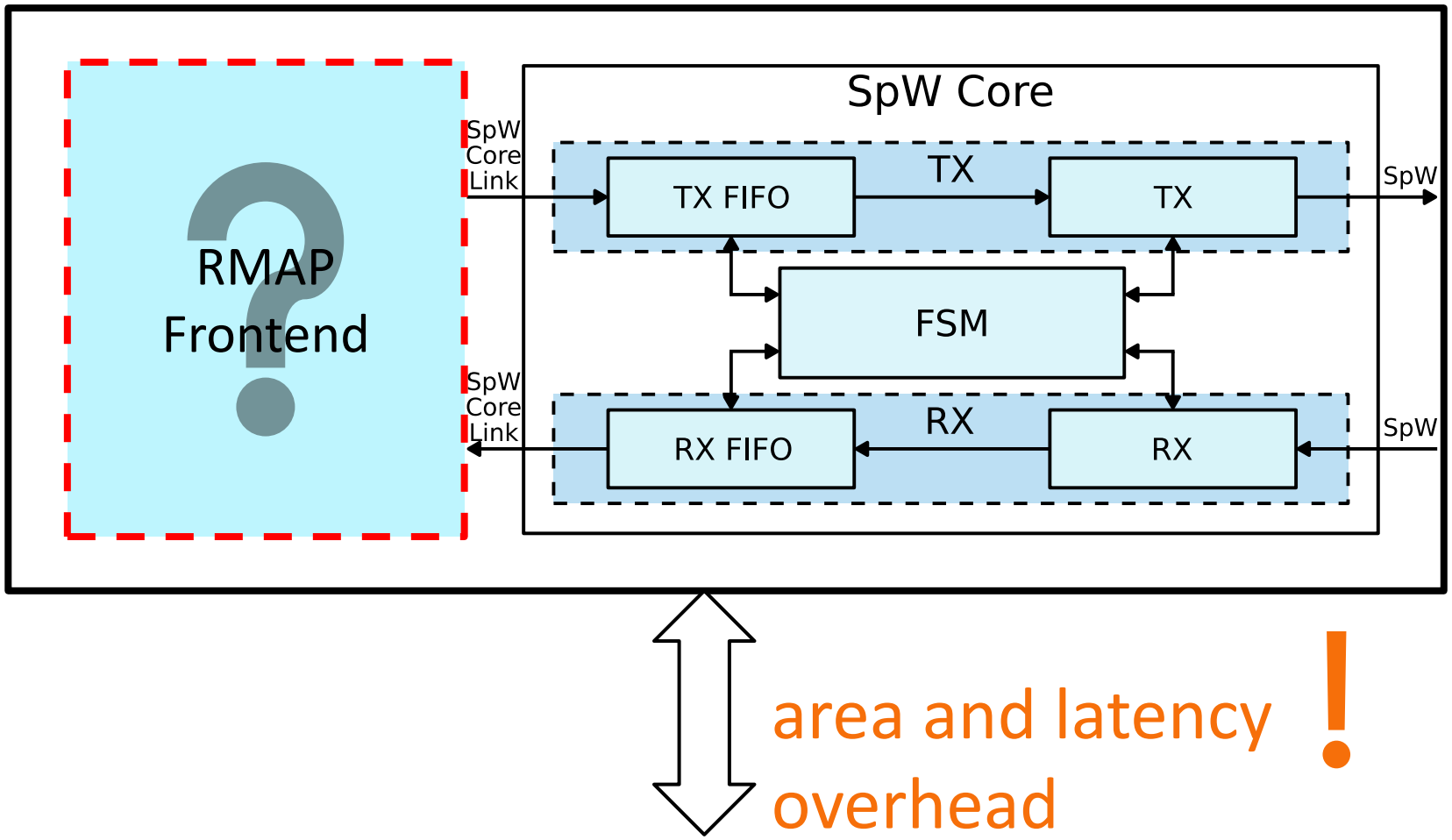
Motivation

Reading from Memory

Field	No. of bytes
Dest. Address	1
Protocol ID	1
Packet Type	1
Destination Key	1
Source Address	1
Transaction ID	2
Ext. Read Address	1
Read Address	4
Data Length	3
Header CRC	1
TOT.	**16**



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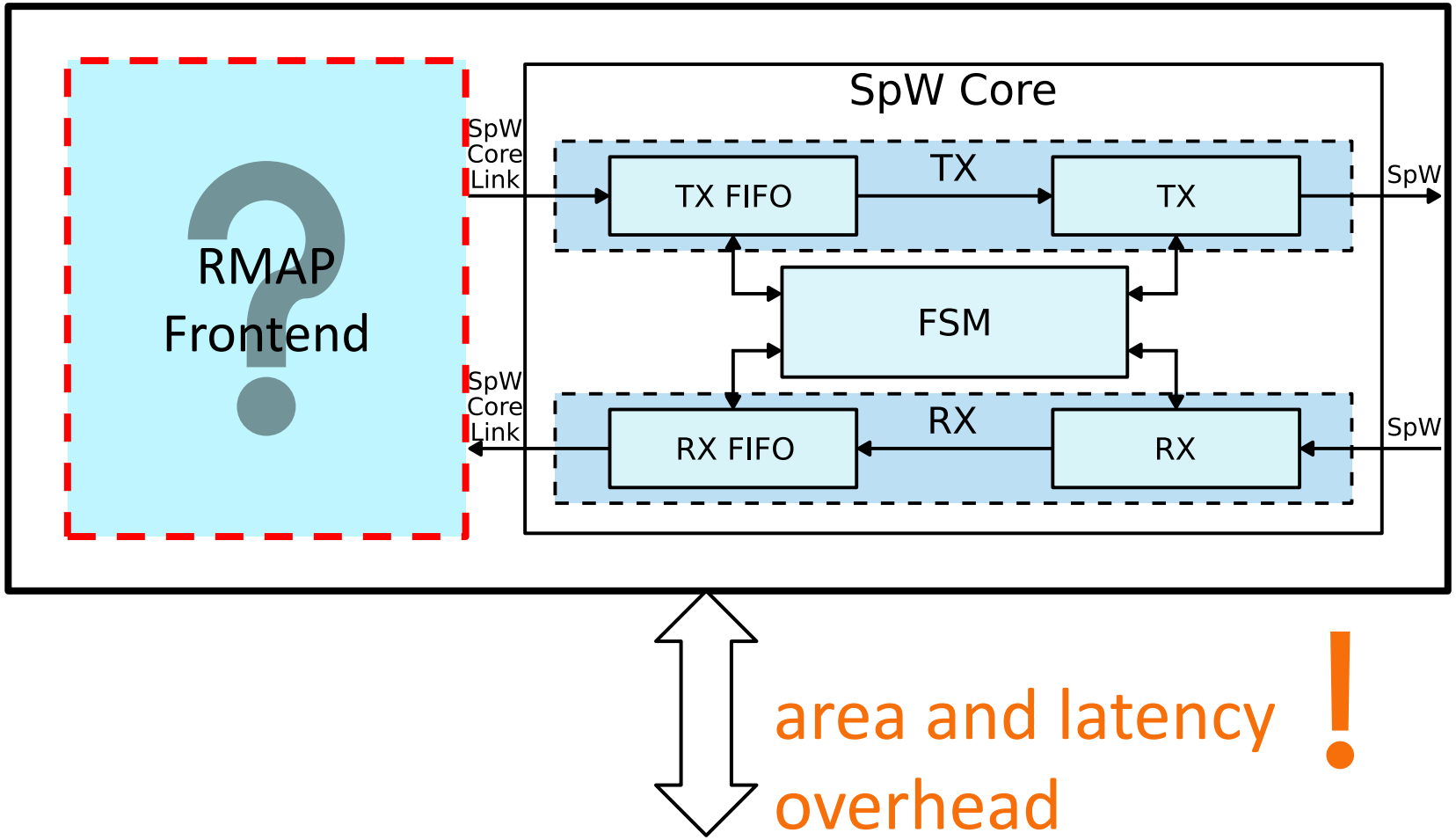
Motivation

Reading from Memory

Field	No. of bytes
Dest. Address	
Protocol ID	
Packet Type	
Destination Key	
Source Address	
Transaction ID	
Ext. Read Address	
Read Address	
Data Length	
Header CRC	
TOT.	

Writing to Memory

Field	No. of bytes
Dest. Address	1
Protocol ID	1
Packet Type	1
Destination Key	1
Source Address	1
Transaction ID	2
Ext. Write Address	1
Write Address	4
Data Length	3
Header CRC	1
Data CRC	1
TOT.	**17**



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Motivation

Reading from Memory

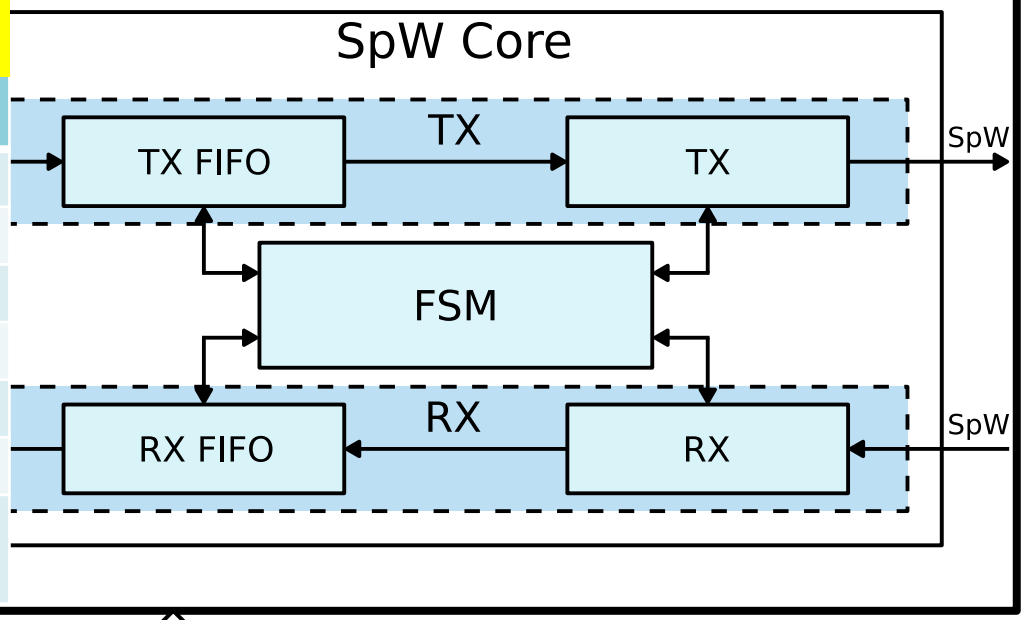
Field
Dest. Address
Protocol ID
Packet Type
Destination Key
Source Address
Transaction ID
Ext. Read Address
Read Address
Data Length
Header CRC
TOT.

Writing to Memory

Field	No. of bytes
Dest. Address	1
Protocol ID	1
Packet Type	1
Destination Key	1
Source Address	1
Transaction ID	2
Ext. Write Address	1
Write Address	4
Data Length	3
Header CRC	1
Data CRC	1
TOT.	**17**

AXI-SpW-AXI Bridge

Field	No. of bytes
Packet Type	1
Read/Write Address	4
Data Size, Burst Type	1
Data Length	1
End of Packet	1
PacketCRC	1
TOT.	**9**



area and latency overhead !

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Motivation

Reading from Memory

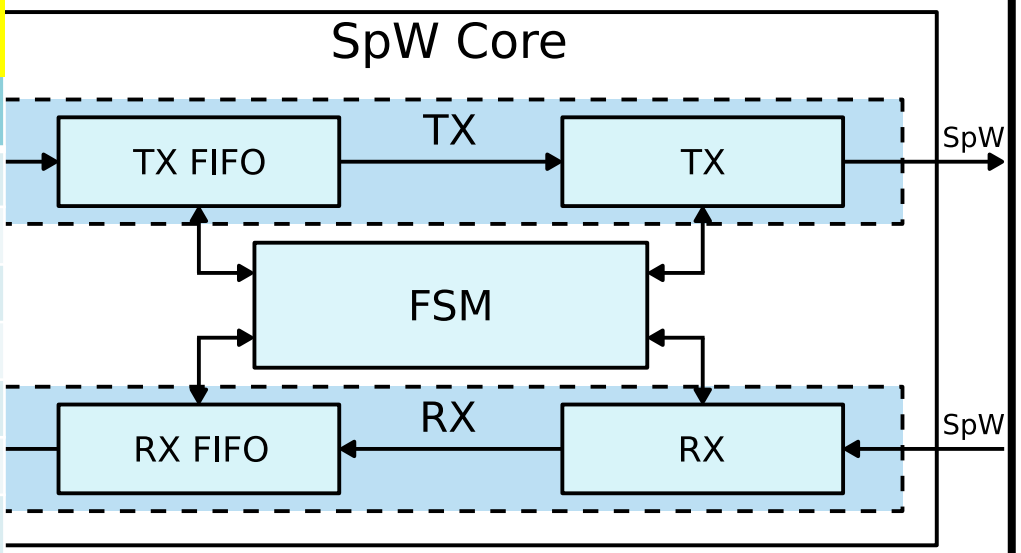
Field	No. of bytes
Dest. Address	
Protocol ID	
Packet Type	
Destination Key	
Source Address	
Transaction ID	
Ext. Read Address	
Read Address	
Data Length	
Header CRC	
TOT.	

Writing to Memory

Field	No. of bytes
Dest. Address	1
Protocol ID	1
Packet Type	1
Destination Key	1
Source Address	1
Transaction ID	2
Ext. Write Address	1
Write Address	4
Data Length	3
Header CRC	1
Data CRC	1
TOT.	**17**

AXI-SpW-AXI Bridge

Field	No. of bytes
Packet Type	1
Read/Write Address	4
Data Size, Burst Type	1
Data Length	1
End of Packet	1
PacketCRC	1
TOT.	**9**



availability !

AXI

area and latency overhead !

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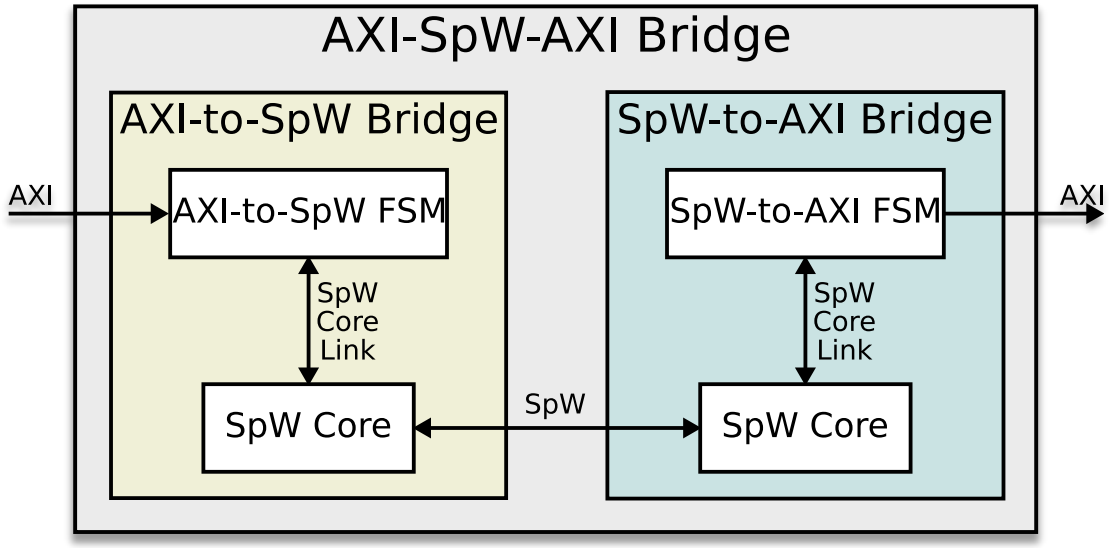

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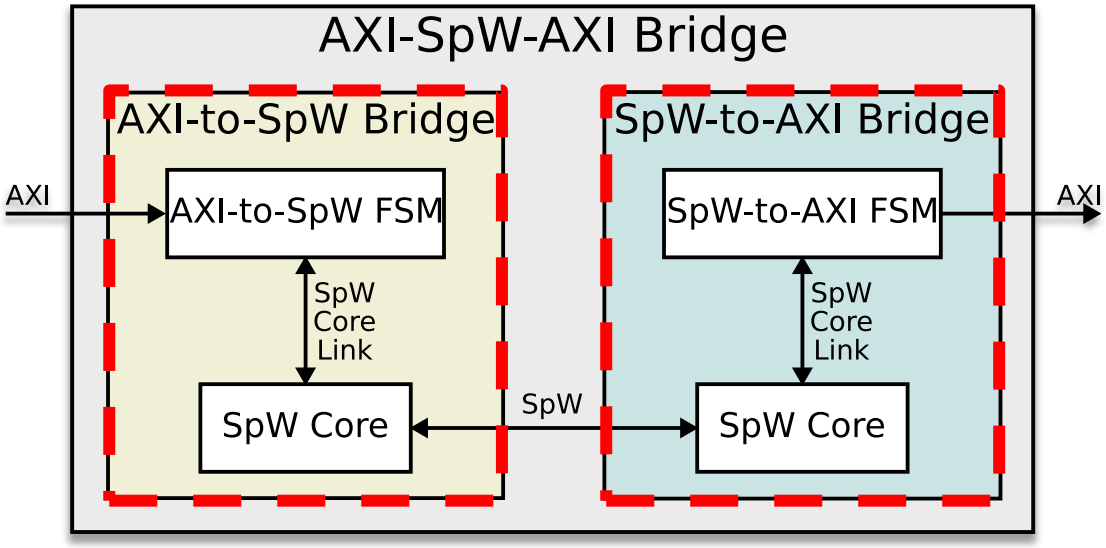

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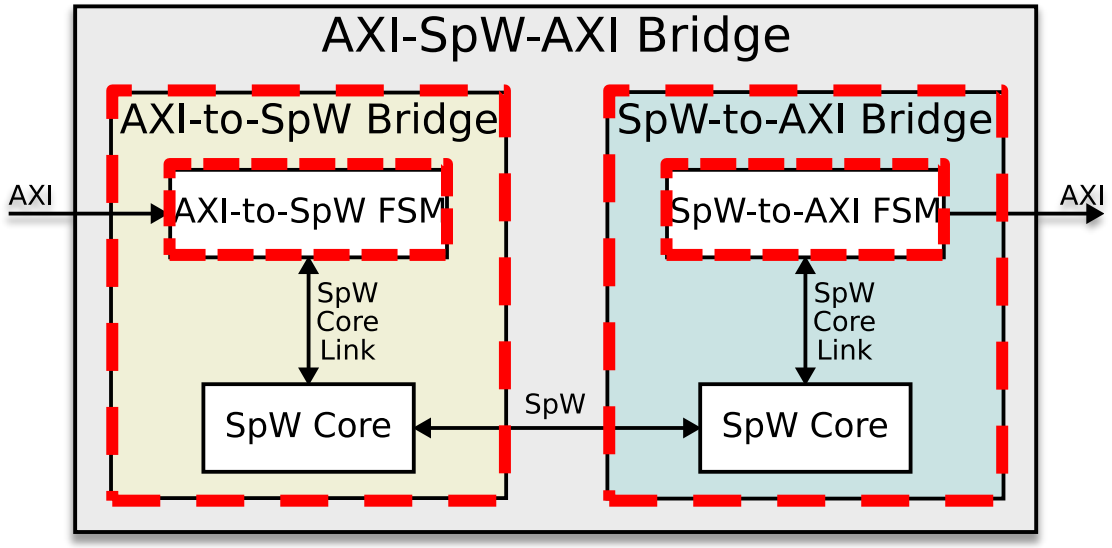

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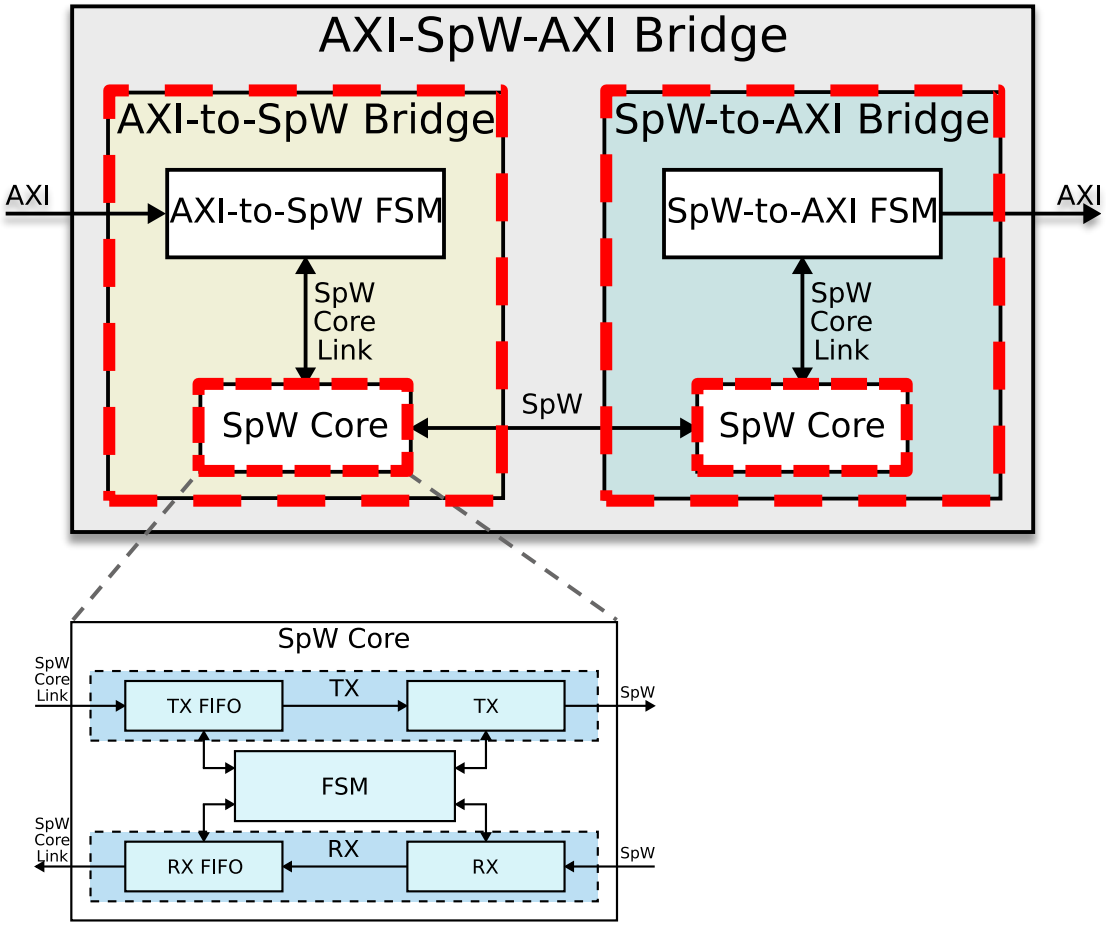

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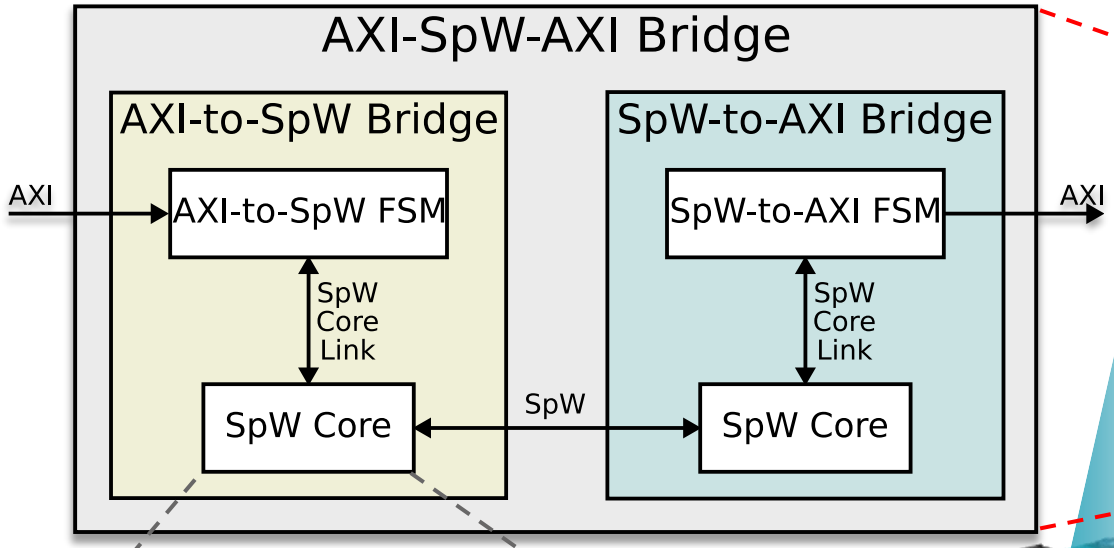

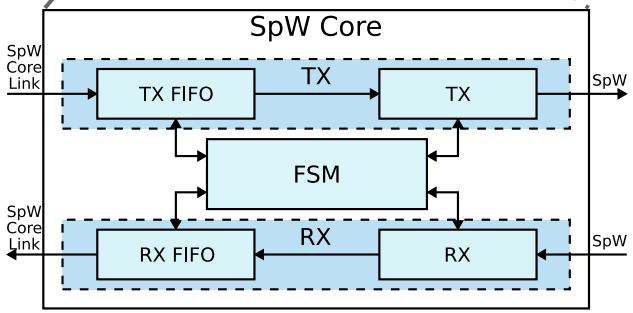

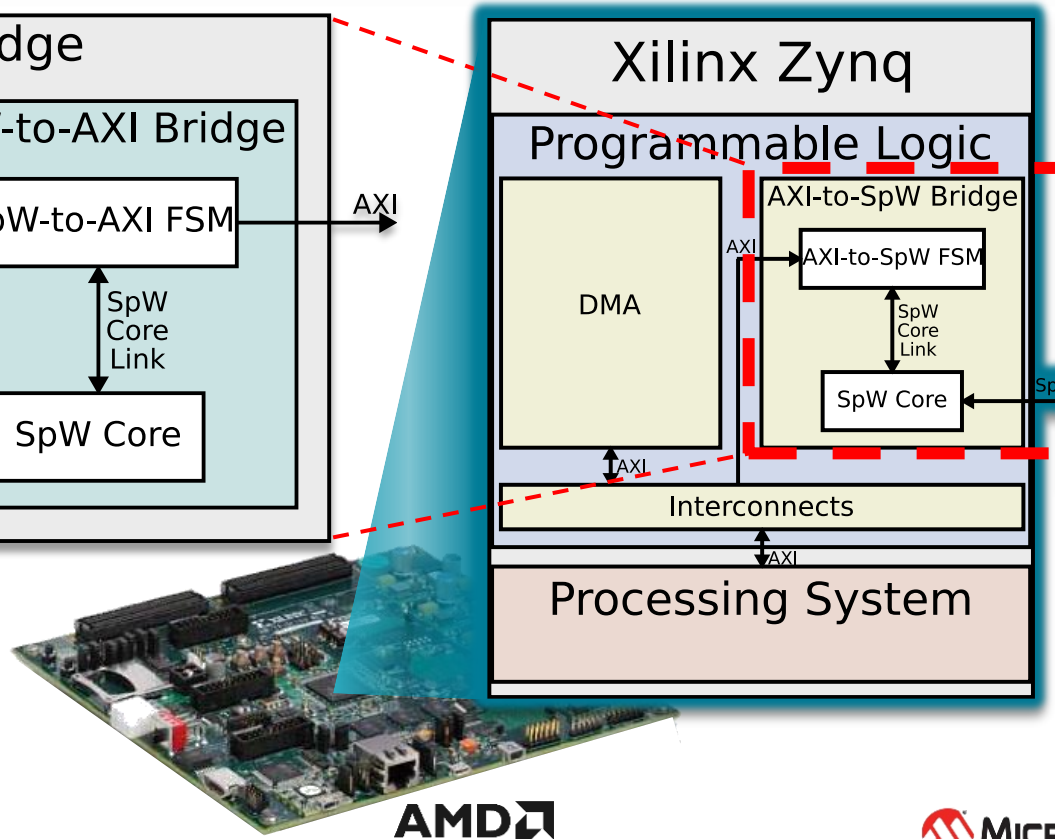

AMD XILINX

MICROCHIP

Microsemi

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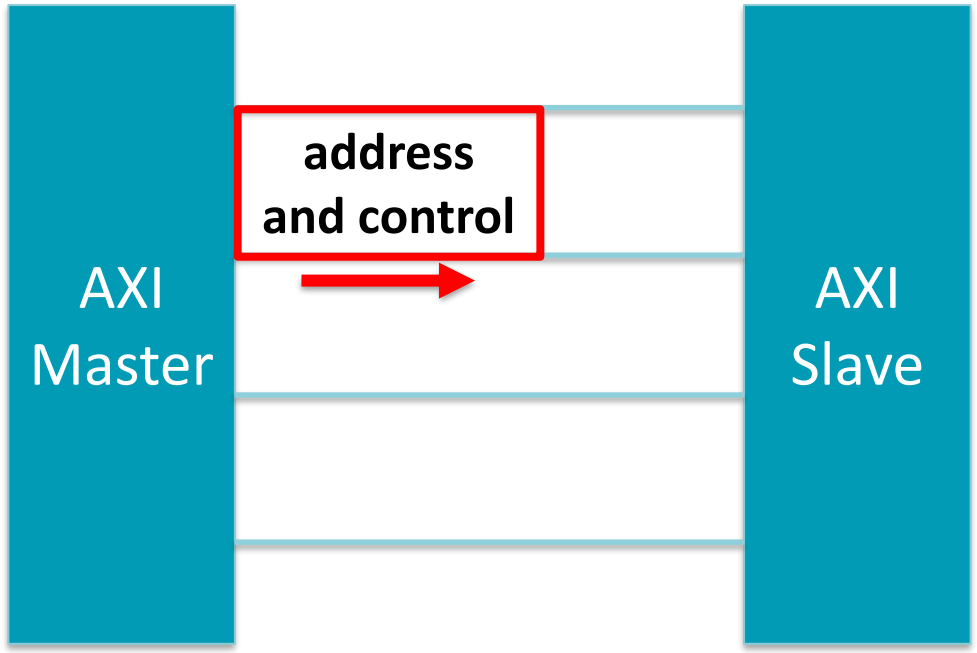
Read Transaction: Address Channel

AXI Transaction



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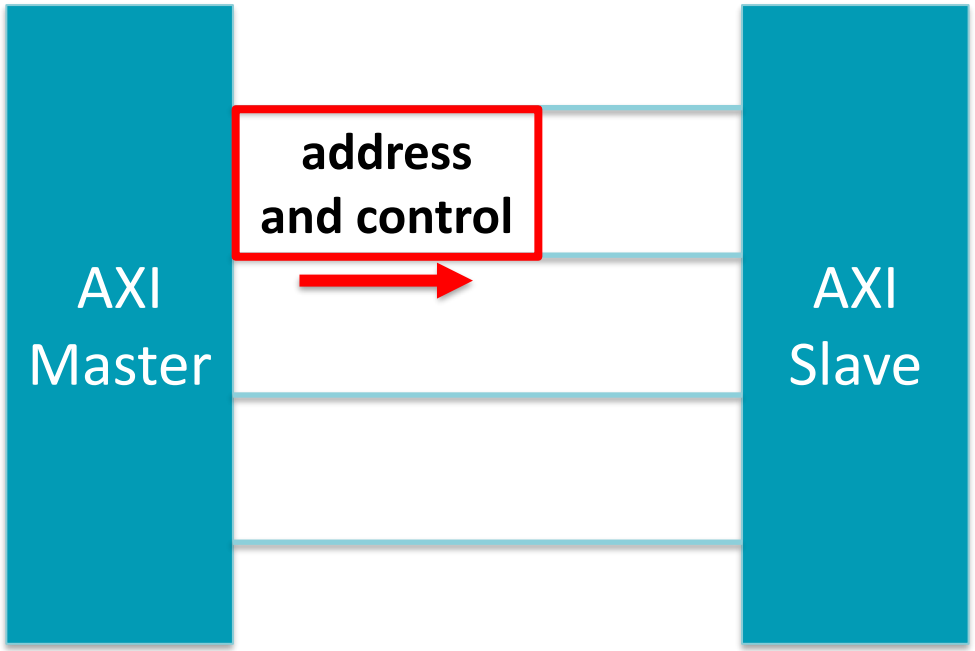
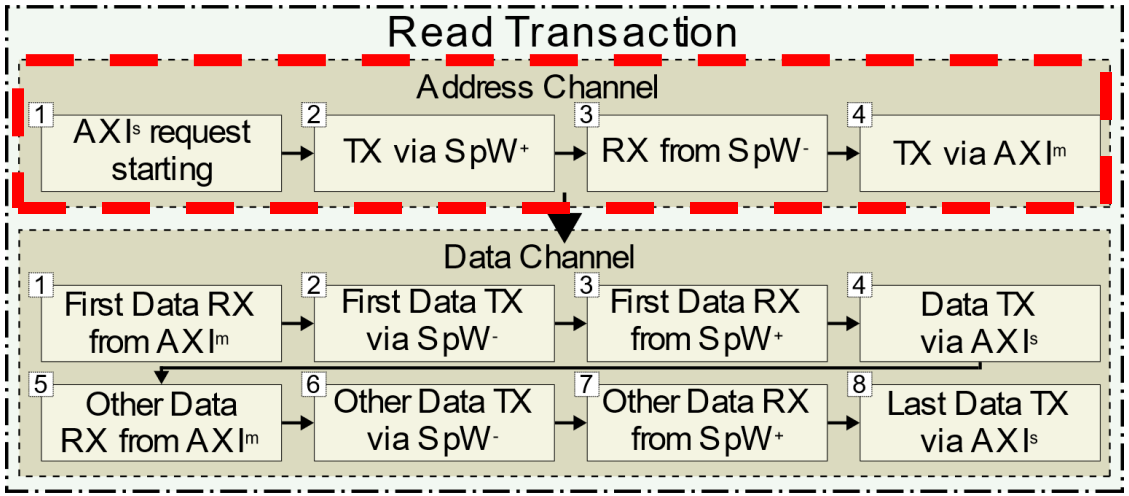
Read Transaction: Address Channel

AXI Transaction



AXI-SpW-AXI Transaction



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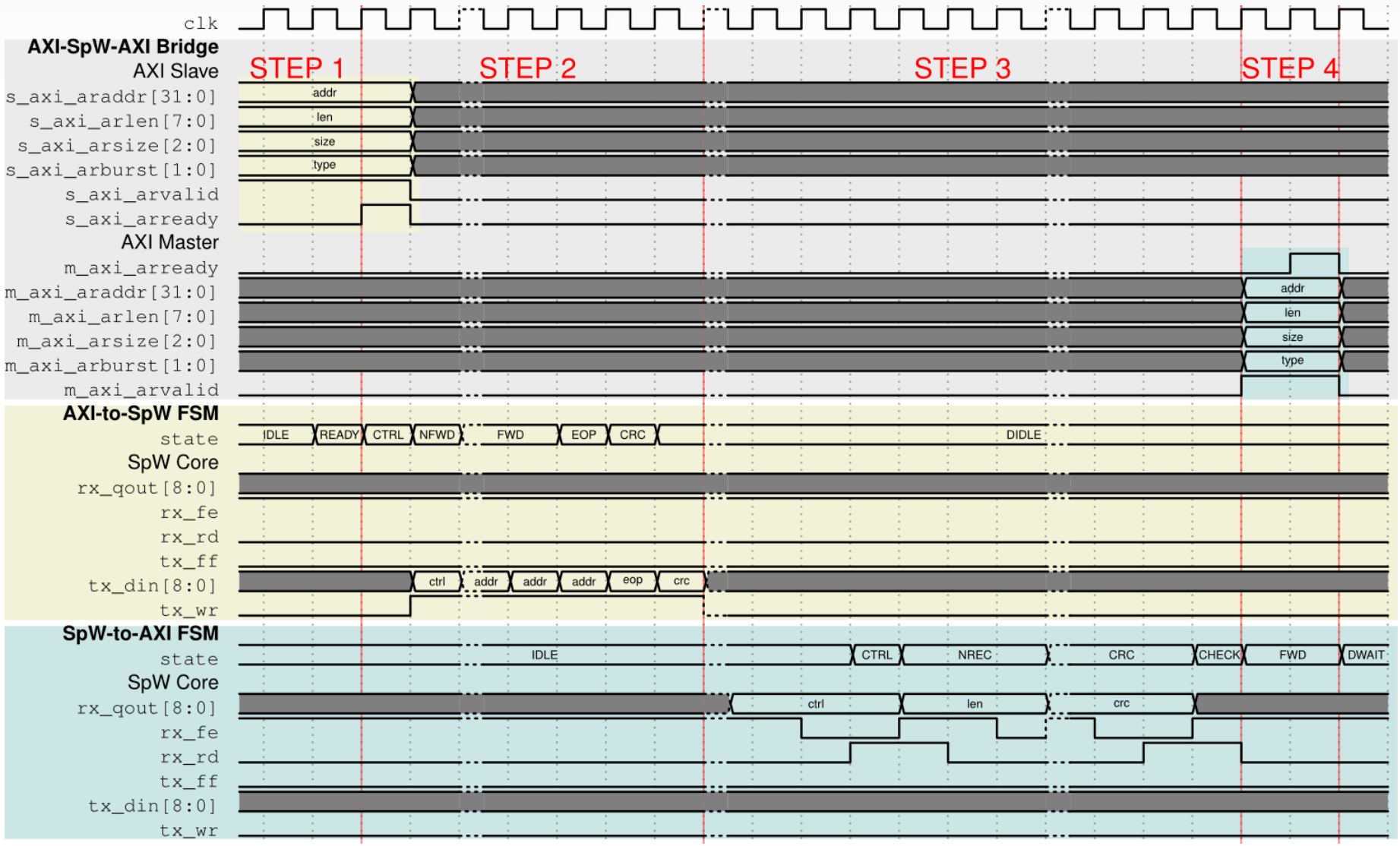
Read Transaction: Address Channel

AXI^{s} request starting

TX via SpW^{+}

RX from SpW^{-}

TX via AXI^{m}



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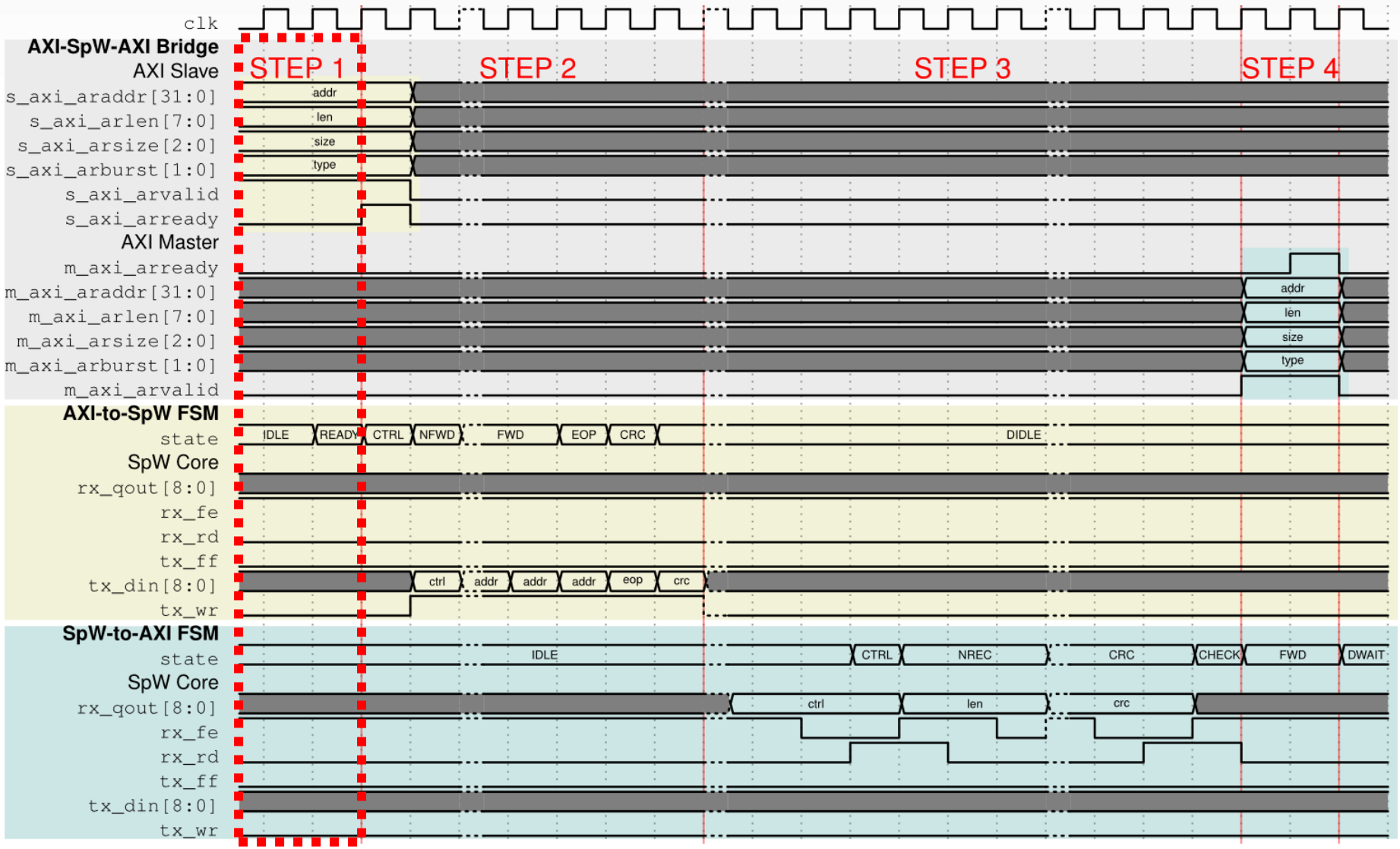
Read Transaction: Address Channel

AXI^{s} request starting

TX via SpW^{+}

RX from SpW^{-}

TX via AXI^{m}



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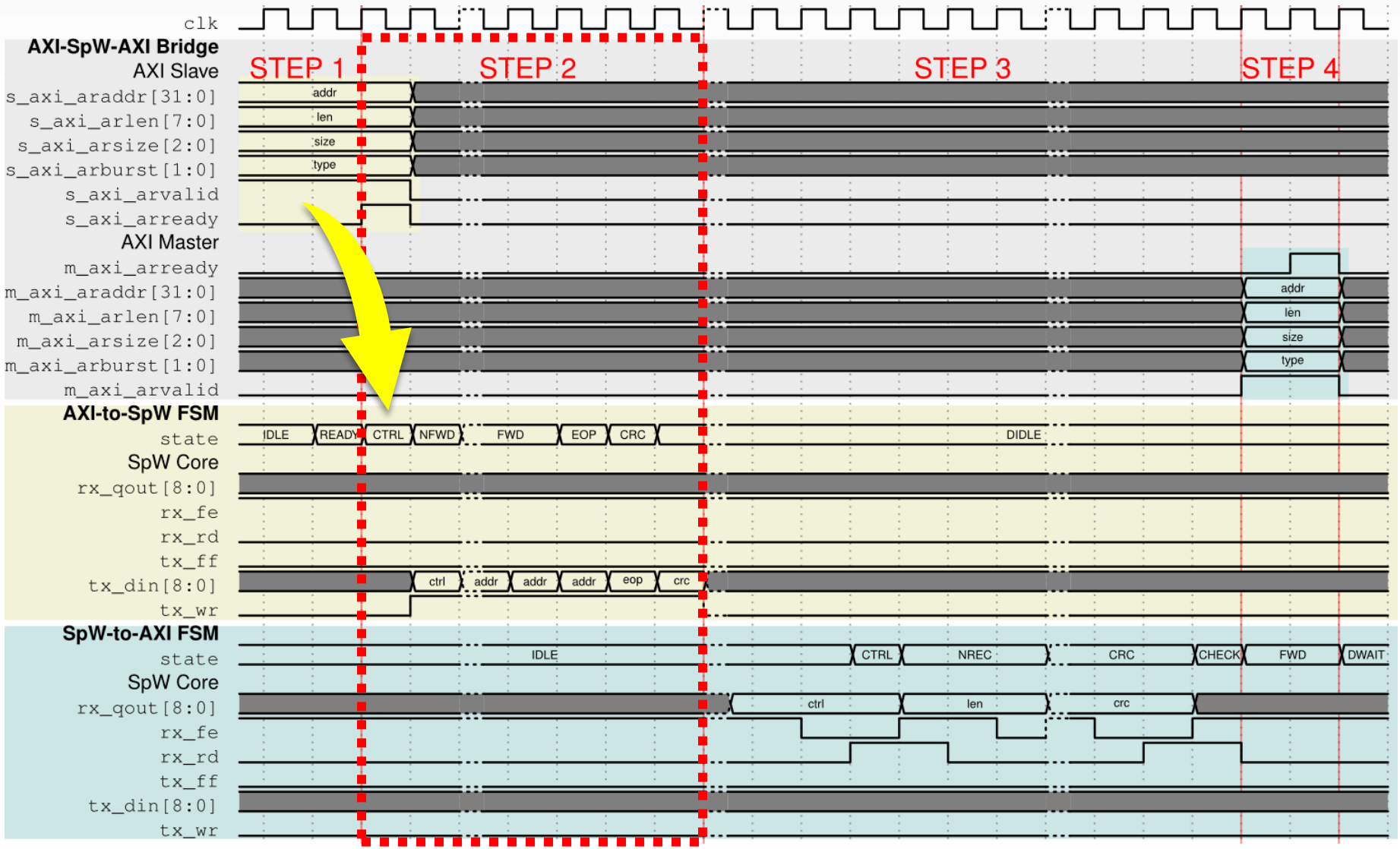
Read Transaction: Address Channel

AXI^{s} request starting

TX via SpW^{+}

RX from SpW^{-}

TX via AXI^{m}



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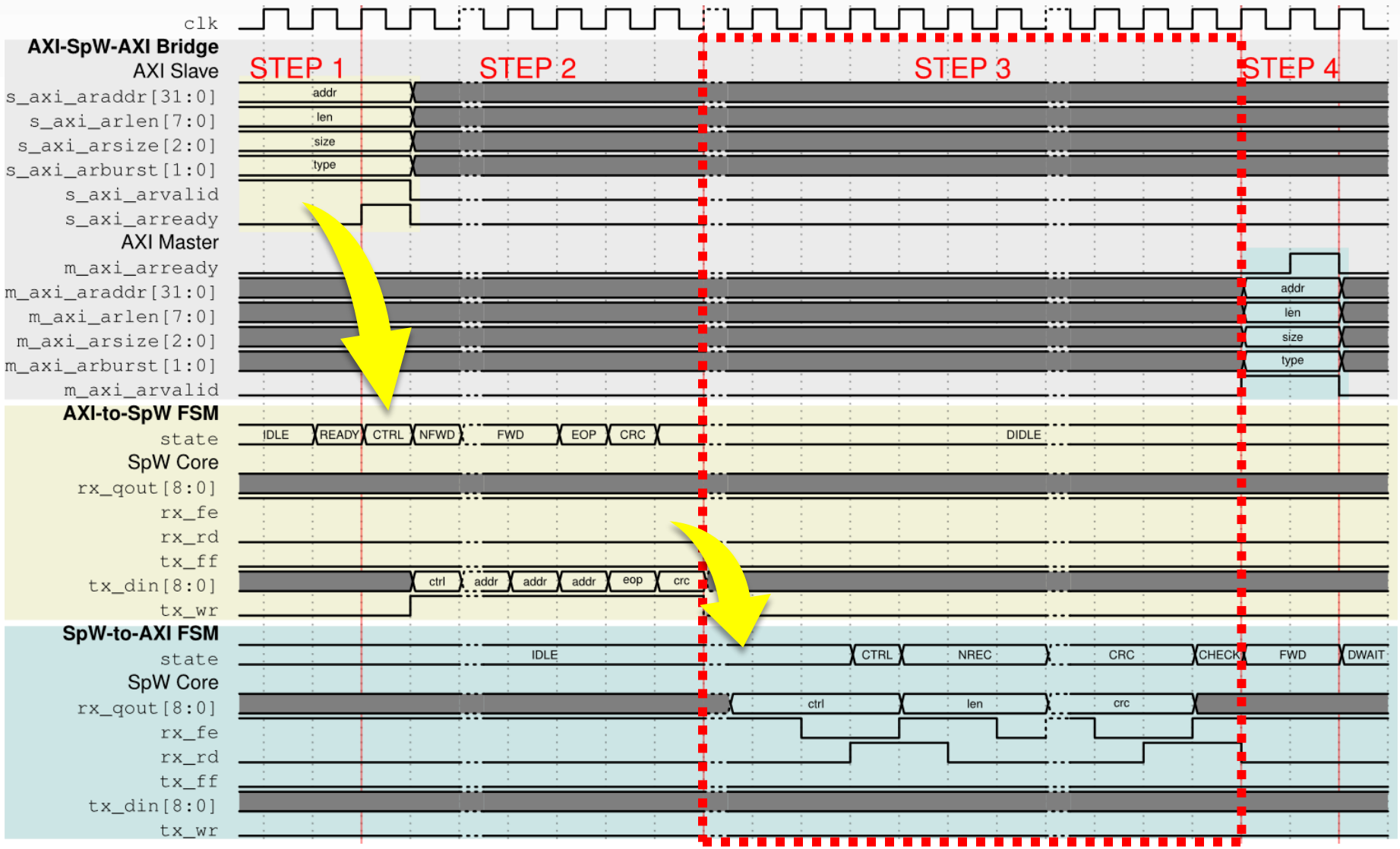
Read Transaction: Address Channel

AXI^{s} request starting

TX via SpW^{+}

RX from SpW^{-}

TX via AXI^{m}



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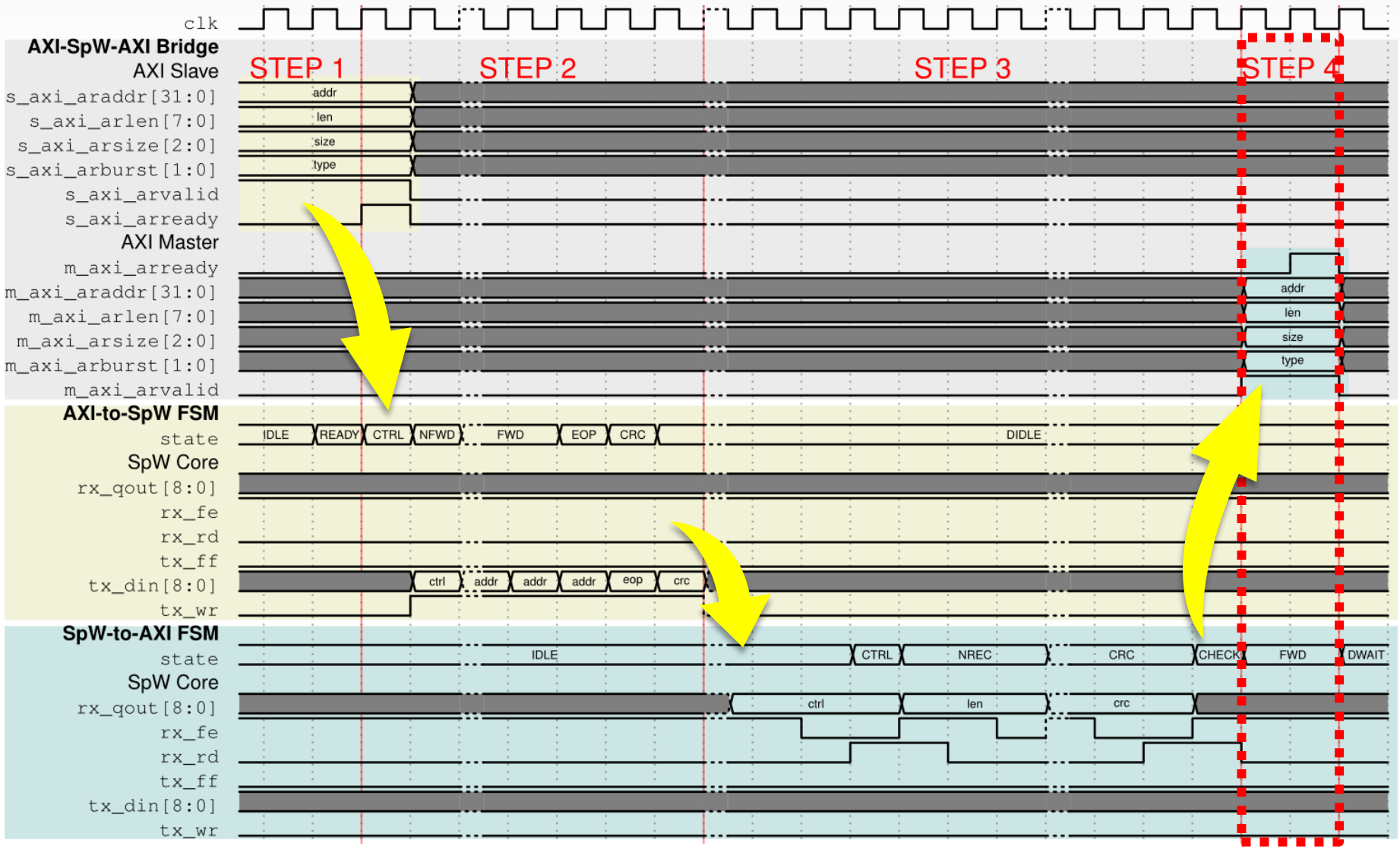
Read Transaction: Address Channel

AXI^{s} request starting

TX via SpW^{+}

RX from SpW^{-}

TX via AXI^{m}



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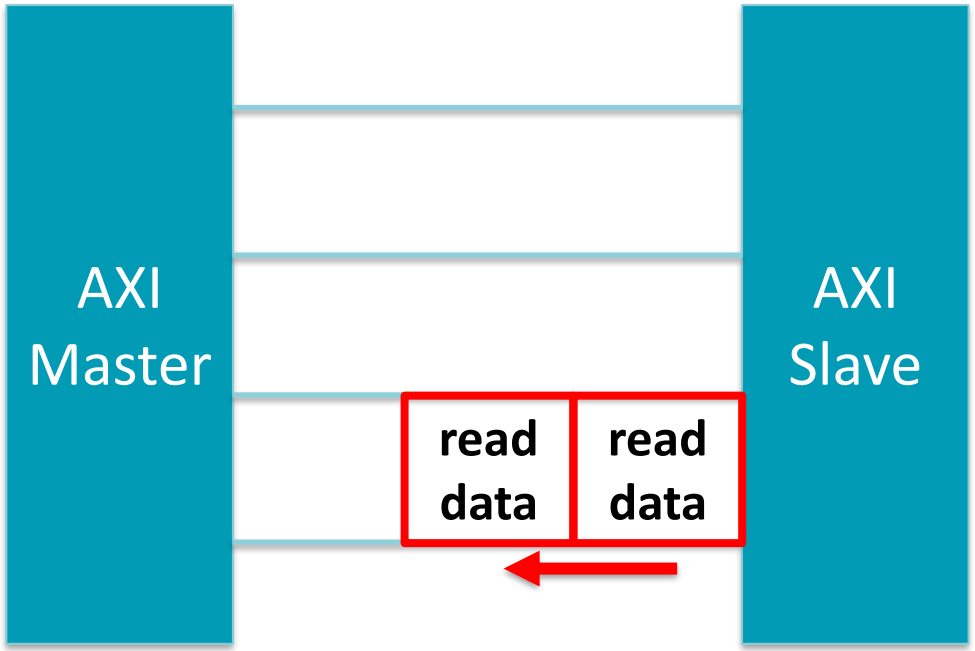
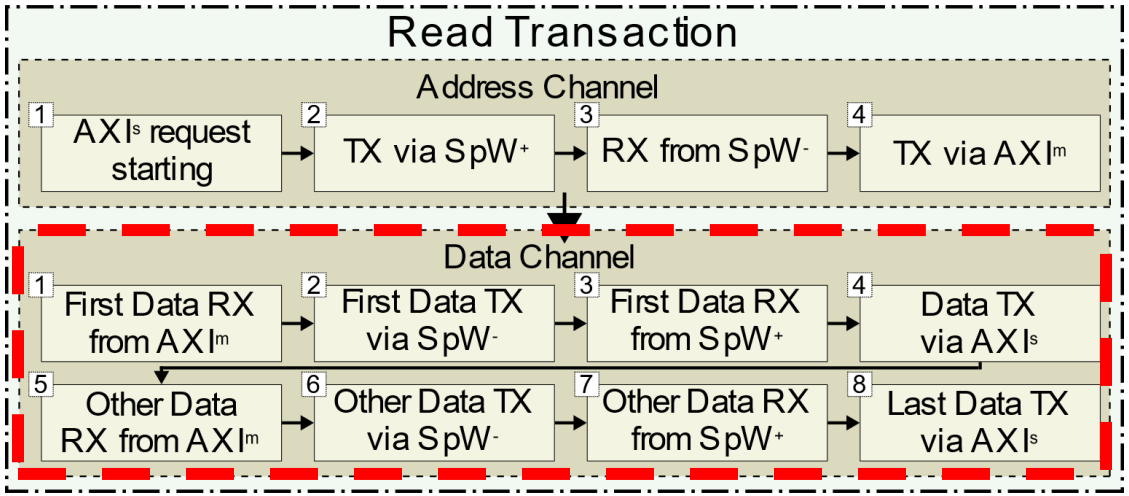
Read Transaction: Data Channel

AXI Transaction



AXI-SpW-AXI Transaction



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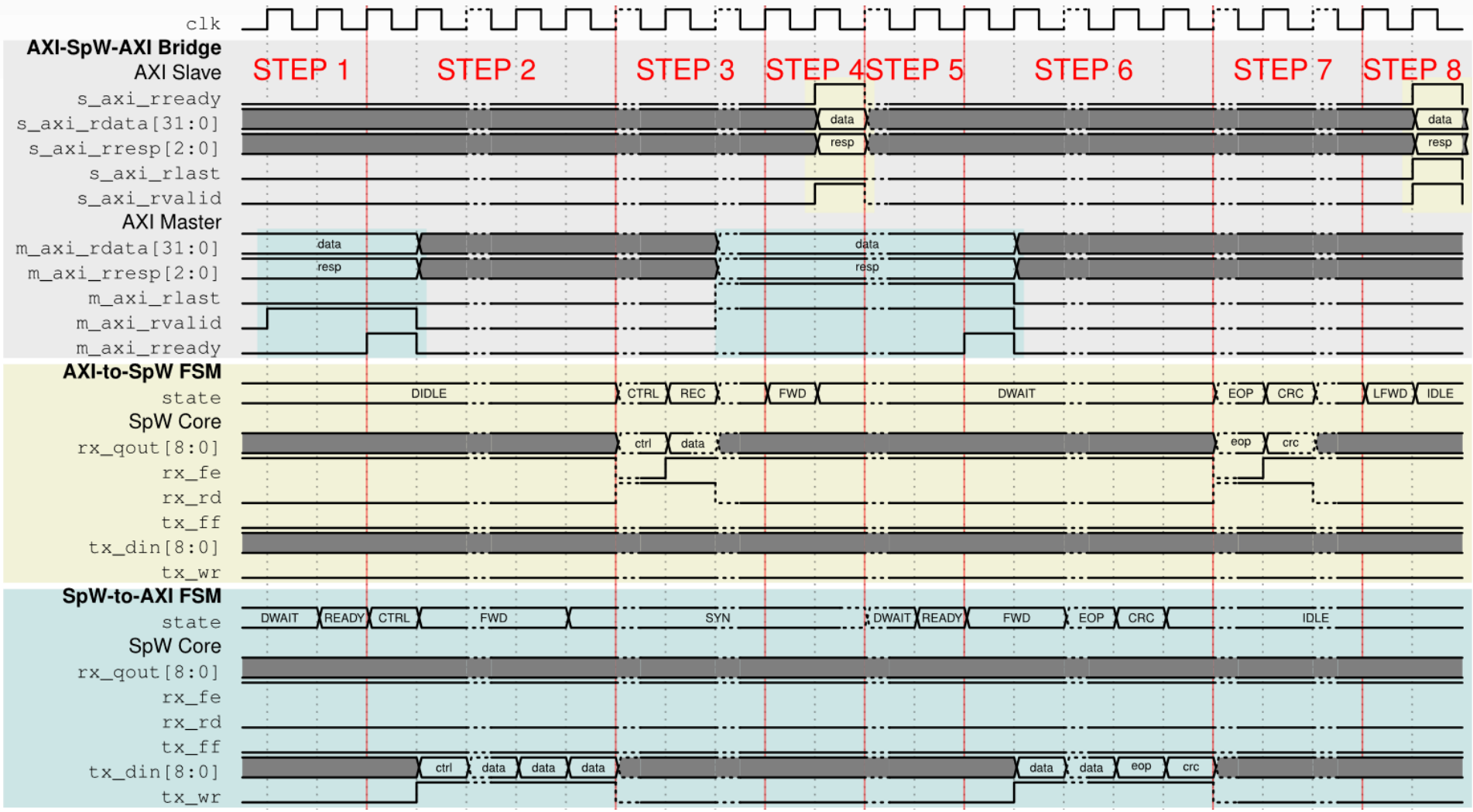
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- Data TX via AXI^{s}
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- Other Data RX via SpW^{+}
- Last Data TX via AXI^{s}



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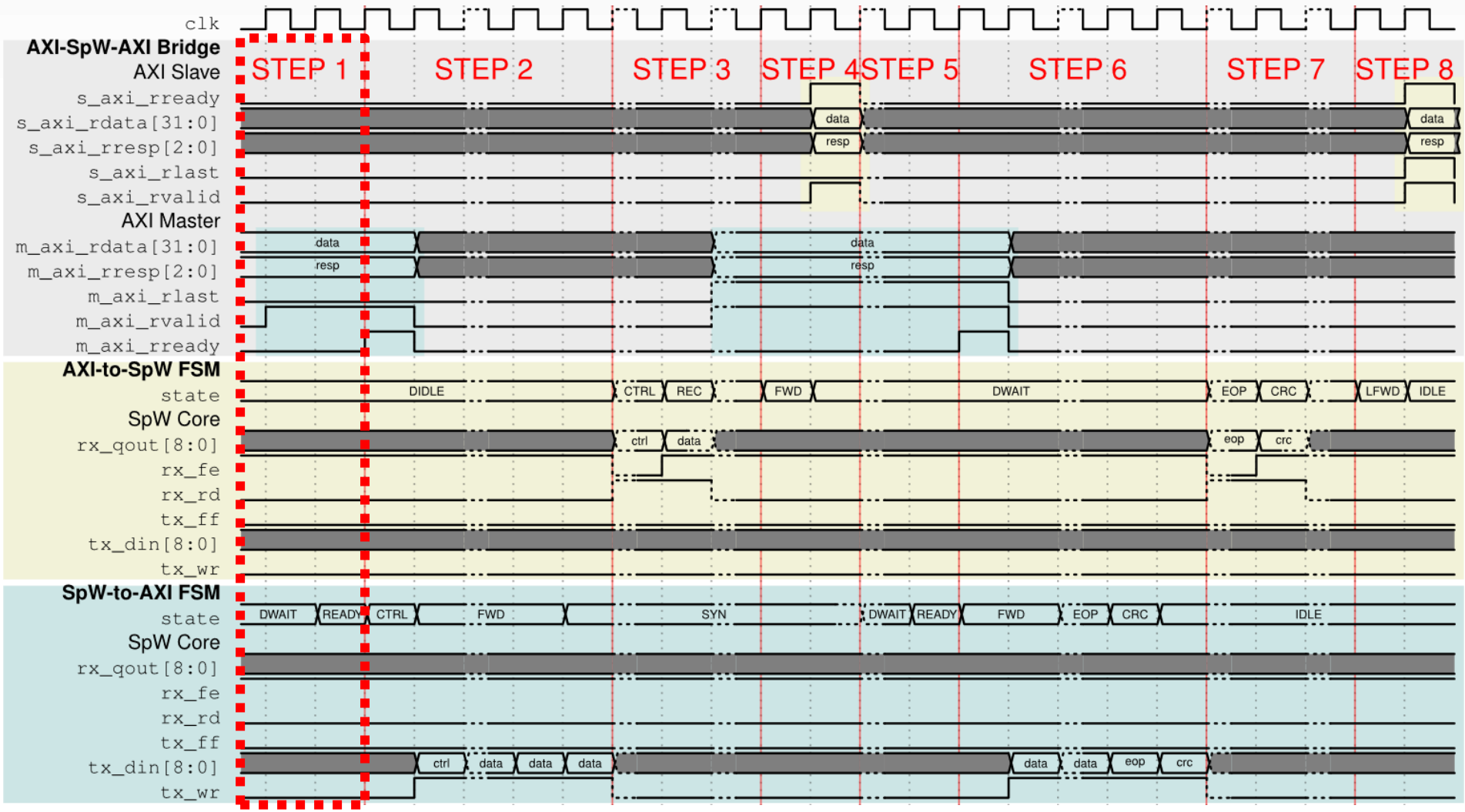
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- Data TX via AXI^{s}
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- Other Data RX via SpW^{+}
- Last Data TX via AXI^{s}



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Read Transaction: Data Channel

First Data RX from AXI^{m}

First Data TX from SpW^{-}

First Data RX from SpW^{+}

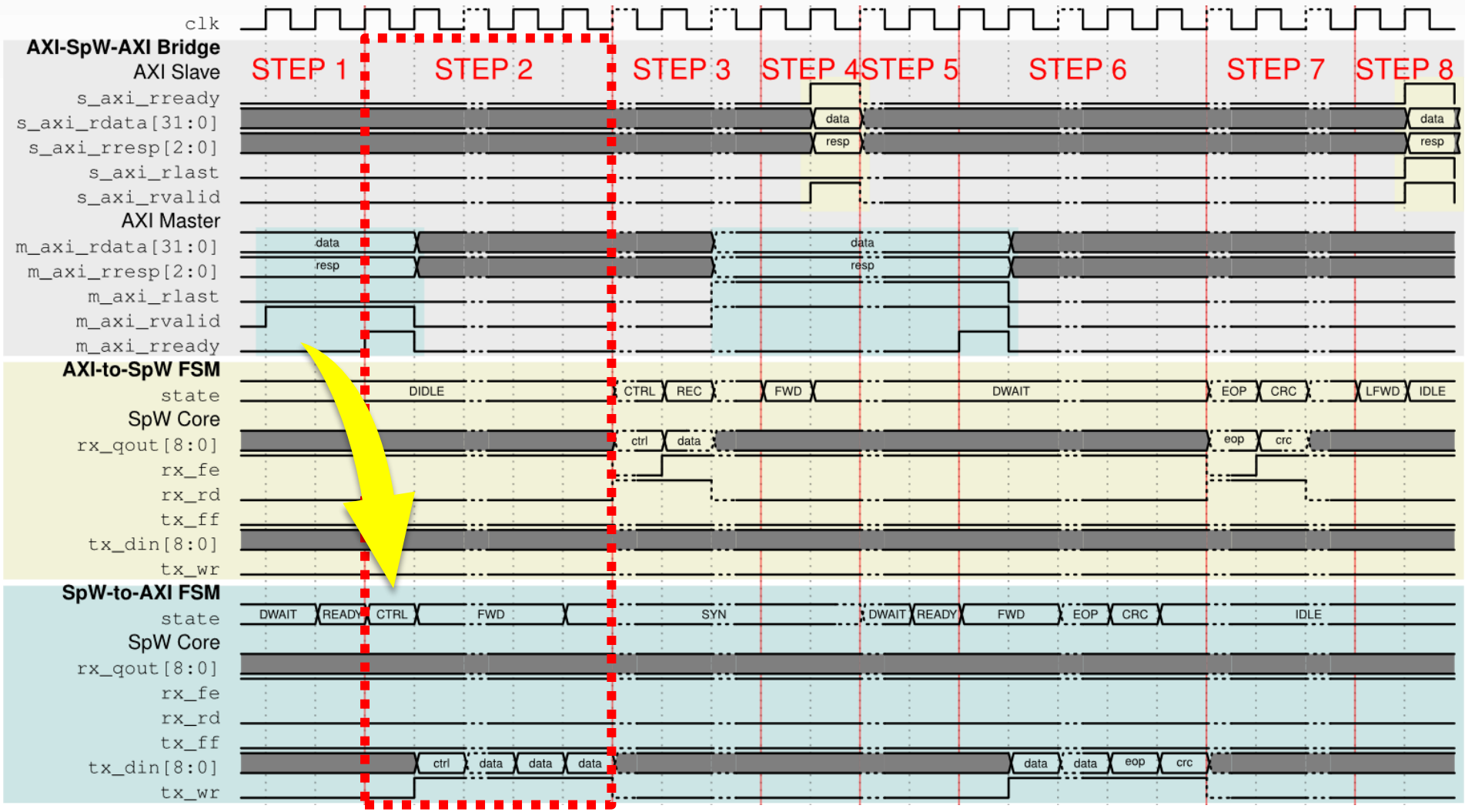
Data TX via AXI^{s}

Other Data RX from AXI^{m}

Other Data TX via SpW^{-}

Other Data RX via SpW^{+}

Last Data TX via AXI^{s}



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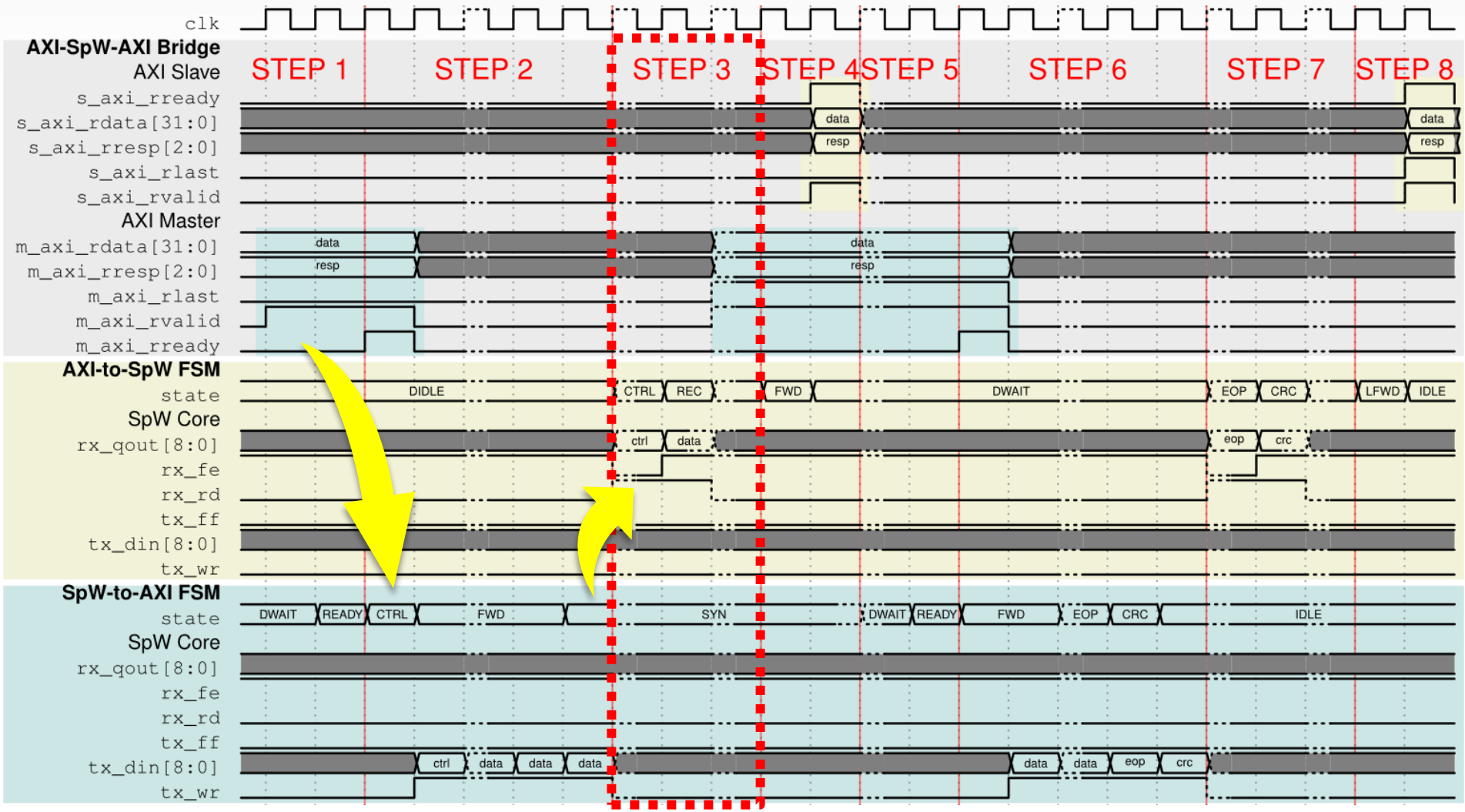
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- Data TX via AXI^{s}
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- Other Data RX via SpW^{+}
- Last Data TX via AXI^{s}



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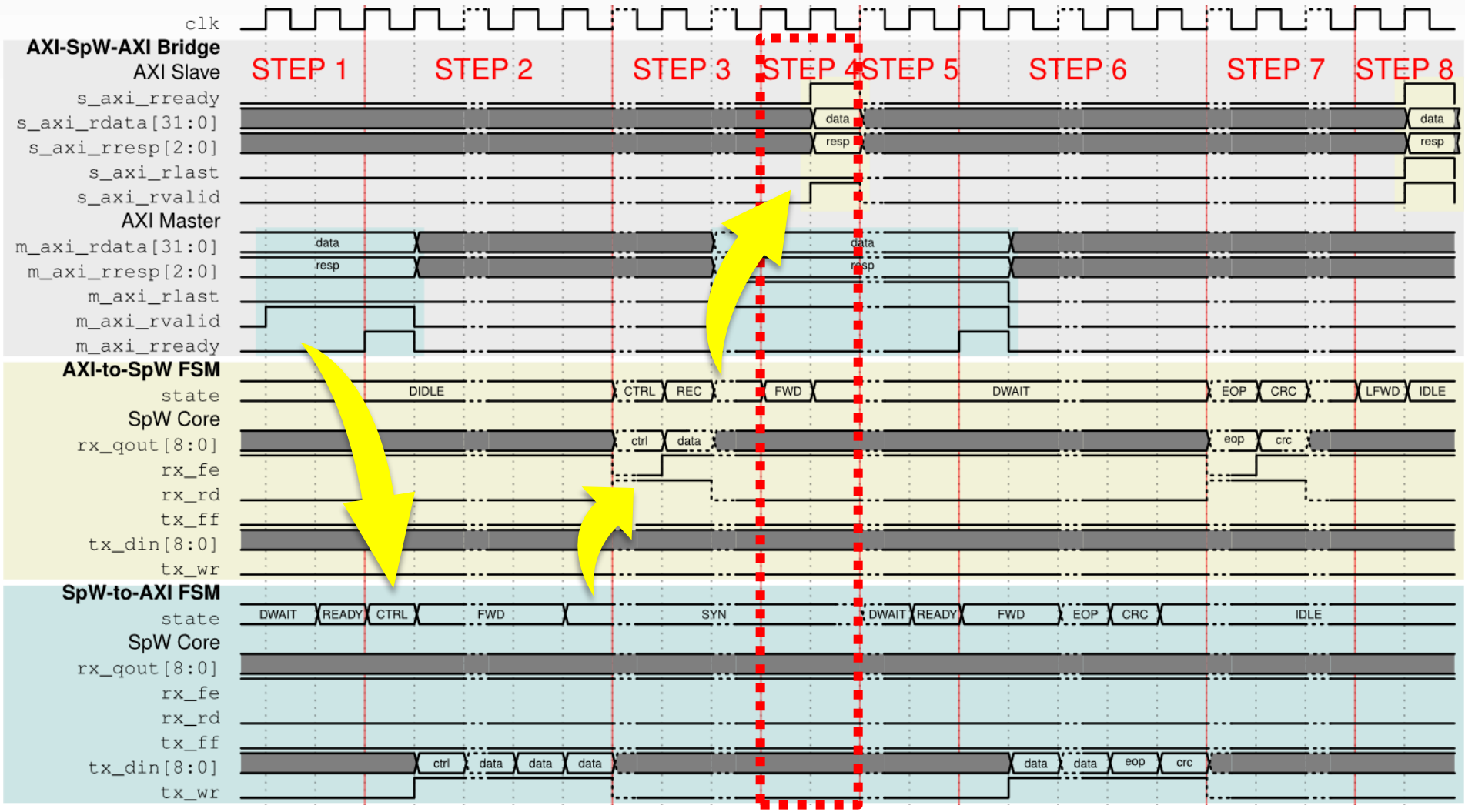
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- **Data TX via AXI^{s}**
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- Other Data RX via SpW^{+}
- Last Data TX via AXI^{s}



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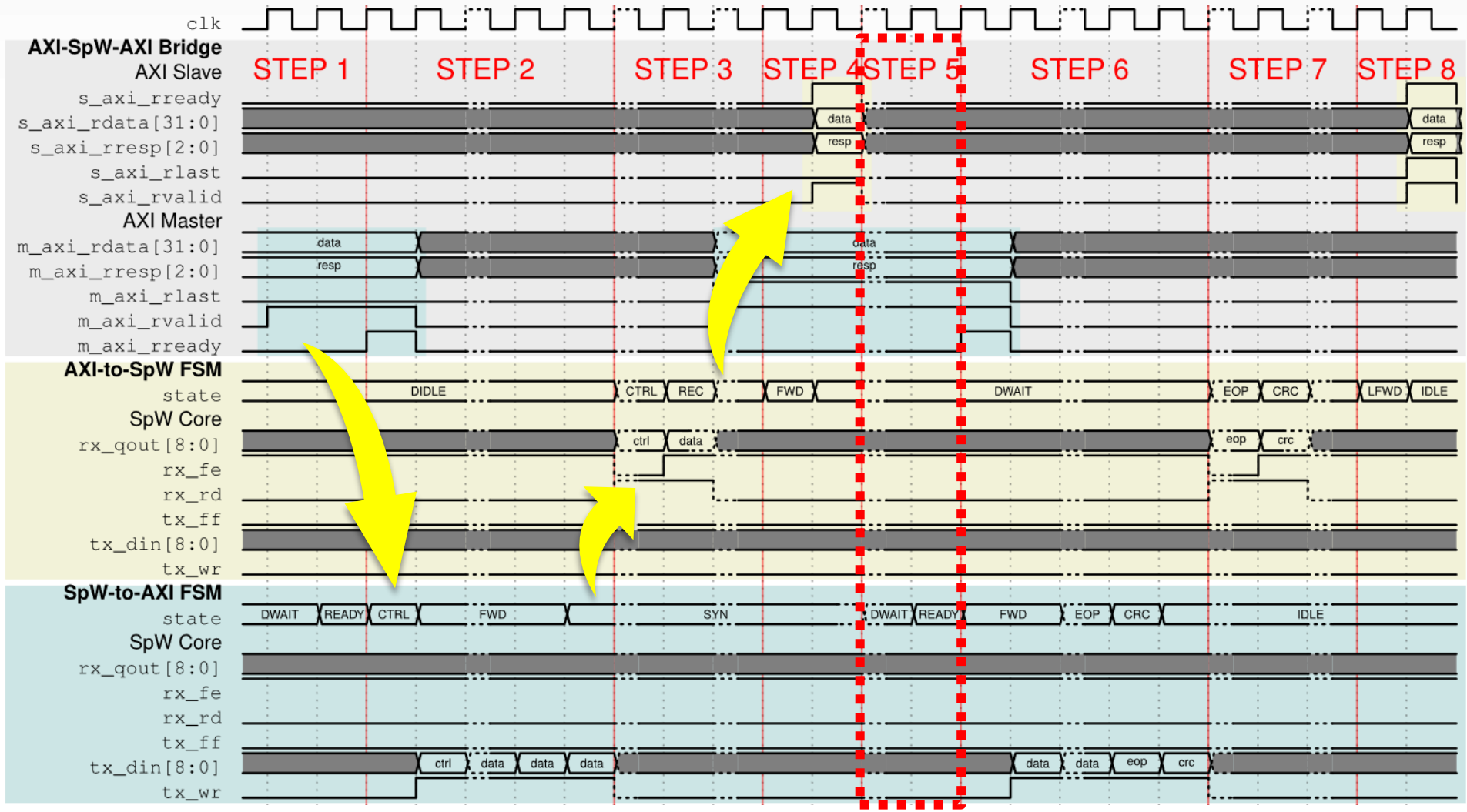
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- Data TX via AXI^{s}
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- Other Data RX via SpW^{+}
- Last Data TX via AXI^{s}



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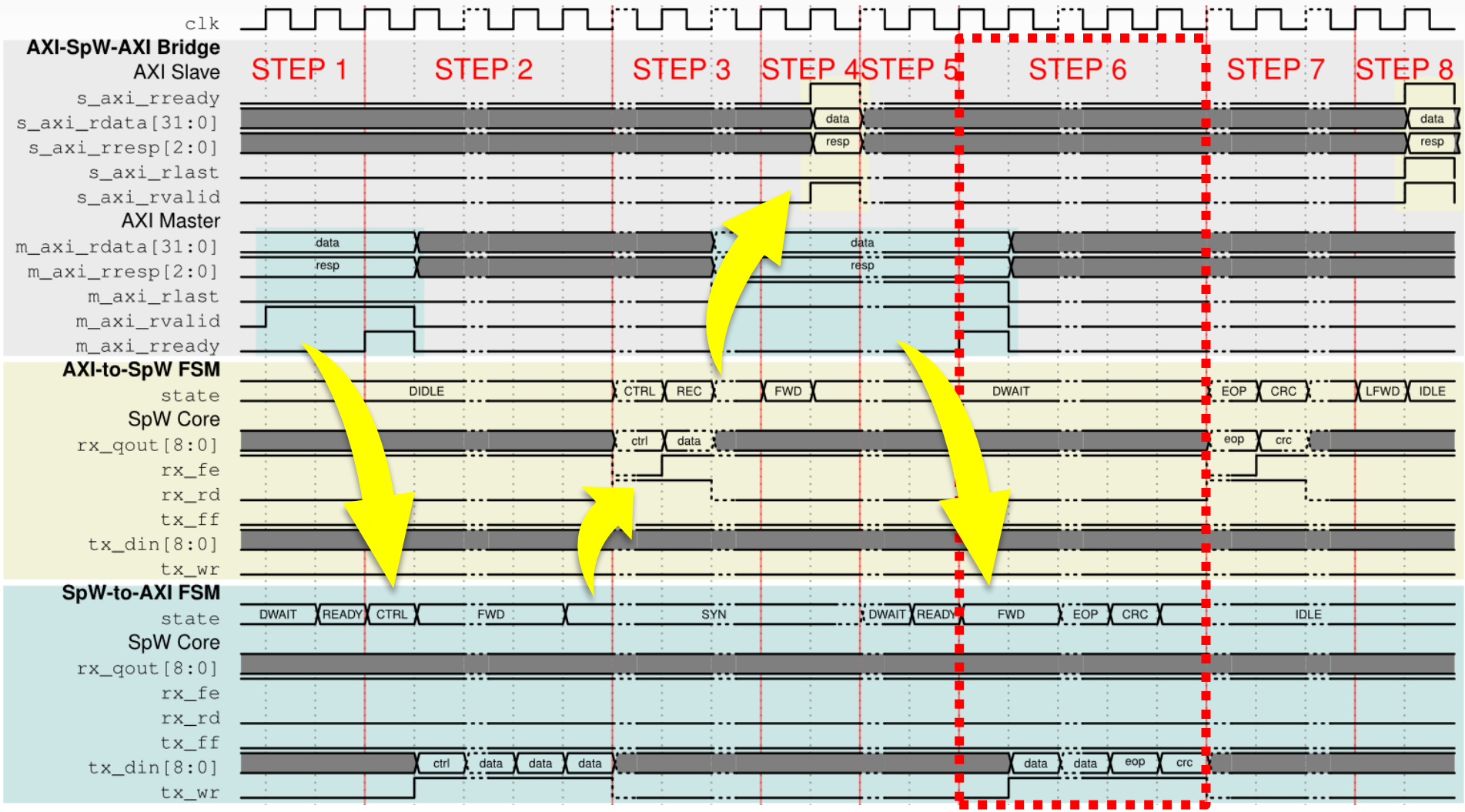
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- Data TX via AXI^{s}
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- Other Data RX via SpW^{+}
- Last Data TX via AXI^{s}



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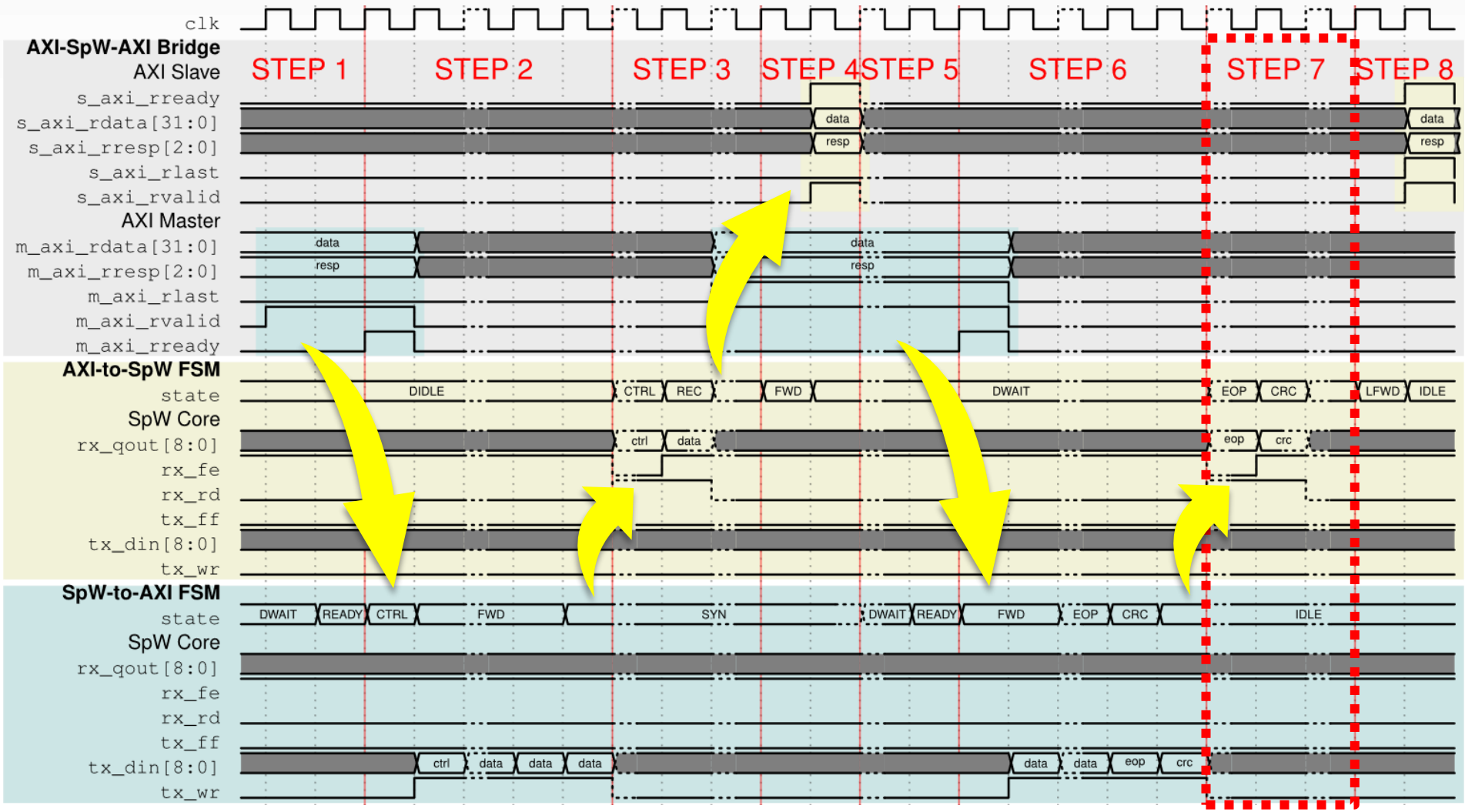
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- Data TX via AXI^{s}
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- **Other Data RX via SpW^{+}**
- Last Data TX via AXI^{s}



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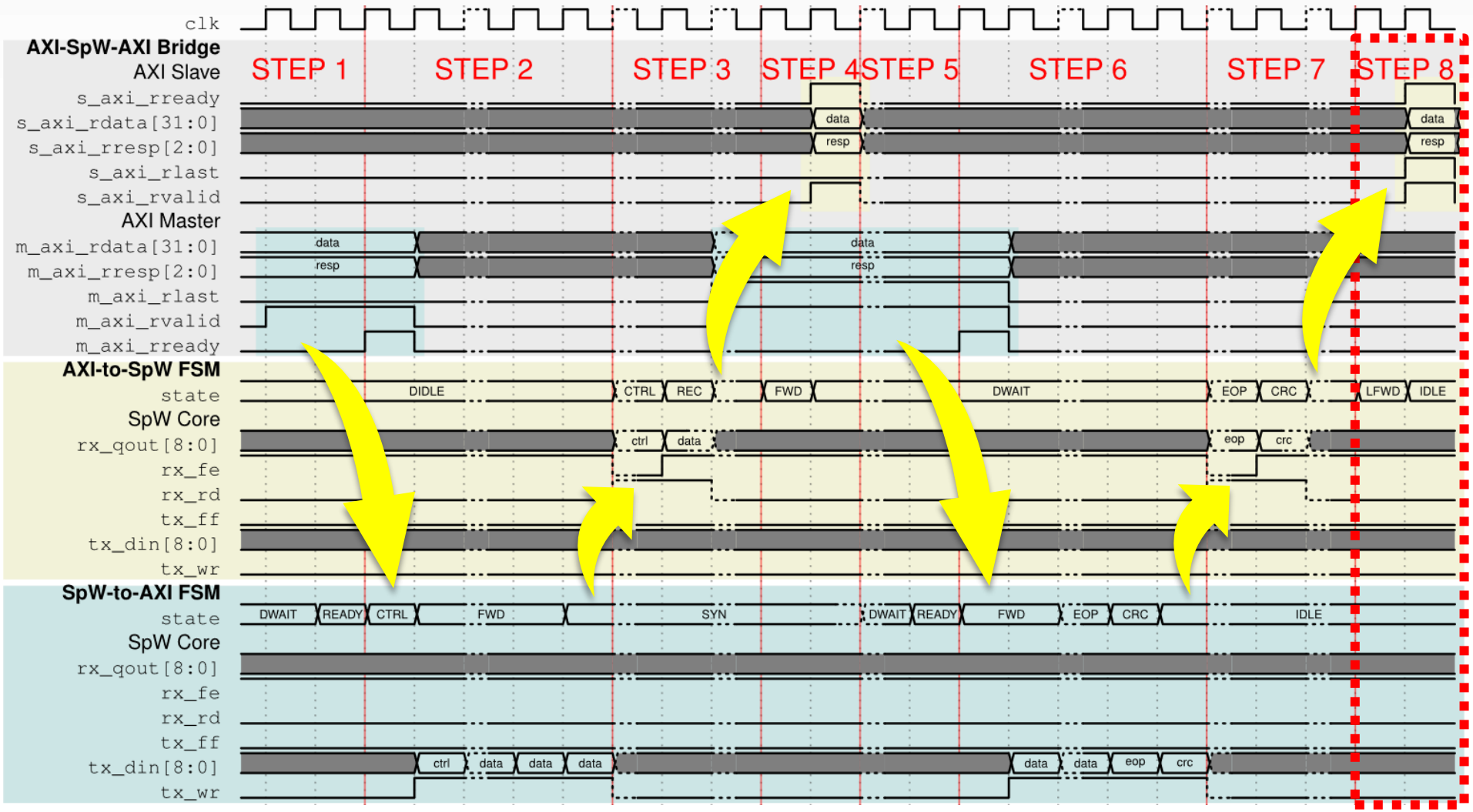
Read Transaction: Data Channel

- First Data RX from AXI^{m}
- First Data TX from SpW^{-}
- First Data RX from SpW^{+}
- Data TX via AXI^{s}
- Other Data RX from AXI^{m}
- Other Data TX via SpW^{-}
- Other Data RX via SpW^{+}
- Last Data TX via AXI^{s}



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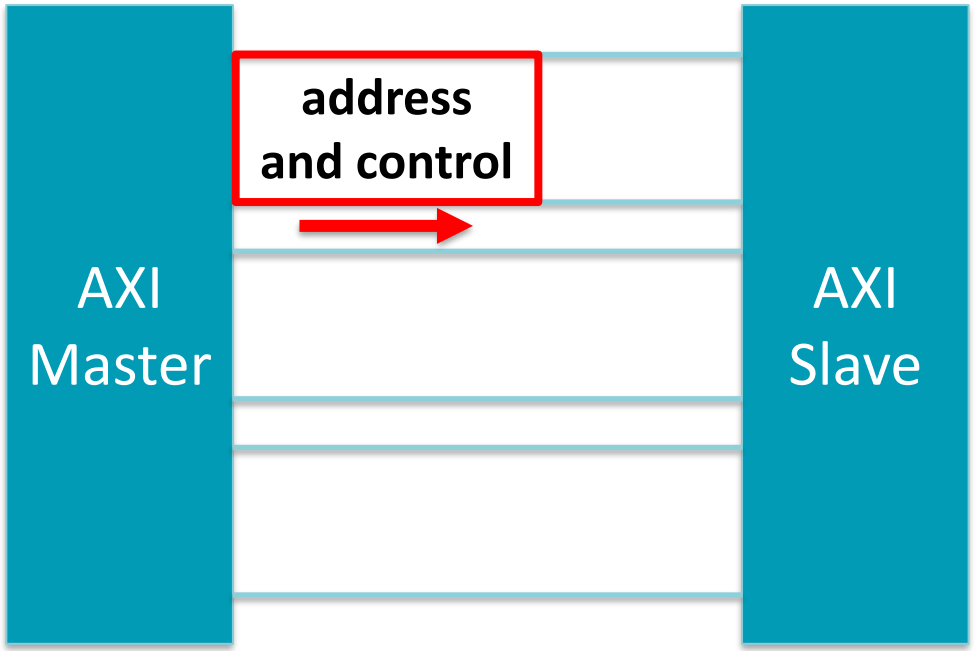
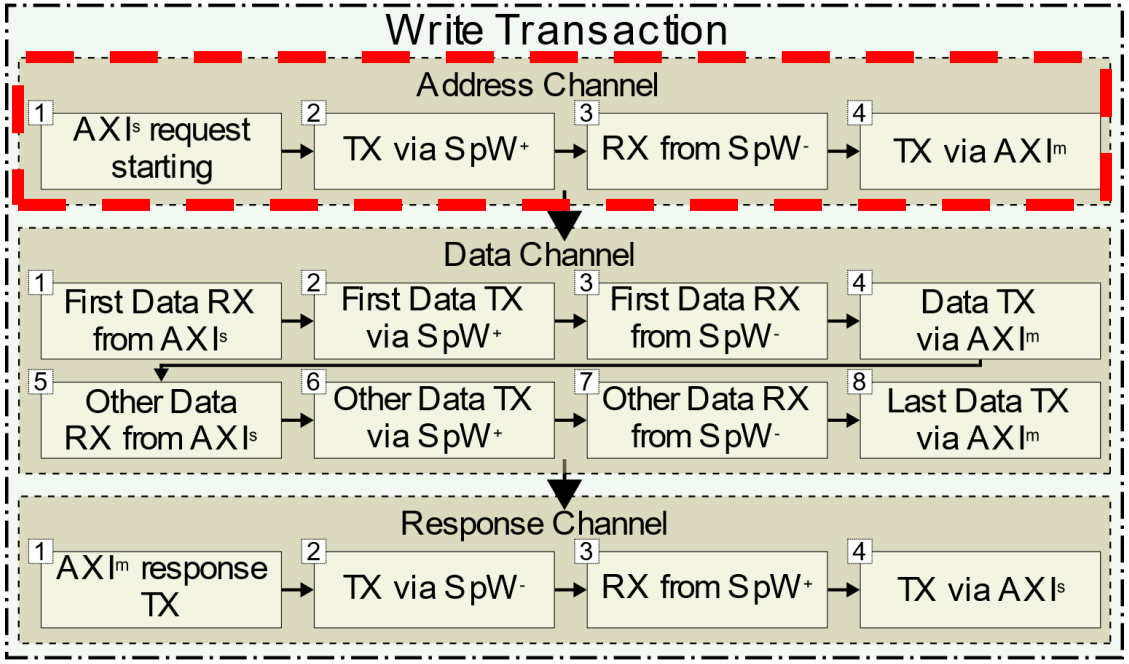
Write Transaction: Address Channel

AXI Transaction



AXI-SpW-AXI Transaction



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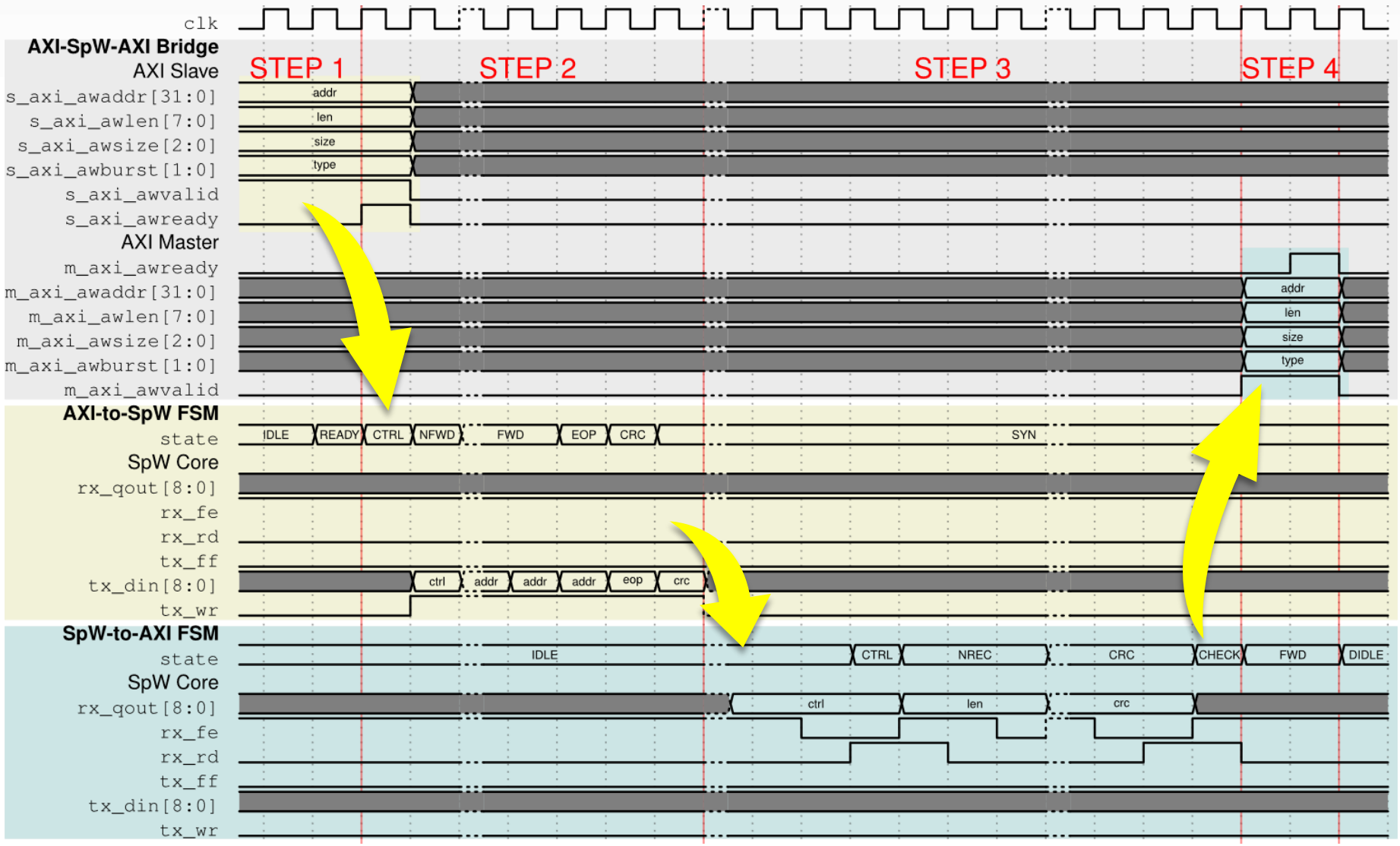
Write Transaction: Address Channel

AXI^{s} request starting

TX via SpW^{+}

RX from SpW^{-}

TX via AXI^{m}



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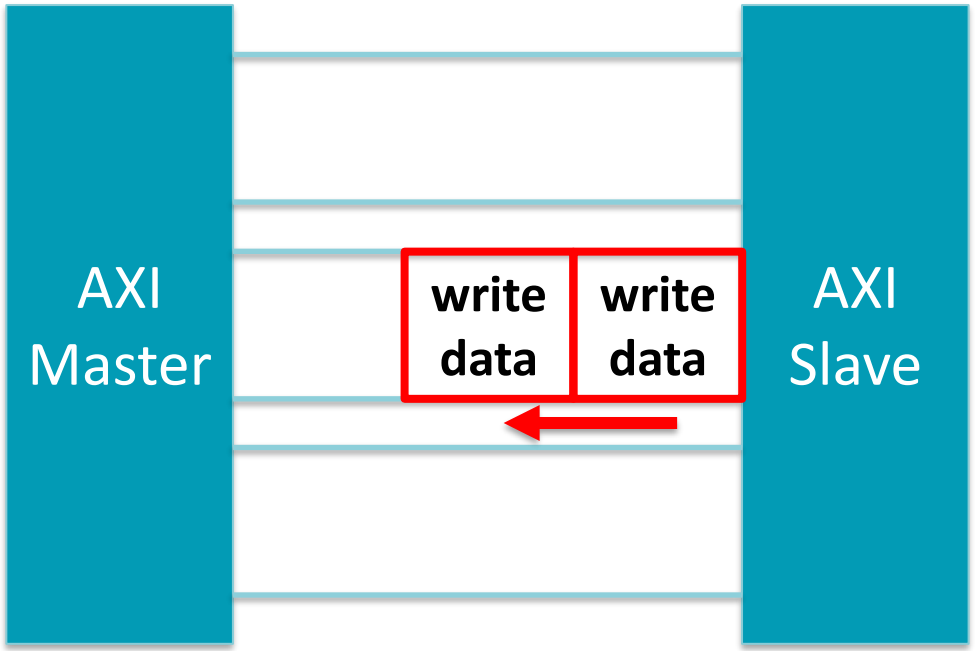
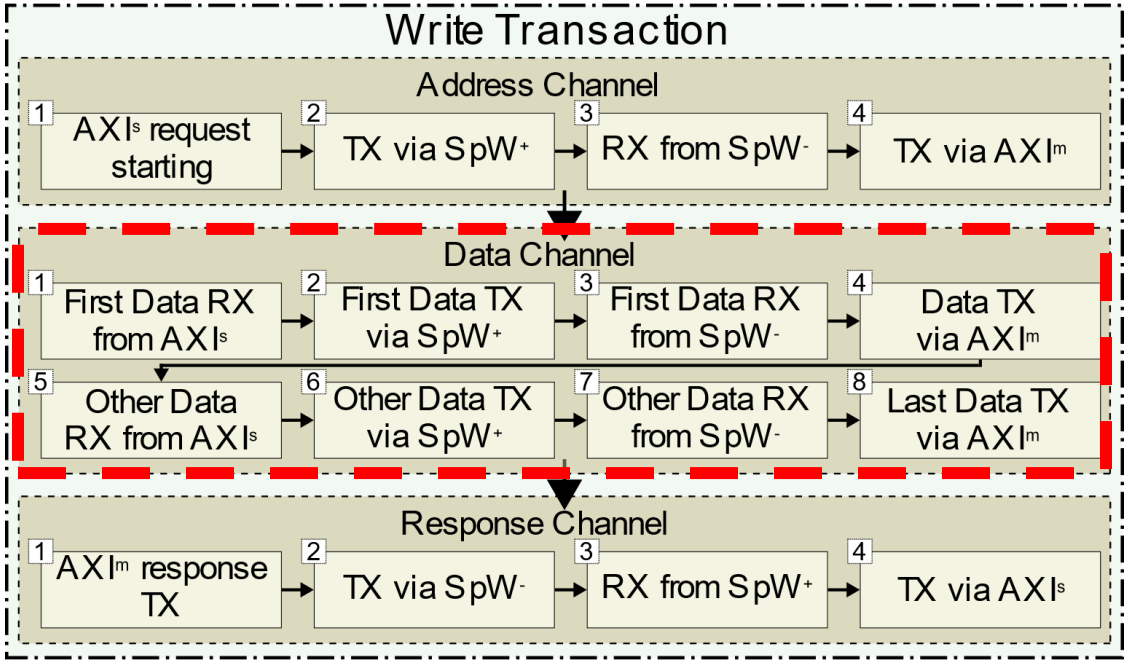
Write Transaction: Data Channel

AXI Transaction



AXI-SpW-AXI Transaction



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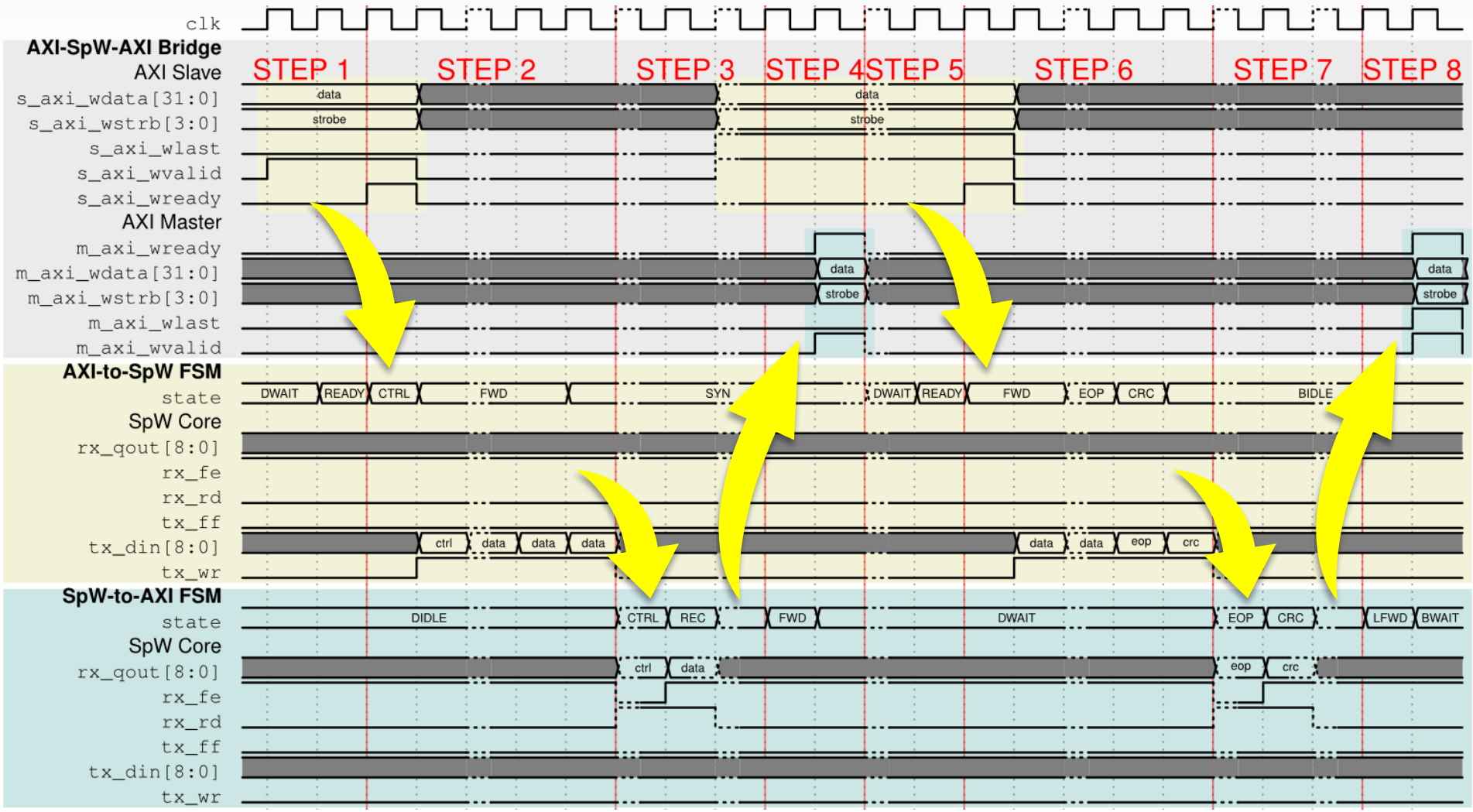
Write Transaction: Data Channel

- First Data RX from AXI^{s}
- First Data TX from SpW^{+}
- First Data RX from SpW^{-}
- Data TX via AXI^{m}
- Other Data RX from AXI^{s}
- Other Data TX via SpW^{+}
- Other Data RX via SpW^{-}
- Last Data TX via AXI^{m}



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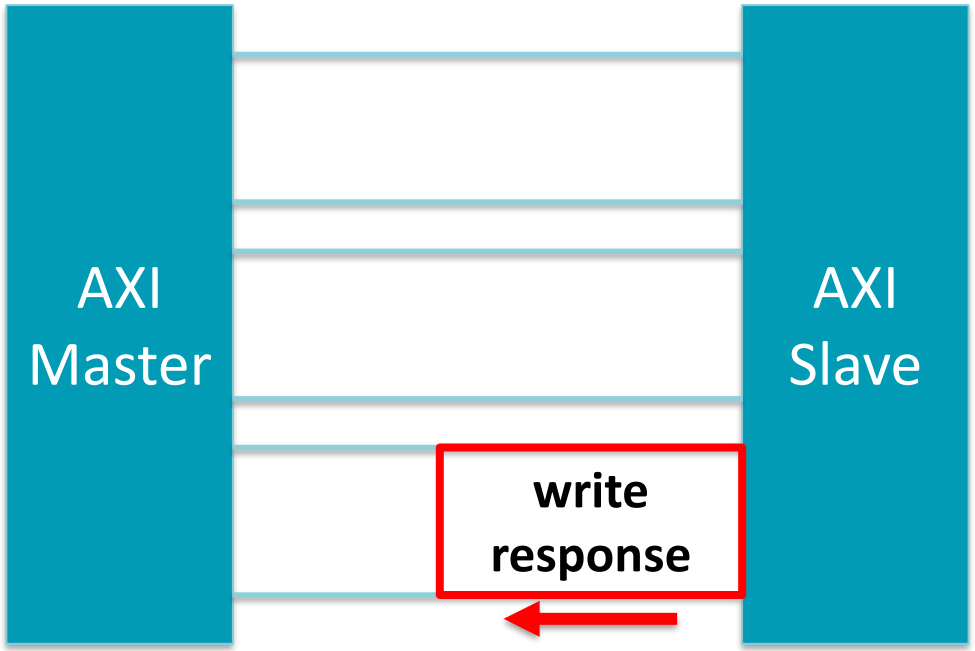
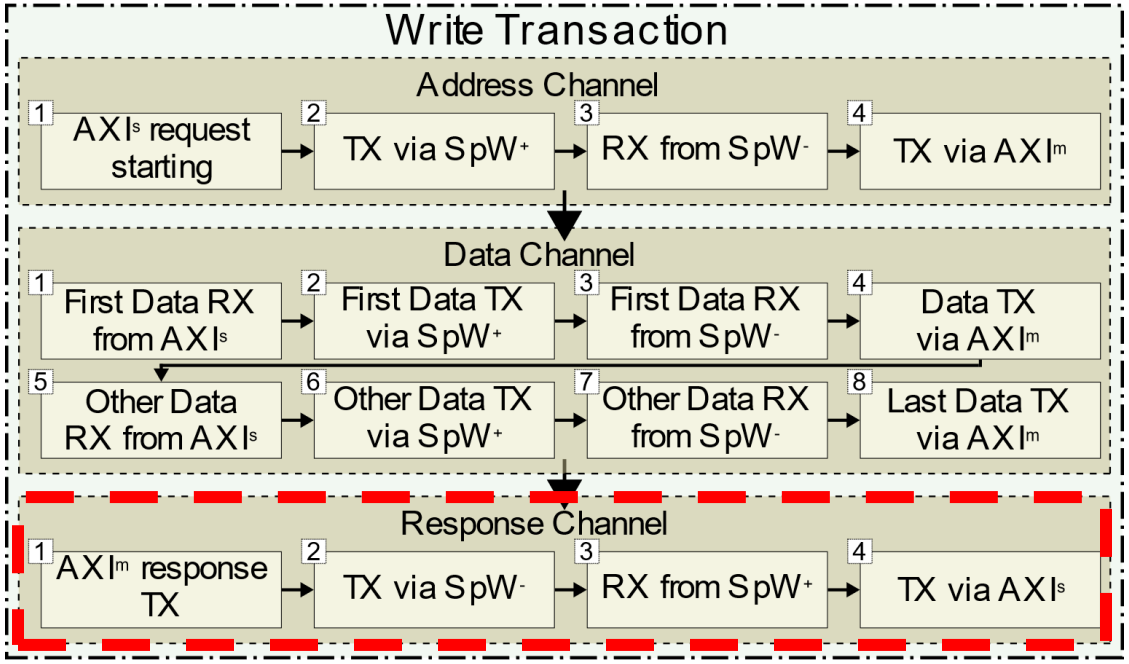
Write Transaction: Response Channel

AXI Transaction



AXI-SpW-AXI Transaction



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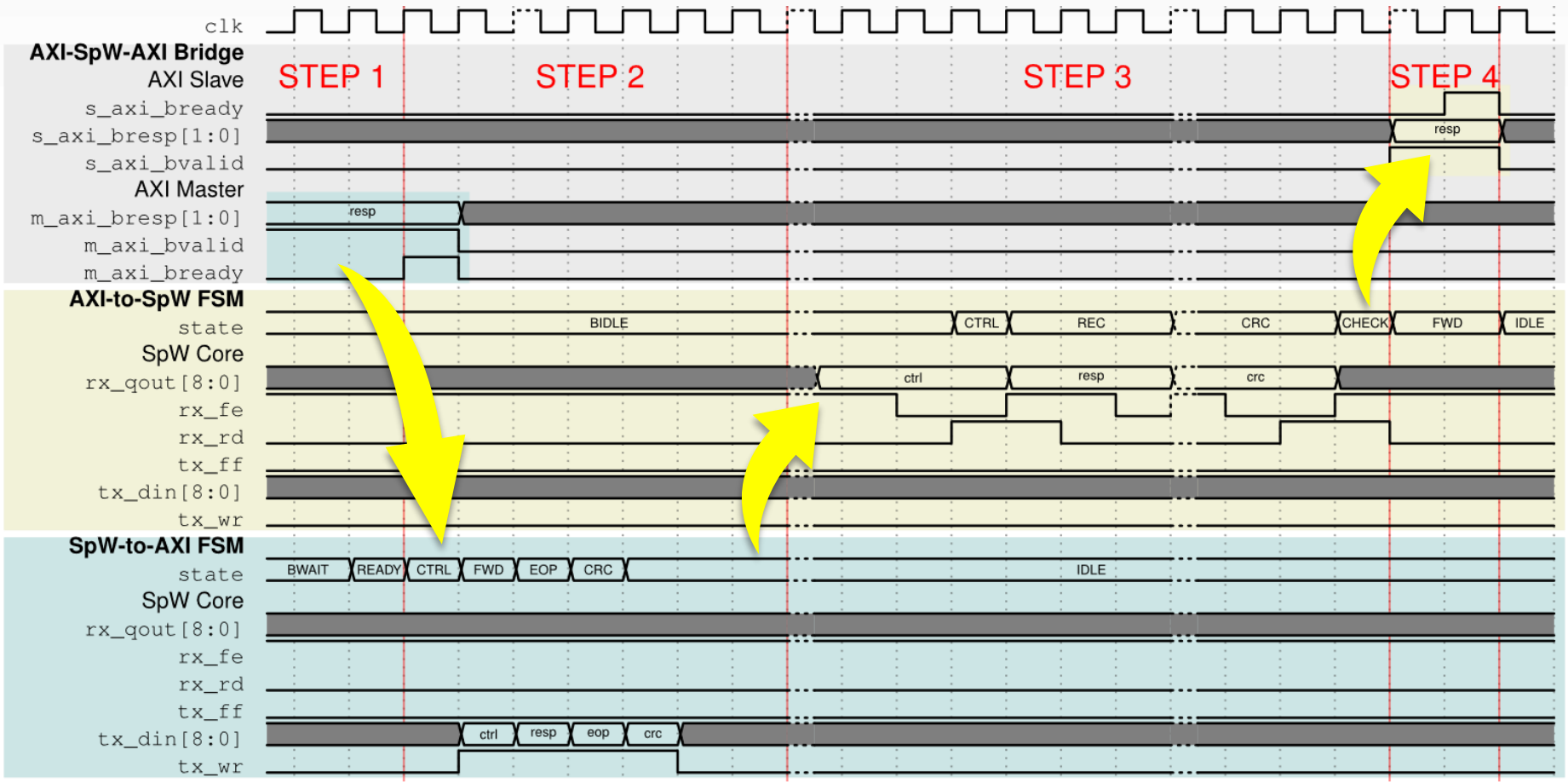
Write Transaction: Response Channel

AXI^{m} response TX

TX via SpW^{-}

RX from SpW^{+}

TX via AXI^{s}



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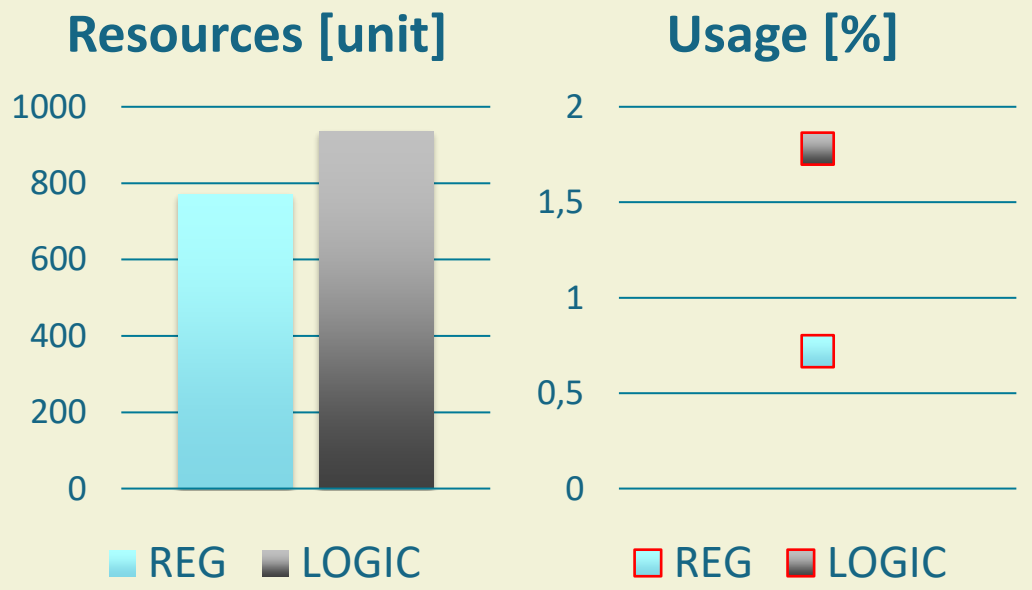
Resource Usage Evaluation: AXI-SpW-AXI Bridge

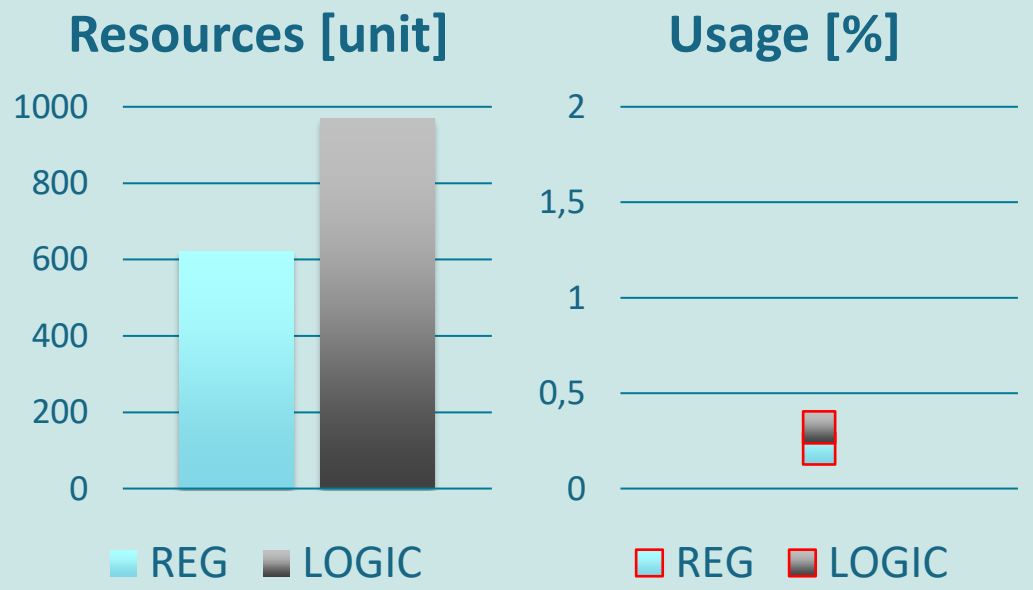
AXI-to-SpW Bridge

target: AMD Xilinx Zynq (XC7Z020CLG484-1)



SpW-to-AXI Bridge

target: Microchip PolarFire (MPF300TS-1FCG1152EES)



VIVADO ML Editions

Libero System-on-Chip

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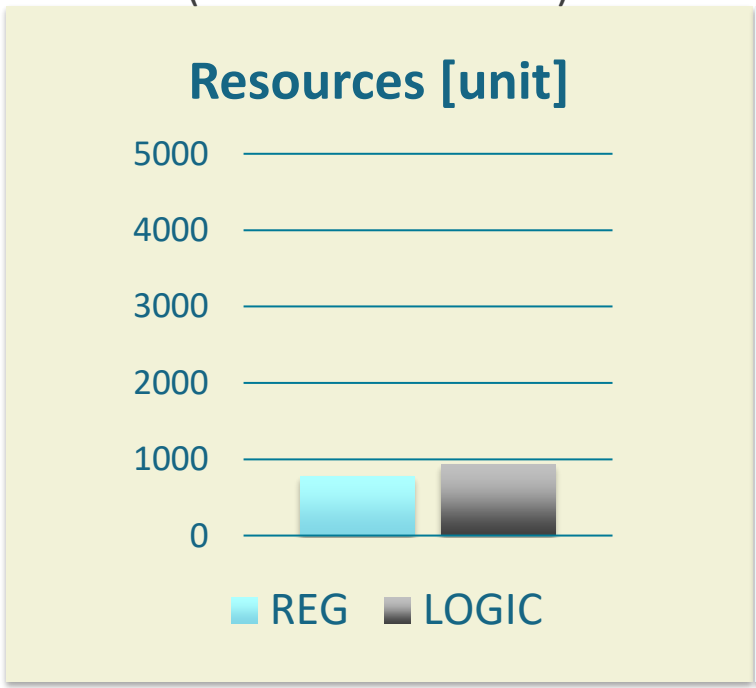
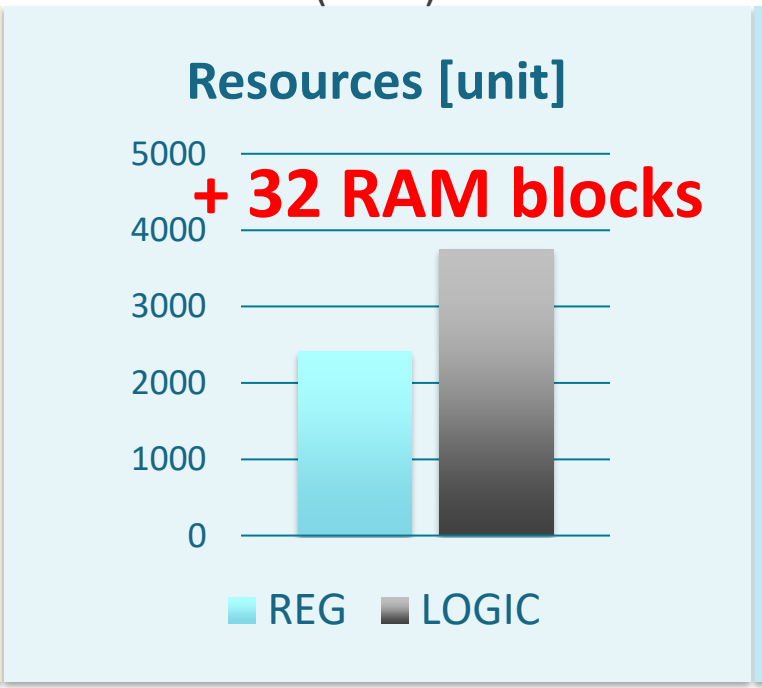
Resource Usage Evaluation: Comparison with SoA

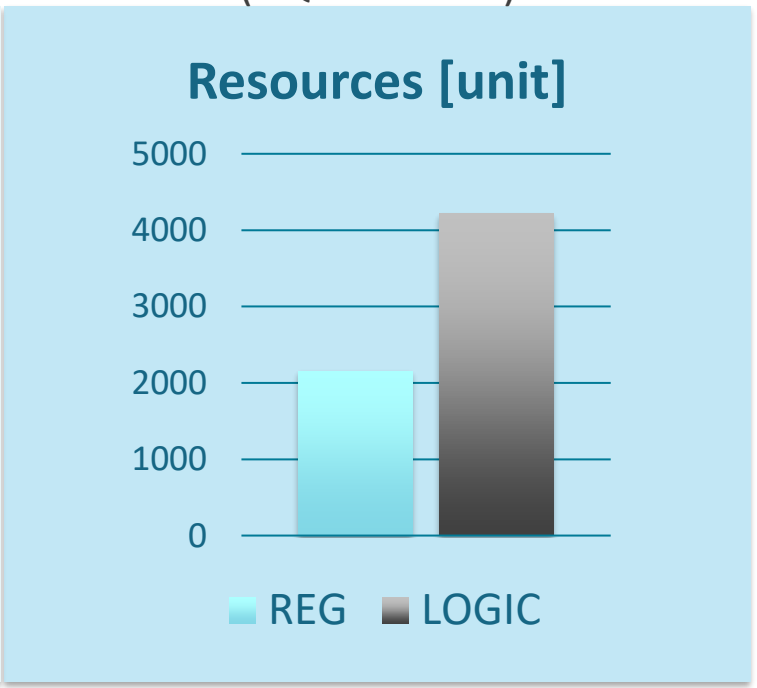
AXI-to-SpW Bridge
target: AMD Xilinx Zynq (XC7Z020CLG484-1)



[1]
target: AMD Xilinx Kintex 7 (410T)



[2]
target: AMD Xilinx Virtex 5Q (XQ5VFX130T)



VIVADO ML Editions

[1] Sterpaio et Al. . "A Complete EGSE Solution for the SpaceWire and SpaceFibre Protocol Based on the PXI Industry Standard"

[2] ESA. "SpW-RMAP-Astrium"

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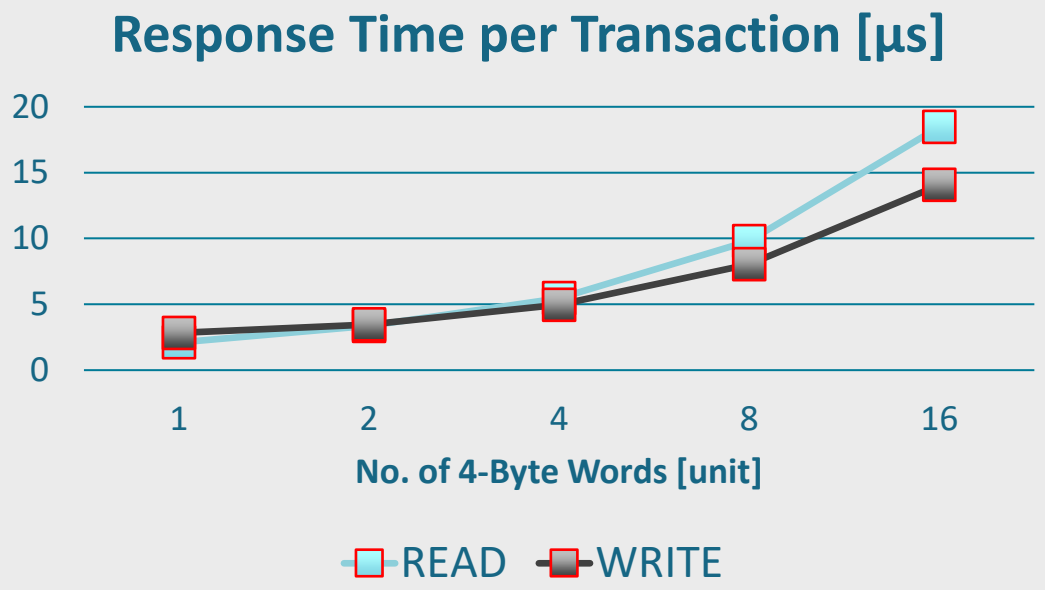
Response Time Evaluation

AXI-SpW-AXI Bridge

(SpW@100Mbps)



ModelSim

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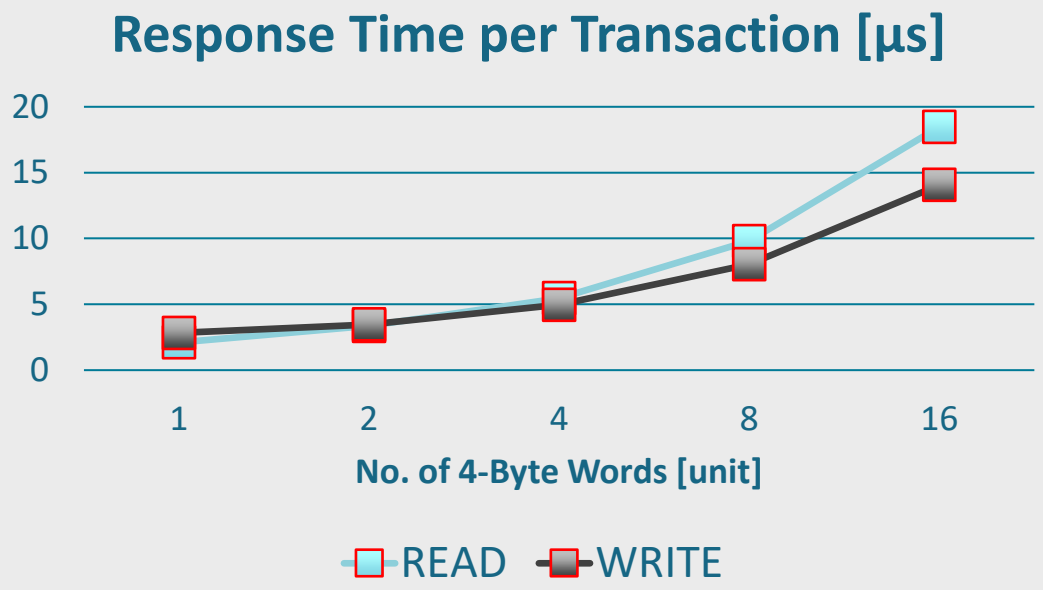
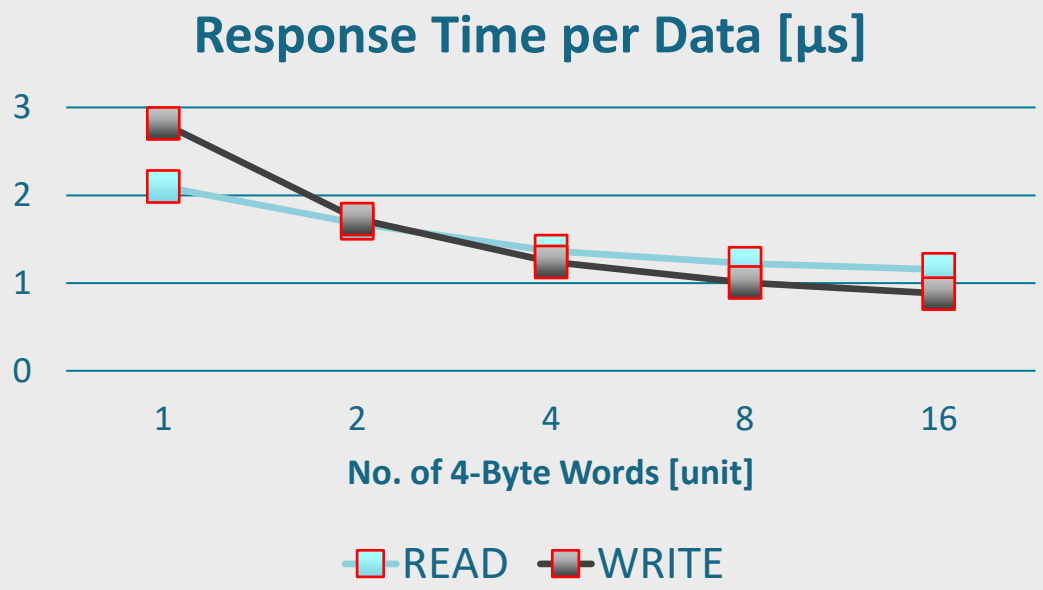
Response Time Evaluation

AXI-SpW-AXI Bridge

(SpW@100Mbps)





ModelSim

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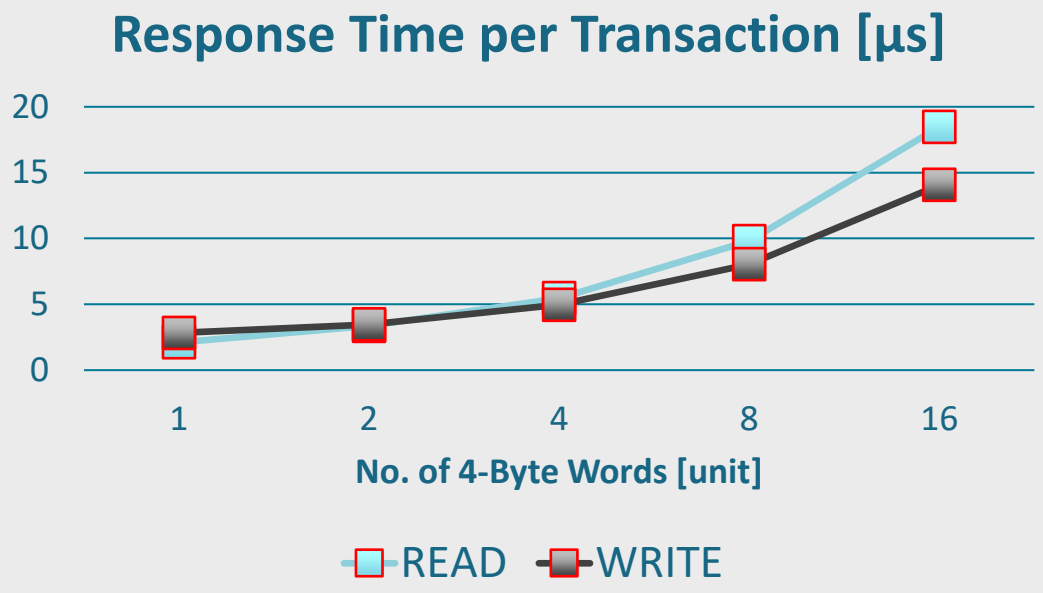
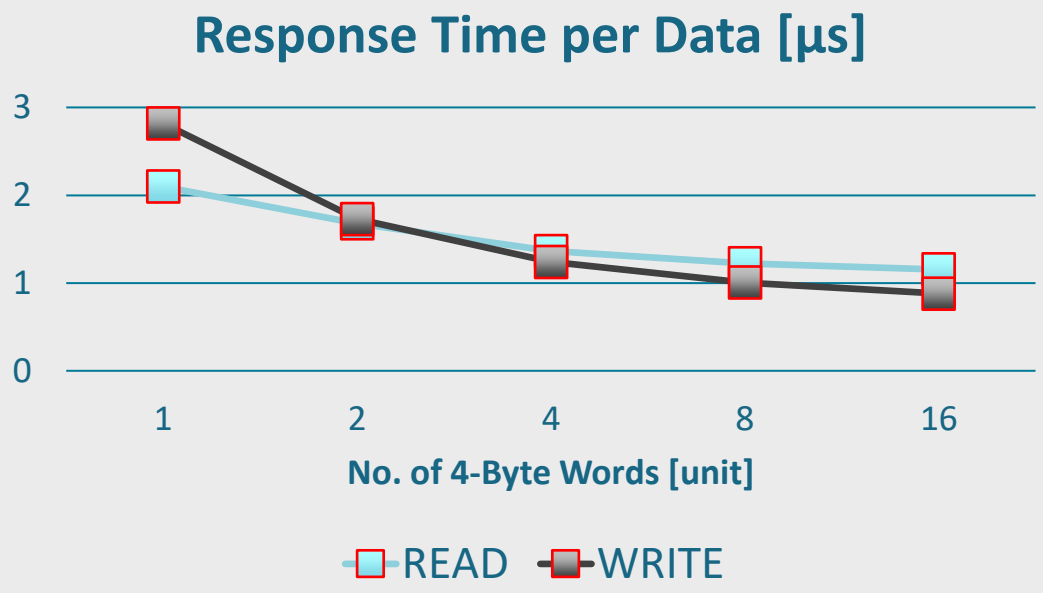
Response Time Evaluation

AXI-SpW-AXI Bridge

(SpW@100Mbps)





ModelSim

RMAP → 16 bytes

AXI-SpW-AXI Bridge → 9 bytes

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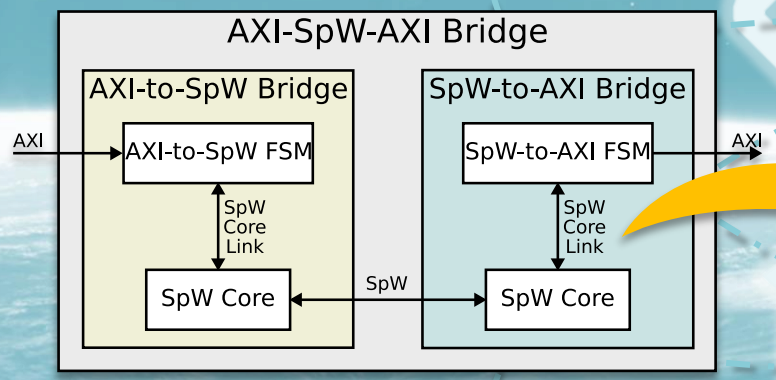
Conclusion



area constraints

latency constraint

100101

few data exchange

RMAP → RMAP Lite?

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Thank you for your attention

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A LOW-OVERHEAD AXI BRIDGE ON SPACEWIRE FOR MULTI-DEVICE SPACECRAFT SYSTEMS

Authors: Claudio Rubattu[1], Walter Errico[1] and Kostas Marinis[2]

Presenter: **Luca Meucci**[1]

[1]SITAEL S.p.A. (ITA), [2]ESA - ESTEC (NL)

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