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A hybrid and reconfigurable edge node computer using SpaceWire and SpaceFibre

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Contents

1. Introduction
2. DESTINY+ MISSION
3. Model-based development
4. Space Cube mk4 for Model-based development
5. Space Cube mk4 architecture
   - SpW/SpFi router
   - Software development kit (SDK) for Model-based development
6. Conclusion

Introduction

- Space Cube mk4 for reducing the development duration
  - Destiny+ satellite system needs shorter development duration
  - Model-based development process to meet the requirement of shorter duration

- Characteristics of Space Cube mk4
  - Space Cube mk4 has both of Field Programmable Gate Array (FPGA), and Dynamically Reconfigurable Processors (DRPs).
  - SpW/SpFi interface for efficiently ground support equipment
  - Dynamically Reconfigurable Processors (DRPs) for efficiently coding

DESTINY+ Mission

Mission objectives

- Developing spaceflight technologies using electric propulsion and expand the range of its utilization
- Expanding the opportunities for small body exploration by acquiring advanced asteroid flyby exploration technologies
- The chance for Phaethon flyby is only one time
  → The simulation on the ground requires higher accuracy, and model-based development with Space Cube mk4 can realize this requirement.

Milestones

- Nominal launch window FY2024

DESTINY+ specifications

- 480 kg spacecraft with an Ion Engine System

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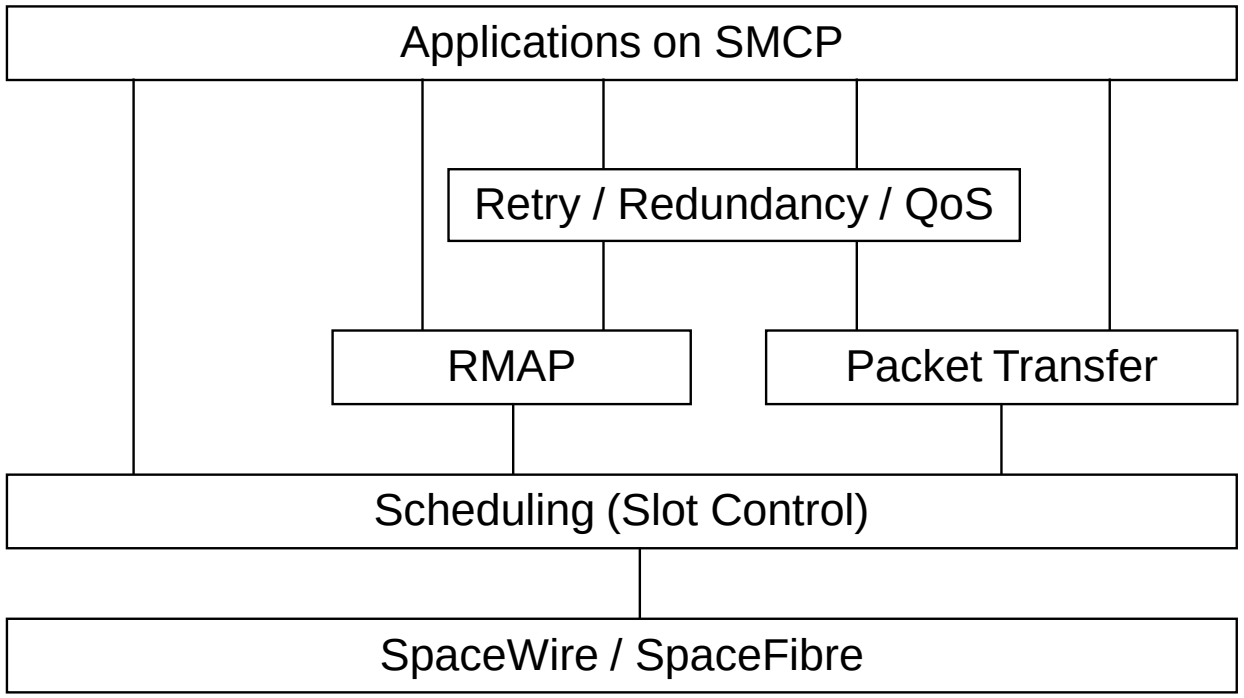
Model-based development

- The standard middleware is based on Space Monitor & Control Protocol (SMCP) designed by JAXA/ISAS.
- Thanks to this standard middleware, it is easy to assemble the model on the processors LEON5, DRP, and Xilinx Kintex UltraScale.



Space Cube mk4(1)

- Three types of processing elements (PEs) are integrated on a Space Cube® mk4.
  - Xilinx Kintex UltraScale FPGA with a micro-processor LEON5 IP
  - RZ/V2M (Dynamically Reconfigurable Processor =DRP)
  - RZ/A2M (DRP)

The outlook of Space Cube® mk4 and its interior assembly

Space Cube mk4(2) -Details of three processing elements (PEs)-

- Xilinx Kintex UltraScale FPGA -①

LEON5 IP for practical way to establish design framework as a software development kit (SDK)

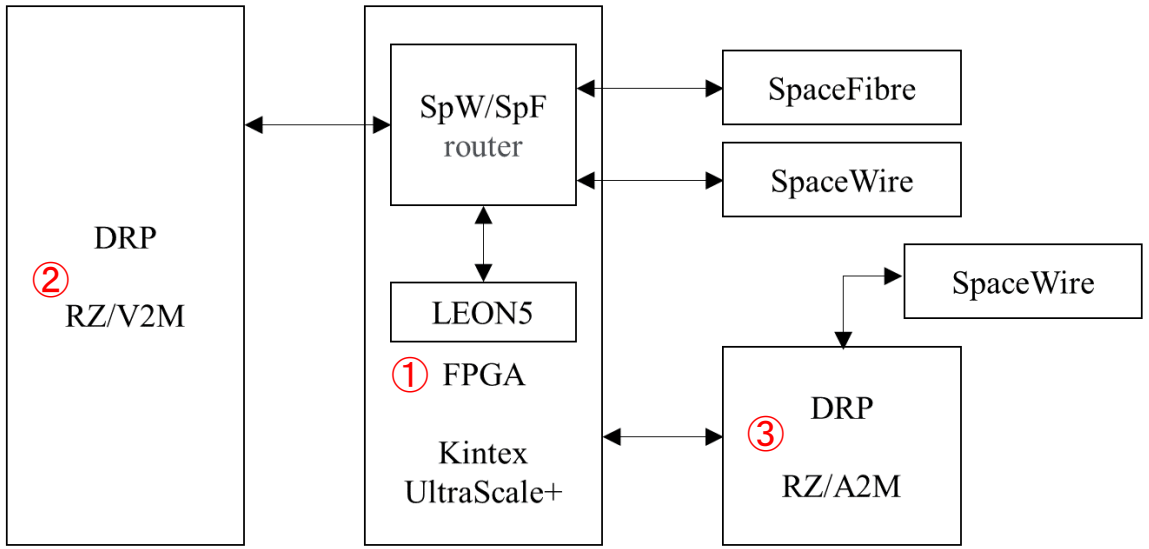
SpW/SpFi router developed by NEC

- RZ/V2M -②

Heavy load processing as neural network functions for artificial intelligence applications can be implemented with sufficient low power consumption as an edge node processor.

- RZ/A2M -③

RZ/A2M is used as a small-scale embedded controller with an Arm®-based micro-controller.



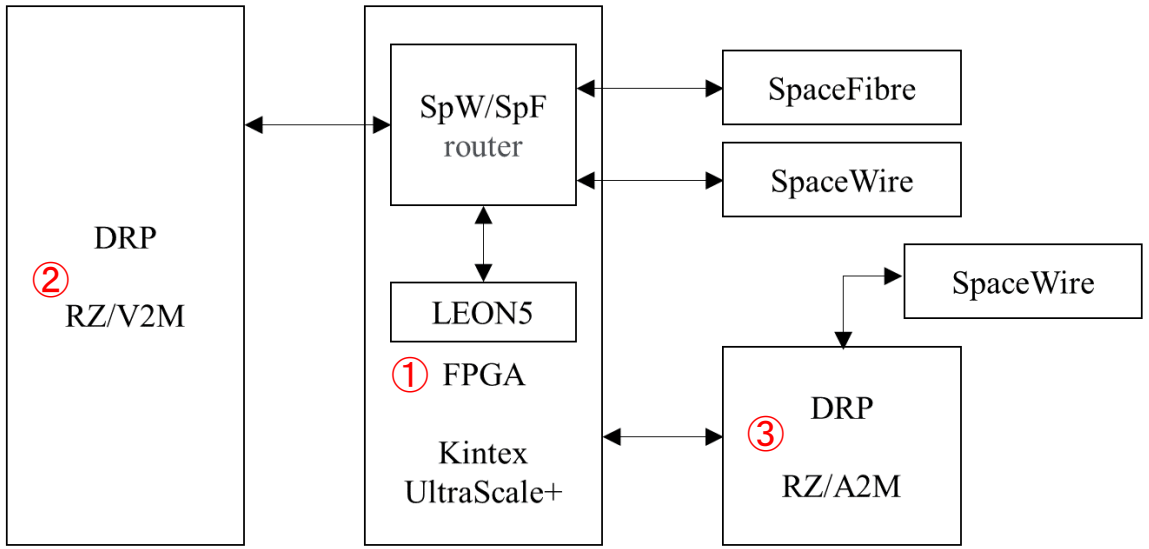
Space Cube mk4(3) –other characteristics of DRPs-

RZ/V2M

- Connected to FPGA through PCI Express interfaces
- Transmition at high speed to the onboard equipment from the SpaceWire and SpaceFibre interfaces

RZ/A2M

- Several input/output (I/O) circuitries
- Wire rate processing capability up to 10 MHz by programmable software



Space Cube mk4 architecture

- Higher level signal processing and protocol handlings are performed by software.
  - Software development kit (SDK) for Model-based development to make developers understand the reference model of complex level onboard processing
    (even the case of component like "all hardware logic")
  - The reference model includes onboard computer architecture, communication model, and database scheme for satellite operations.

- Transferring the software simulation results easily
  - By utilizing these DRPs, it is possible to transferring the software simulation results easily in short time, and the switchover from a simulation to the actual device evaluation becomes smooth.

Conclusion

- Versatile simulator
  - Space Cube® mk4 accommodates three types of processing element, a conventional micro-processor, an FPGA, and a DRP.
- Established based on SMCP
  - The method to exploit hybrid and reconfigurable computing technology has been established based on Spacecraft Monitor & Control Protocol (SMCP) designed by JAXA/ISAS.
- Model-based development
  - The process is employed prior to system level integration test to follow the tight development schedule.
- DRPs and a SpaceWire/SpaceFibre router are key components
  - Extensive simulation is performed by a hardware-in-the-loop simulator.

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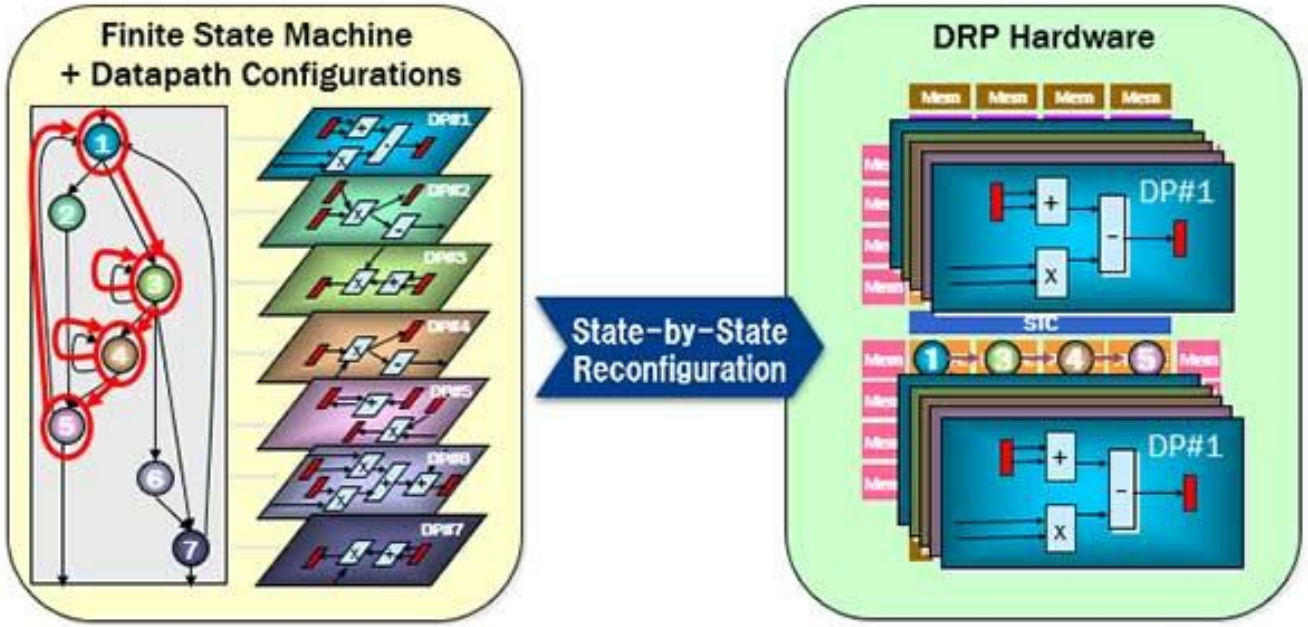
Dynamically Reconfigurable Processor (DRP)

- High-speed context switching capability.
- Several context planes in a chip
  - Context switching even in every clock cycle.
- Wire rate processing capability up to 10 MHz by programmable software

https://www.renesas.com/jp/en/application/key-technology/artificial-intelligence/voice-face-recognition/drp



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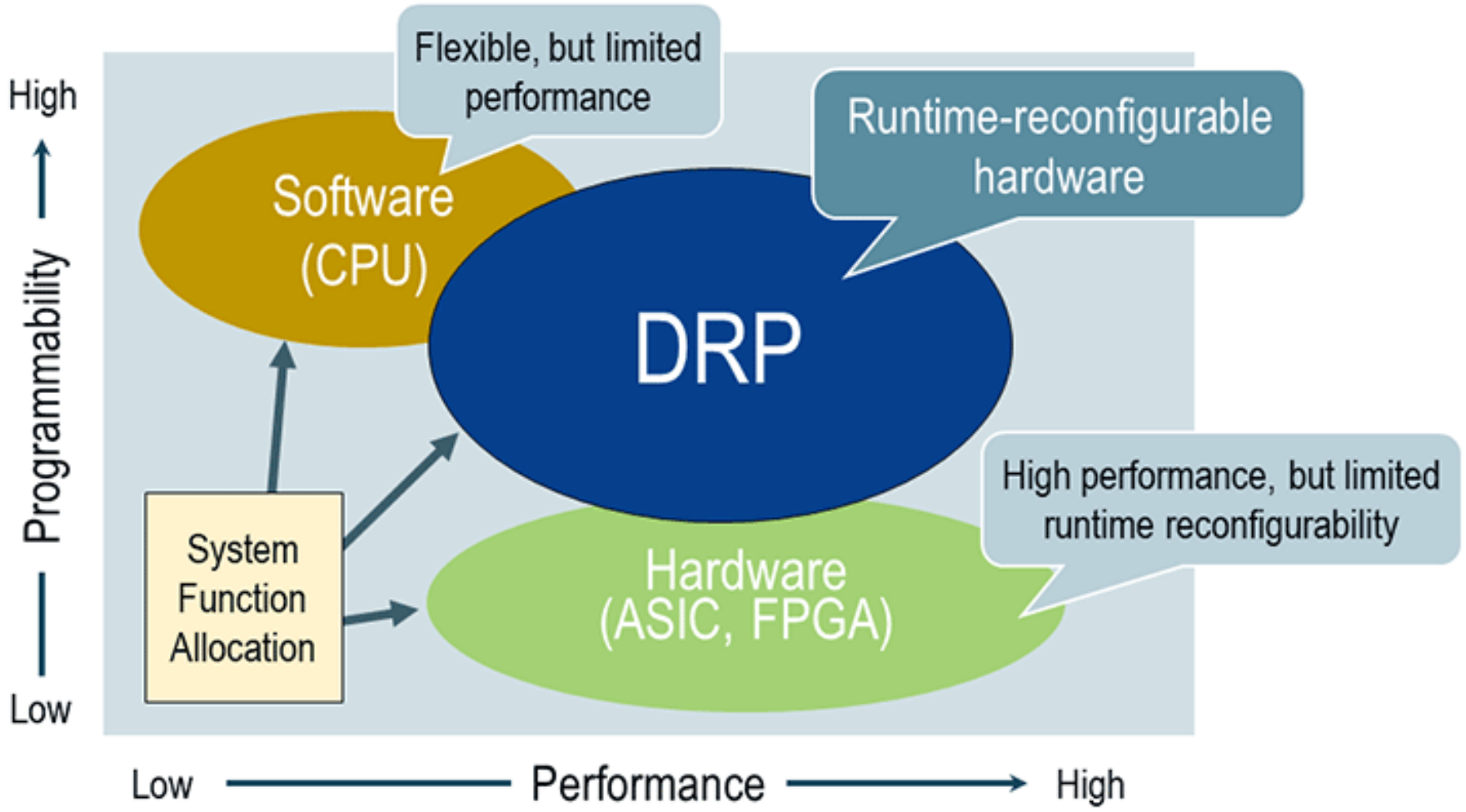
Dynamically Reconfigurable Processor (DRP)



https://www.renesas.com/jp/en/application/key-technology/artificial-intelligence/voice-face-recognition/drp

Model-based development

- The standard middleware is based on Space Monitor & Control Protocol (SMCP).
- This protocol is performed by a conventional MPU. SMCP was developed by JAXA/ISAS [9, 10].
- The protocol aims at unified building method of commands, telemetry messages, and sequence for all satellites and onboard equipment.
- Telemetry and Command processing functions are realized through SMCP.
- Reliability and timeliness were taken into account by exploiting Remote Memory Access Protocol (RMAP) and Time-Code delivery function.
- Retry and Redundancy control are carried out using Cyclic Redundancy Check (CRC) in RMAP packet.
- Quality of Service (QoS) functions are provided by SpaceFiber protocol. Scheduling (Slot Control) are implied by Time-Code.