

An Optical SpaceFibre Testbed for Transceiver Evaluation & Validation of a Design-Time Configurable Router

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Who we are





Malte Bargholz Junior Professional in On-Board Data-Handling European Space Agency



Wolfgang Rönninger Young Graduate Trainee in Microelectronics European Space Agency



Felix Siegle *Payload Data-Handling Engineer* European Space Agency

- Former trainee at ESA, now staff
- Interested in payload processing, high-speed SoC design, ML/AI acceleration
- Background in embedded system development, both HW and SW
- Former trainee at ESA, now digital designer at Axelera AI, Netherlands
- Interested in digital and ASIC design, GNSS processing, AI/ML acceleration
- Background in electrical engineering with digital design specialization
- Staff in the On-Board Computer and Data Handling Section, ESA-ESTEC
- R&D in the field of mass memory units, high-speed links, and future data handling architectures
- Project support (CO2M, Biomass, Solar Orbiter, Euclid...)

Motivation



- Current trends in on-board data-handling
 - More data from payloads: multi-spectral image sensors, SAR, ... (multiple Gbit/s)
 - Faster downlinks (100 Mbit/s \rightarrow >1 Gbit/s)
 - Harness reduction, higher integration density

→ Future DH systems have to handle multiple multi-Gigabit data sources and sinks with minimal harness

- Optical high-speed links are a promising option for future on-board communication
 - High-performance (> 10 Gbit/s) and good signal-integrity over long distances
 - Favorable SWaP parameters:
 - Low Power (typically ~100mW per transceiver channel)
 - Lightweight cabling and connectors
 - Built-in fault isolation
 - Wide-range of protocols due to SerDes: SpaceFibre, Serial RapidIO, WizardLink, many commercial protocols...

Agenda



Goal: Evaluate optical high-speed links in the context of future on-board data-handling systems

- 1. Create representative testbed that mimics future optical-based on-board data-handling architecture
 - Using optical high-speed transceivers from different manufacturers
 - Using modern protocol, currently used \rightarrow SpaceFibre
 - Configurable data-sinks and sources with variable packet data rate
 - Configurable link parameters, traffic criticality (QoS), ...
 - Observable link statistics, error-rate, signal-integrity
- 2. Evaluate the testbed by trying to emulate a realistic data handling unit
 - SpaceFibre router as example system providing high-speed data sources/sinks
 - Design-time configurable routing matrix further improves SWaP parameters

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Optical transceivers (for space)



• Broad selection of transceivers viable for future missions, ranging from COTS to fully qualified components









Product	DataStar SPACE	LightAble / SpaceAble	OptoFire	FireFly
Manufacturer	Glenair	Smiths Interconnect (former: Reflex Photonics)	APITech	Samtec
Туре	RHBD	COTS/RHBD	RT	COTS
No. channels	4 (full-duplex)	4 (full-duplex) 12 (half-duplex)	4 (full-duplex)	4 (full-duplex) 12 (half-duplex)
Link-rate	10Gbit/s	10 or 28 Gbit/s	10 Gbit/s	10 or 28 Gbit/s
Radiation Tests	Proton, TID, Heavy-Ion	Proton, TID, Heavy-Ion	?	TID

SpaceFibre Optical Transceiver Testbed

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Demonstrate SpaceFibre link(s) over optical transceivers and verify performance

Setup

- Two FPGA board setup with Xilinx Kintex UltraScale development kits:
 - HTG-K800 (XCKU060): Data-Generator
 - KCU105 (XCKU040): Loopback
- Smiths Interconnect LightAble 10G LM series as FMC add-on card
 - Up-to 12 channel 10 GBit/s full-duplex configuration (separate TX/RX)
 - 1 meter of OM3 ribbon-fiber (up-to 300 meter is possible)



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SpaceFibre Optical Transceiver Testbed: FPGA design

- FPGA design was developed based on previous SpFi lab activities
 - → re-uses SpFi Port IP core (ESA IP-Core library/Cobham Gaisler), data generator and configuration IPs
- Design in a nutshell
 - 8 separate SpFi ports with 3 virtual channels
 - Connected to SerDes macro configured with 8 TX/RX pairs in single-lane mode
 - Both boards run nearly identical designs, loop-back or data generator



SpaceFibre Optical Transceiver Testbed: Evaluation



- Synthesis and Implementation with Vivado 2020.1
 - Different virtual channel configurations (1, 2 and 3 virtual channels)
 - Recorded resource utilization, timing and power consumption estimation
- Bit-error rate calculation by enabling data generation and monitoring lane state through UART interface
 - Developed GRMON drivers and scripts to aid this process

grmon3> spfi::print_lane_error_summary								
	Lane-04	Lane-00	Lane-05	Lane-(
rx_err_cnt	0	0	0					
retry_cnt	0	0	0					
too_many_errors	0	0	0					
rx_err_cnt_ov	0	0	0					
far_end_los	0	0	0					
timeout	0	0	0					
far_end_standby	0	0	0					
far_end_reset	0	0	0					
seq_err	0	0	0					
crc8_err	0	0	0					
crc16_err	0	0	0					
frame_err	0	0	0					
protocol_error	0	0	0					
fe_cap	7	7	7					
fe_los_cause	0	0	0					

grmon3> spfi::print_datagen_status															
		VC 00	L	VC 01	L	VC 02	L	VC 03	L	VC 04	L	VC 05	L	VC	
	- 1				L		L		L		L				
<pre>tx::bw_cnt_last</pre>	:	95.5%	L	0.0%	L	0.0%	Ι	0.0%	L	0.0%	L	0.0%	1	0.	
<pre>rx::bw_cnt_last</pre>	:	0.0%	L	0.0%	L	0.0%	L	95.5%	L	0.0%	L	0.0%		0.	
rx::err_cnt		0		0	L	0	L	0	L	0	L	0			
rx::eep_cnt		0	L	0	L	0	Ι	0	L	0	L	0			
		BC													
			- 1												
<pre>tx::bw_cnt_last</pre>		0.0%	5												
<pre>rx::bw_cnt_last</pre>		0.0%	5												
rx::late_cnt		0													
rx::err_cnt		0													
rx1::delayed_cr	nt	0													

SpaceFibre Optical Transceiver Testbed: Results



- Recorded for the XCKU060
 - Utilization

	LUTs	FFs	BRAM
SpFi Port IP (1 VC)	3227 (0.97 %)	1931 (0.29 %)	3 (0.14 %)
SpFi Port IP (3 VC)	3645 (1.10 %)	2364 (0.36 %)	8 (0.37 %)
System Total	39023 (11.8 %)	30666 (4.62 %)	64 (2.96 %)

Power Consumption

[W]	Optical Engine	SpFi Codec	SERDES	Total
One Link	~0.1	0.047	0.203	0.353
System	~0.8	0.376	1.627	2.168 (excl. static)



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SpaceFibre Optical Transceiver Testbed: Results (2)



- Timing
 - SpFi port IP (and system AHB bus) is clocked with SerDes TX clock
 → 10 Gb/s / 40 bit = 250 MHz
 - Timing achieved with 0.002 ns WNS, 0.004 ns WHS
 - Critical path in data-generator
- Bit-Error Rate (BER)
 - Test-setup ran full-bandwidth test for approx. 24 hours (TBC)
 → 0 errors
 - 8 lanes * 10 Gbit/s * 24h * 60 min * 60 sec = 6912 Tbit transferred
 - System BER < 1e-15 with 99.9% confidence level

$$CL = 1 - e^{-N \times BER_s} \times \sum_{k=0}^{E} \frac{(N \times BER_s)^k}{k!}$$



Design-Time Configurable SpaceFibre Router



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Design-Time Configurable SpaceFibre Router



Goal: Emulate a realistic on-board data-handling unit with high-speed data sinks/sources

- Design-time configurable
 SpaceFibre Router
 - Configurable network topology → minimal, generated implementation
 - Improved isolation and security guarantee
- Implement design-time configurable SpaceFibre router for realistic example system with optical transceiver testbed



SpaceFibre Router: Routing Switch Specification



- Standard specifies routing switch components
- General implementation: Switch matrix, routing table, configuration node
 - Often, not all features are used
 - Overhead in implementation
 - Easy to introduce errors

Idea: Use the configurability of an FPGA to bake the switching configuration into the fabric

ECSS-E-ST-50-11C: Fig 5-55: Components of a SpaceFibre Routing Switch



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SpaceFibre Router: Switch configuration file



Model routing switch configuration using a description file (YAML)

<pre>prts: # The first part in the list is reserved for configuration of the router name: config params: mane: bbc params: mame: bbc mame: bbc mame: mmu params: mame: mmu params: mame: mmu params: mame: norman mame: instr_1 mame: instr_2 mame: instr_4 mame: instr_2 mame: instr_2 mame: instr_2 mame: instr_2 mame: instr_2 mame: instr_2 mame: instr_1 mame: instr_2 mame: instr_2 mame: instr_1 mame: instr_2 mame: instr_1 mame: instr_1 mame: instr_1 mame: instr_2 mame: instr_1 mame: instr_2 mame: instr_1 mame: instr_1 mame: instr_2 mame: instr_1 mame: instr_2 mame: instr_1 mame: instr_2 mame: instr_2</pre>	name: sfr_sample_system	# Virtual Network description
<pre>ports:</pre>		virtual nets.
<pre> name: config name: config params: name: obc name: nobc name: no</pre>	ports:	
<pre>- name: config - params: - name: obc - params: - name: obc - params: - name: obc - params: - name: mmu - name: processing: - name: instr_1: - name: instr_1 - name: instr_1 - name: instr_1 - name: instr_1 - name: instr_1 - name: instr_2 - name: instr_1 - name: instr_2 - name: instr_1 - name: instr_1 - name: instr_1 - name: instr_1 - name: instr_2 - name: instr_1 - name: instr_2 - name: instr_2 -</pre>	\cdots # The first port in the list is reserved for configuration of the router	name, command
<pre>d gtob_index: 0 gtob_inde</pre>	- name: config	- Indine: Command
<pre>port ve_map:</pre>	params:	gtob_index: 0
<pre> name: obc params: name: mmu name: mmu name: mmu name: mmu name: mmu name: mmu name: processing name: instr_1 name: instr_1 name: instr_2 name: instr_2 name: instr_2 name: instr_2 name: transmit name: transmit</pre>	····NumVc: 1	port_vc_map:
<pre>>> obc: 0 >>> obc: 0 >>> obc: 0 >>>> obc: 0 >>>> obc: 0 >>>> obc: 0 >>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>></pre>	- name: obc	config: 0
<pre>>- name: mu params: name: processing 0 instr_1: 0 instr_2: 0 instr_2: 0 instr_2: 0 instr_1: 0 instr_2: 0 instr_1: 0 instr_2: 0 instr_2: 0 instr_1: 0 instr_2: 0 instr_1: 0 instr_2: 0 i</pre>	···· params:	·····obc: 0
<pre>name: muu params: processing: 0 process</pre>	·· ··NumVc: 2	······································
<pre>params: - name: processing - name: processing - name: instr_1 - name: instr_1 - name: instr_1 - name: instr_2 - name: transmit - name: transmit</pre>	name: mmu	····processing: 0
<pre>/* name: processing ** name: processing ** name: processing ** name: instr_1 ** name: instr_1 ** name: instr_2 ** name: transmit ** name: transmit</pre>		instr_1: 0
<pre>name: processing processing</pre>	para processing	···instr_2: 0
<pre>promotions: </pre>	in alle: processing	····transmit: 0
<pre>/ Tomme: instr_1 // params: // NumVc: 2 // params: // NumVc: 3 // NumVc: 2 // Params: // NumVc: 2 // Params: //</pre>	parains.	connections:
<pre>what is the global address map used for generating the address decoding # Path addressing is generated by port index if the vc has it enabled addr_map logic: ************************************</pre>	- name: instr 1	····· from port: config
<pre># This is the global address map used for generating the address decoding # This is the global address map used for generating the address decoding # Path addressing is generated by port index if the vc has it enabled addr_map_logic: ************************************</pre>	params:	····to ports: [obc]
<pre></pre>	·····NumVc: 2	addr type: ['path']
<pre></pre>	- name: instr 2	- from port: obc
<pre></pre>	params:	to ports: [config, mmu, processing, instr 1, instr 2, transmit]
<pre>>- name: transmit >- params: >- NumVc: 2 # This is the global address map used for generating the address decoding # Path addressing is generated by port index if the vc has it enabled addr_map_logic: >- 32 ·: obc >- 33 ·: obc >- 33 ·: obc >- 35 ·: obc</pre>	····NumVc: 3	
<pre># This is the global address map used for generating the address decoding # This is the global address map used for generating the address decoding # Path addressing is generated by port index if the vc has it enabled addr_map_logic: </pre>	- name: transmit	- from port: mmu
<pre>// / · NumVc: 2 // This is the global address map used for generating the address decoding // Path addressing is generated by port index if the vc has it enabled addr_map_logic: // addr_type: ['path'] // addr_type: ['path']</pre>	····params:	to ports: [obc]
<pre># This is the global address map used for generating the address decoding # Path addressing is generated by port index if the vc has it enabled addr_map_logic:</pre>	····NumVc: 2	addr type: ['path']
<pre># This is the global address map used for generating the address decoding # Path addressing is generated by port index if the vc has it enabled addr_map_logic:</pre>		- from port: processing
<pre># Path addressing is generated by port index if the vc has it enabled addr_map_logic: addr_type: ['path'] from_port: instr_1 </pre>	# This is the global address map used for generating the address decoding	to norts: [obc]
addr_map_togic: addr_type: path >32 ·: obc from_port: instr_1 >33 ·: obc to_ports: [obc] >34 ·: obc from_port: instr_2 >35 ·: obc from_port: instr_2	# Path addressing is generated by port index if the vc has it enabled	addr type: ['math']
32 : obc 33 : obc 34 : obc 35 : obc 35 : obc 36 : obc	addr_map_logic:	from port, instr 1
····································	22 · · · · · · · · · · · · · · · · · ·	interport. Instr_1
35 : obc - 35 : obc		adds type: [lpath]
- Trom_port: Instr_2	135 · · · obc	from port, instruct
		- irom_port: instr_z
40 ··· obc	40 · : obc	to_ports: [obc]
41 : processing	41 : processing	addr_type: ['path']
42 : processing	······································	- from_port: transmit

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SpaceFibre Router: HDL Code Generation



Generate with Python the HDL instantiation and connections between modules



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SpaceFibre Router: Broadcast Mechanism



System to quickly get small messages to all nodes in a SpaceFibre network

- Transfer broadcast messages (BCM)
- Prevent broadcast storms → Timeout
- Drop outdated BCM
- Enable/disable individual ports (filter)



SpaceFibre Router: Validation



- UVM testbench with random packet stimuli generation
 - Virtual channel switch matrix: generated, post simulation validated
 - Broadcast mechanism: custom, scoreboard validation during simulation
- Hardware implementation in optical transceiver-testbed
 - Vivado 2020.1 for XCKU040 FPGA (loop-back side)
 - Two configurations implemented, designed with example system in mind
 - 5x5 fully-connected router with 3 virtual networks
 - 5x5 minimal router with 3 virtual networks
 - Implementation frequency 250MHz → 10GB/s for each virtual channel per port

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SpaceFibre Router: Evaluation



Utilization shows clear advantage of

optimized switch-matrix

(a) Optimized

Block	LUT	FF	BRAM			
Switch	3622 (1.5 %)	4749 (1.0 %)	0 (0.0 %)			
Broadcast	1187 (0.5%)	2501 (0.5 %)	0 (0.0 %)			
Codecs	19710 (8.1 %)	13932 (2.9 %)	34 (5.7 %)			
Total	24802 (10.2 %)	22110 (4.6 %)	34 (5.7 %)			
(b) Fully connected						
Block	LUT	FF	BRAM			
Switch	17740 (7.3%)	24900 (5.1 %)	0 (0.0 %)			
Broadcast	1158 (0.5%)	2501 (0.5%)	0 (0.0 %)			
Codecs	27272 (11.3 %)	20487 (4.2 %)	66 (11.0 %)			
Total	46492 (19.2 %)	48816 (10.1 %)	66 (11.0 %)			

• Power estimation [W]

	Block						
Variant	Switch Matrix	Broadcast	Codecs	Total			
Fully Connected Optimized	0.18 0.05	0.02 0.02	0.78 0.41	0.98 0.49			



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Summary



- Optical transceiver testbed in a nutshell
 - 10 Gbit/s data-rate achieved with up-to 3 virtual channels, 8 links \rightarrow 80 Gbit/s system data-rate
 - Utilizes ~1% of LUTs, 0.36 % of FFs and 0.37% of BRAM per channel
 - Consumes ~0.35W of power including SerDes and transceiver per link
 - System BER < 1e-15 with 99.9 % confidence level
- Design-time configurable SpaceFibre Router
 - Successfully demonstrated a realistic high-speed data-handling unit in optical transceiver testbed
 - 10 Gbit/s data-rate achieved with 5x5 fully-connected/optimized network
 - Utilizes ~10% of LUTs, ~5% of FFs and BRAMs overall (optimized)
 - Consumes <1 W of power (w/o SerDes) (optimized)
 - Validation and evaluation of design-time tailoring shows significant advantage
 - Utilizes 0.5x the resources and power on average when compared to fully connected switch



Backup Slides



SpaceFibre Router: Summary & Outlook



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- Done: HDL generator for the switching fabric
 - Broadcast mechanism
 - RTL functional tests
 - KU040 implementation
- Next: Integration of the broadcast mechanism into the KU040 demonstrator
 - End-to-End system HDL generation
 - Optional feature implementation
 - Dedicated router configuration node for status
 - Group adaptive routing
 - Packet multicast

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SpaceFibre Optical Transceiver Testbed - Background

SpaceFibre

- Successor protocol to SpaceWire, packet-level compatible
- Built-in FDIR and QoS on protocol level
- Variable data-rates up-to 10 Gbit/s depending on cabling used even more with multi-lane implementations
- Smith Interconnect (former Reflex Photonics) LightAble series Transceivers
 - Industrial optical transceiver based on 850 nm multi-mode laser
 - Up-to 10 Gbit/s per channel, available in 4+4 ch. full-duplex and 12 ch. half-duplex configurations
 - Low-power consumption: <100 mW per channel
 - Space-qualified versions (SpaceAble series) available (>100 kRad TID, heavy-ion and proton results available)







SpaceFibreRouter: Broadcast Table





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