Simulation and hardware validation of SerDes links for SpaceFibre

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SpaceFibre compliance testing

SpaceFibre is a high-speed protocol for on-board spacecraft application

- Data rate: up to 6.25 Gbps per lane (copper)
- SerDes based
- Compliance testing necessary for:
  - Front-panel connections
  - Backplanes, such as used in the Advanced Data Handling Architecture (ADHA)

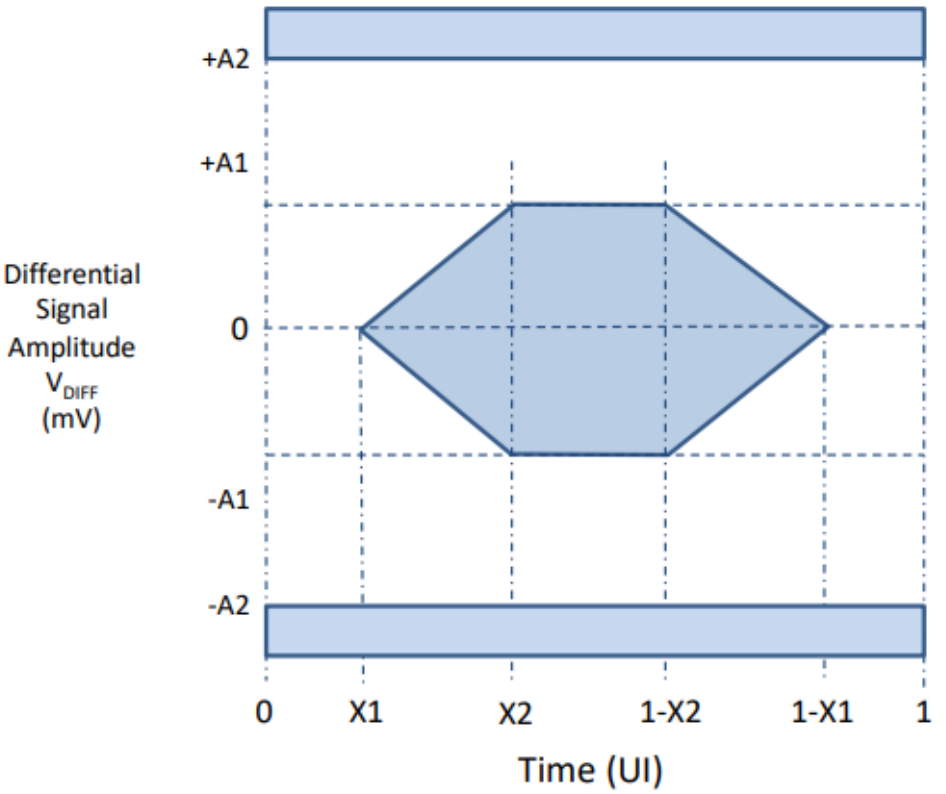


Figure 5-12: Serial eye pattern mask

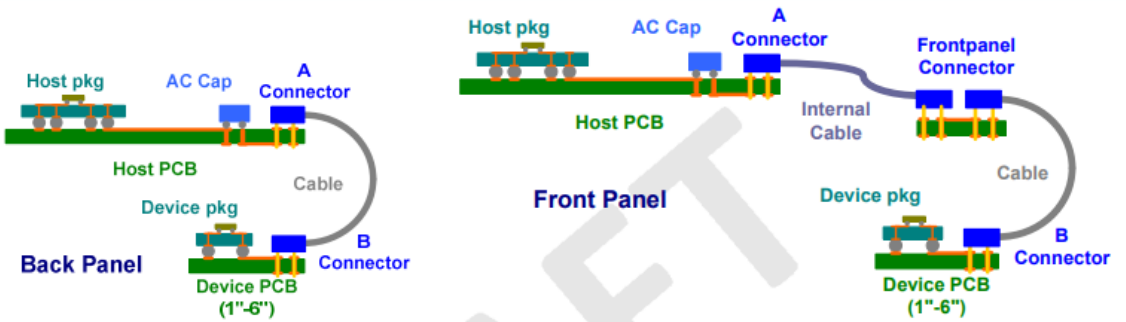
Source: *ECSS-E-ST-50-11C(15May2019)*

USB 3.0 compliance testing

- Data rate: 5Gbps
- SerDes based

The USB 3.0 Electrical Compliance Methodology:

- Describes the compliance values at the end of a compliance channel (including PCB routing, connectors and cables)
- Describes different patterns for testing different properties
- Different values for Random jitter (Rj), Deterministic jitter (Dj) and Total jitter (Tj) for both Tx and Rx are specified.
- For Tx testing, CTLE equalizer is simulated by the measuring equipment.



(a) Back panel port channel topology

(b) Front panel port channel topology

Figure 2. Example channels for front panel and back panel ports.

Source: *USB 3.0 Electrical Compliance Methodology*

DisplayPort 1.0 compliance testing

- Data rate: 10 Gbps
- SerDes based

VESA DisplayPort PHY Compliance Test Standard:

- Describes the test set-up with additional fixtures and requires its characterization before performing measurements.
- specifies different patterns for every test, some criteria are tested under only one pattern
- only considers total jitter (Tj)
- Describes different pass/fail values at different test points
- Defines signal attenuation of Rx signal at test points, and describes noise measurements (mainly focused on the cable properties)

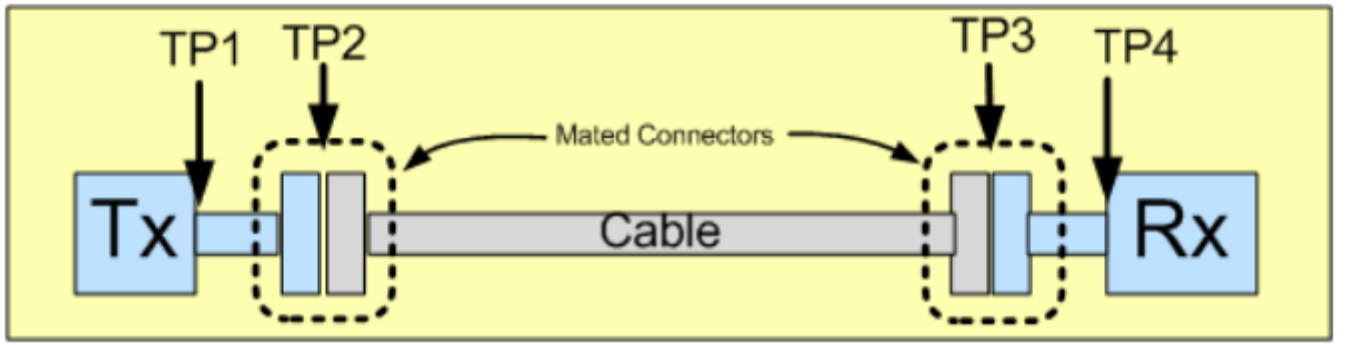


Figure 2-1: The Four Ideal Measurement Points in a DisplayPort Interconnect System

Source: *VESA DisplayPort PHY Compliance Test Standard*

HPCB board overview

High – Performance Compute Board

24 bidirectional HSSLs using FPGA SerDes ch.:

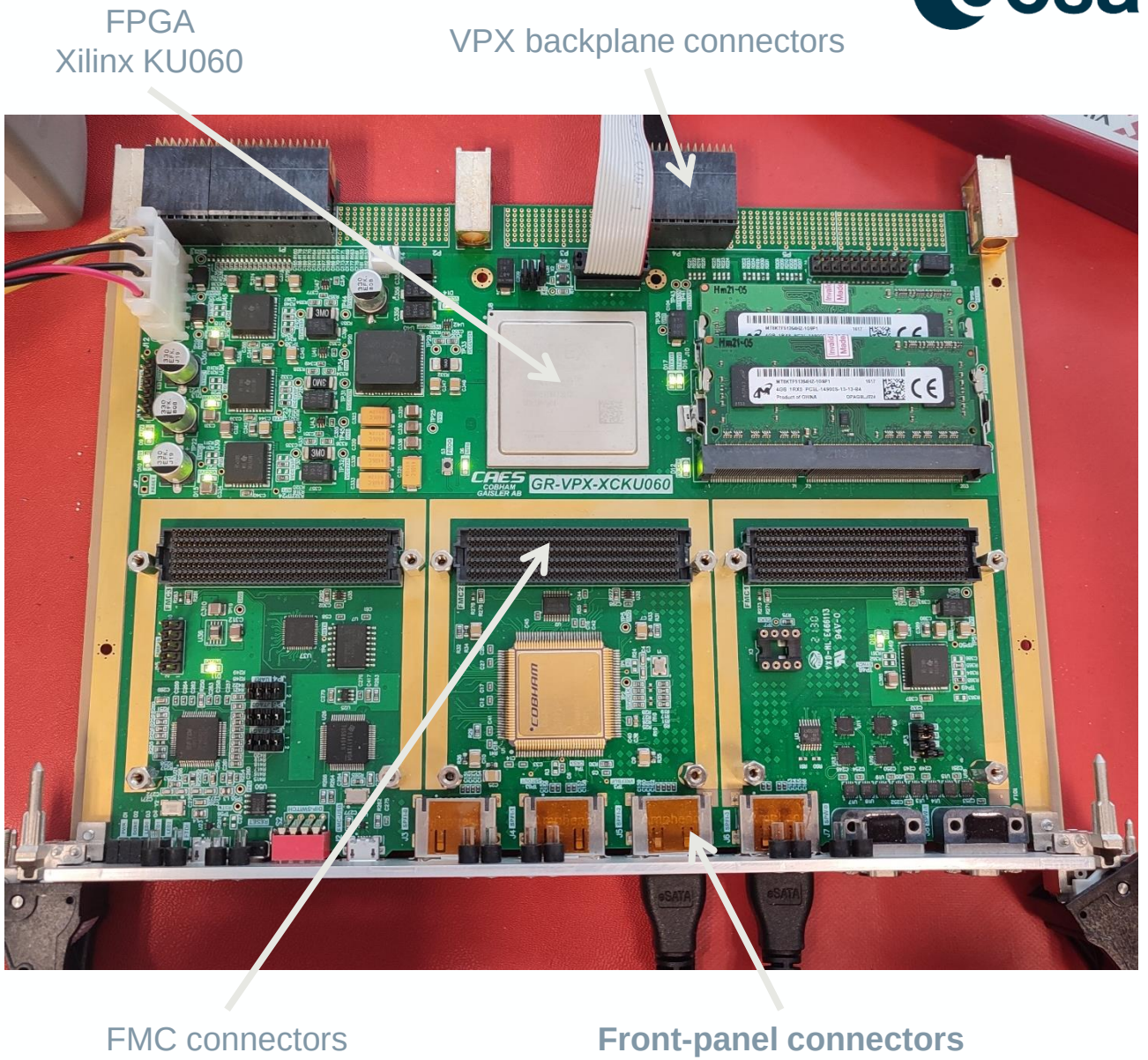
- front-panel connectors (4, eSATA)
- VPX backplane connectors (4+4)
- FMC connectors (4+4+4)

Data rate up to 6.25 Gbps per lane.

Two different RX-equalization settings (LPM, DFE).

FPGA - Field-Programmable Gate Array

HSSL – High Speed Serial Links

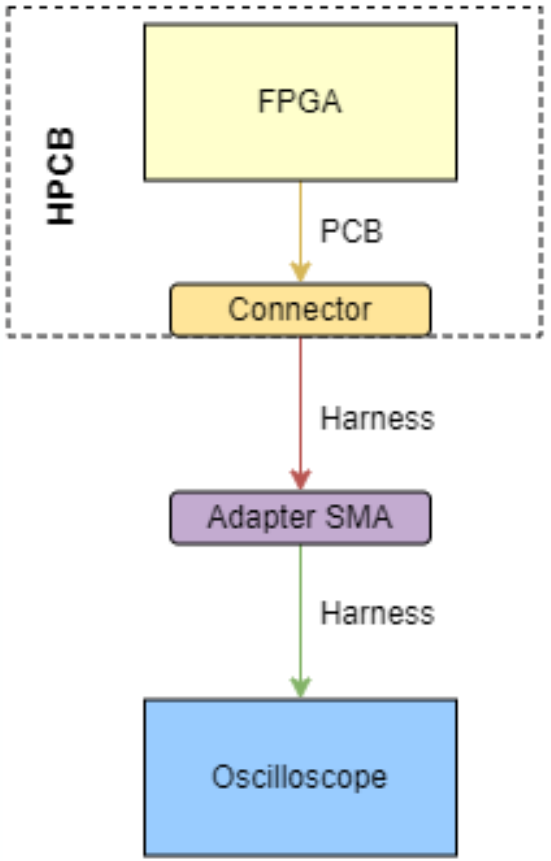


Test set-up

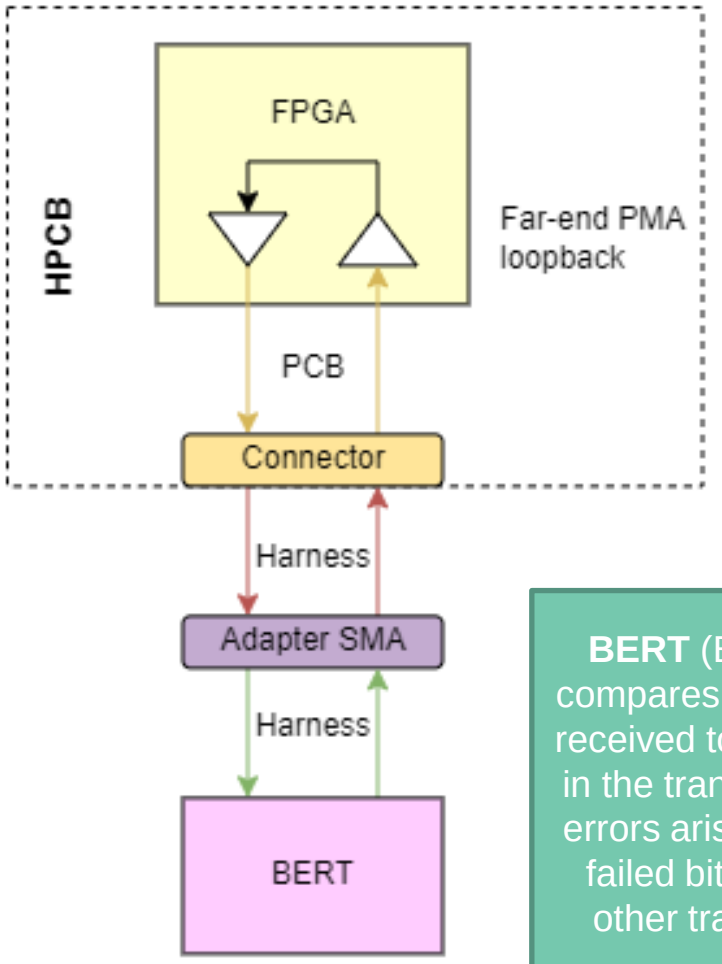
SerDes – serialiser-deserialiser

Source: *Wikipedia*

(A) Tx Testing



(B) Rx Testing



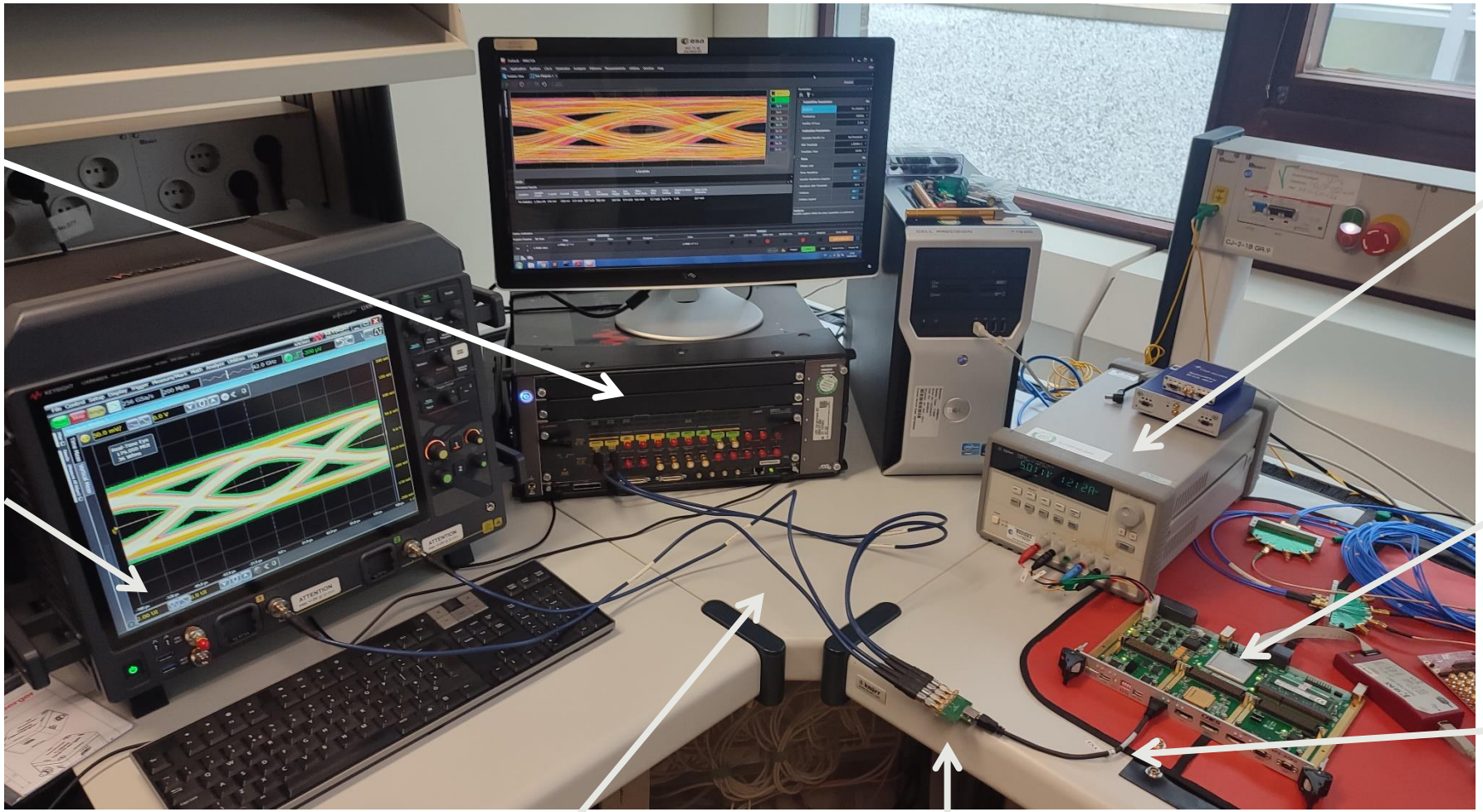
BERT (Bit Error Ratio Tester) - compares the ratio of the bit errors received to the total number of bits in the transmitted data stream. Bit errors arise from noise, distortion, failed bit synchronizations, and other transmission anomalies.

Source: *keysight.com*

Test set-up for transmitter testing

BERT
Keysight M8041A
8.5 Gb/s

Oscilloscope
Keysight UXR0402A
40 GHz, 256 GSa/s
Teledyne SDA 820Zi-B
20 GHz, 80 GSa/s



Power supply
Agilent E3631A

HPCB

SpFi cable
0.25 m
1 m
2 m
4 m

Laboratory: *ESA, ESTEC*

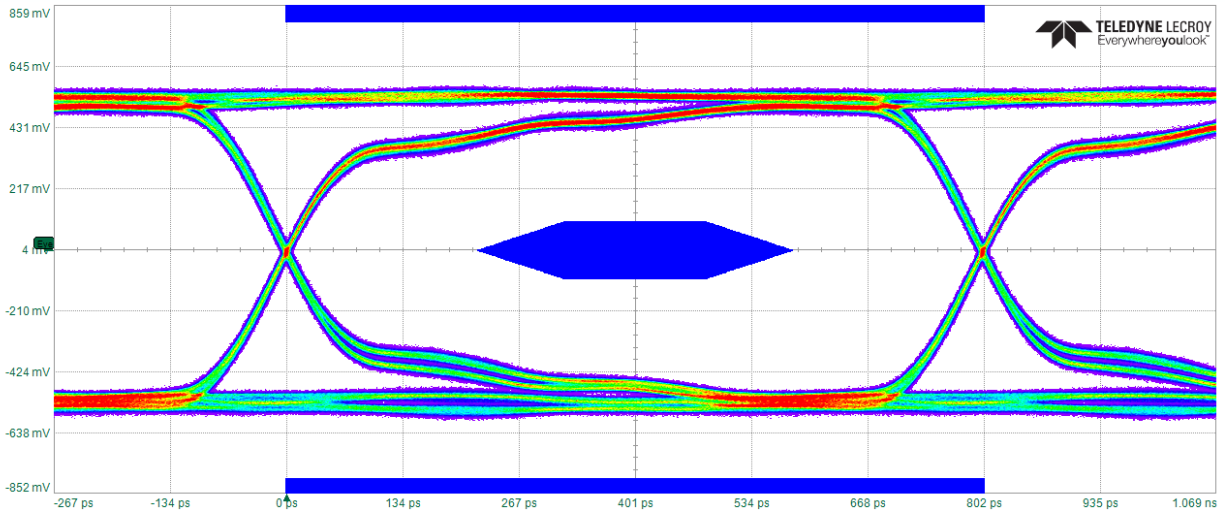
BNC cable
1 m

Connector swap
eSATA <-> BNC

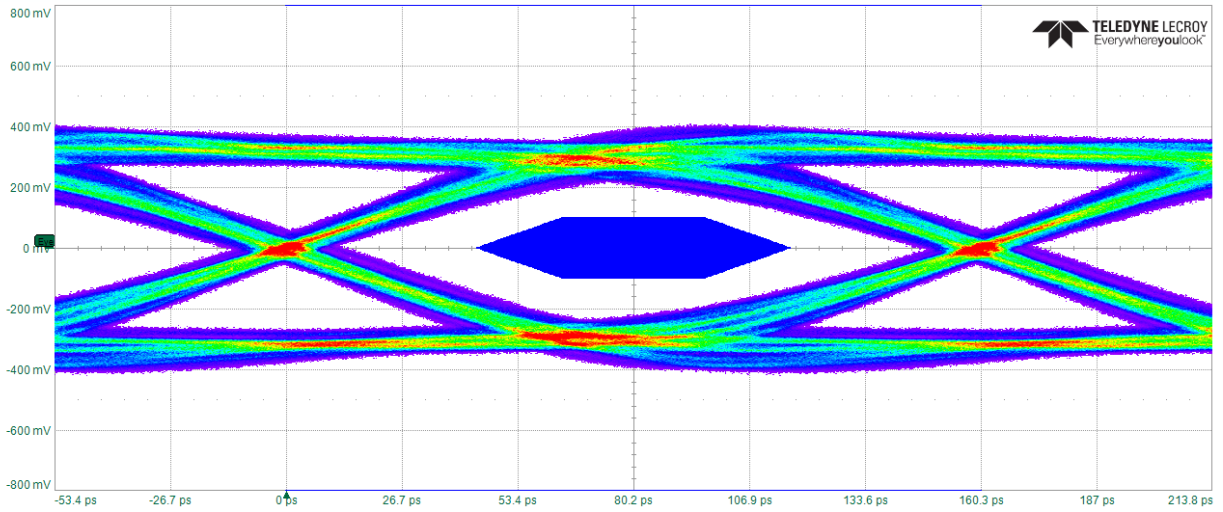
Transmitter test results

SerDes configuration: Voltage swing - 1080 mV, PRBS signal

Harness: 0.25 m cable

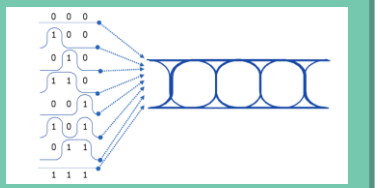


Data rate: 1.25 Gbps; Eye height: 782 mV



Data rate: 6.25 Gbps; Eye height: 383 mV

Eye diagram – Formed by overlaying of bit sequences



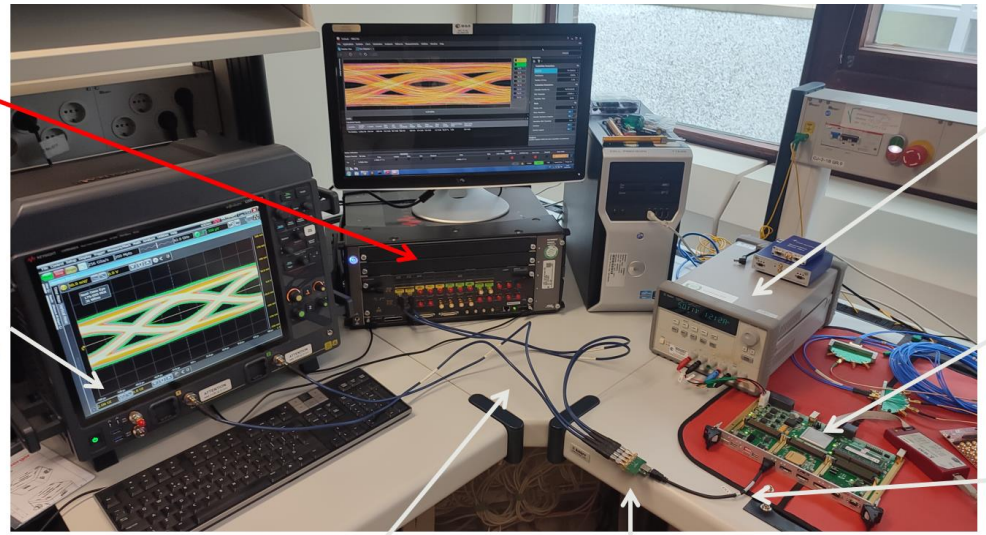
Source: *Textronic*

Jitter – “noise” in the time domain

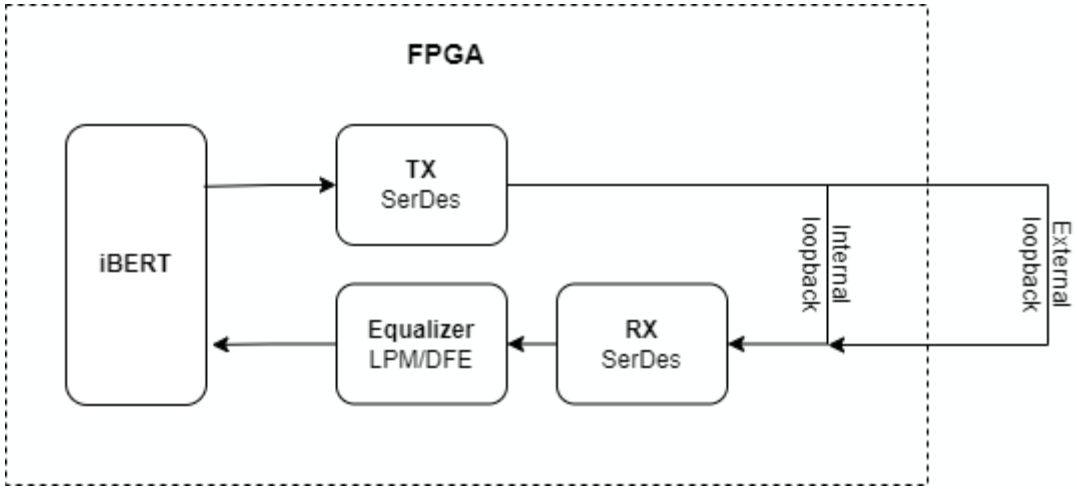
Test set-up for receiver testing

Two approaches:

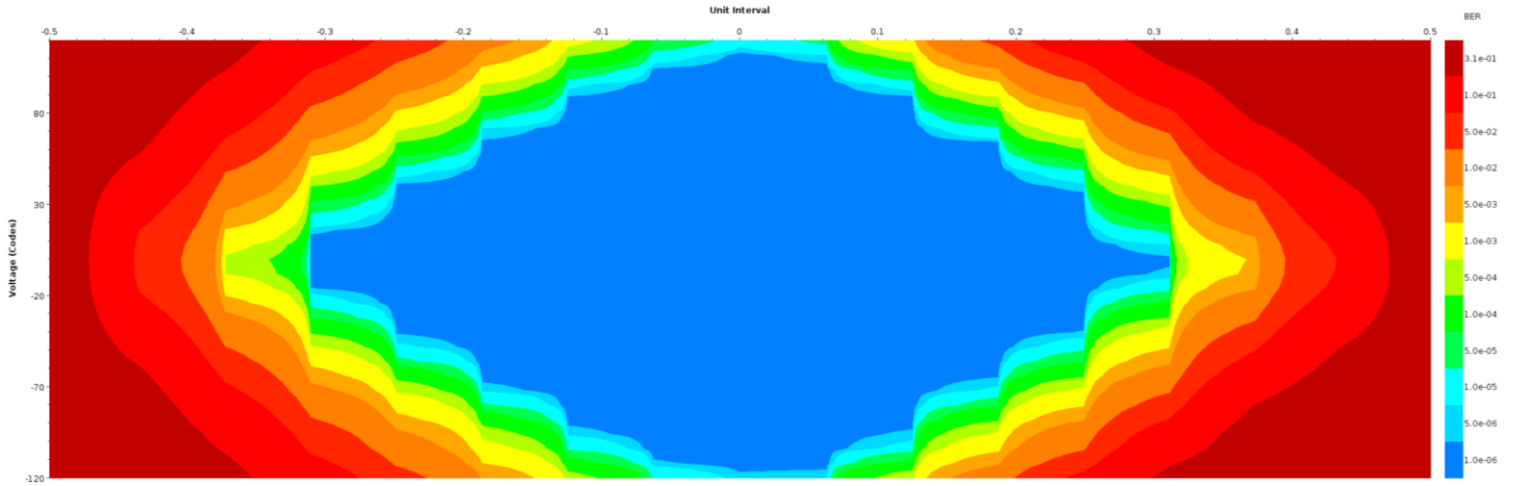
1) Signal from BERT looped back in the HPCB and checked by the oscilloscope



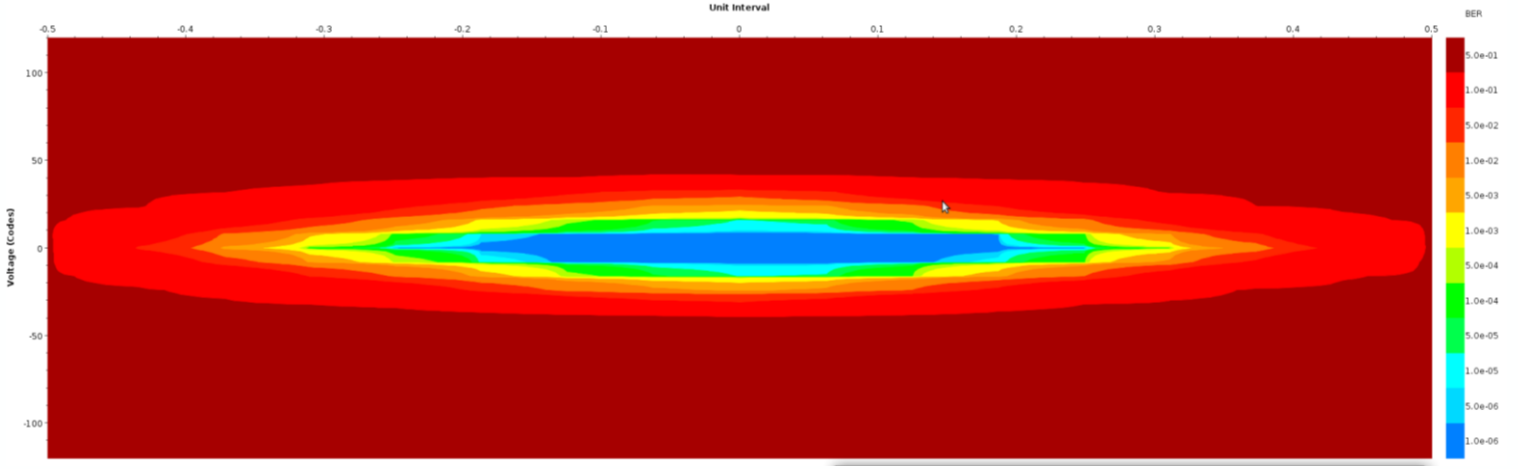
2) Self-diagnosis iBERT scan (eye diagram after equalization)



Receiver test results



Voltage swing: 1080 mV



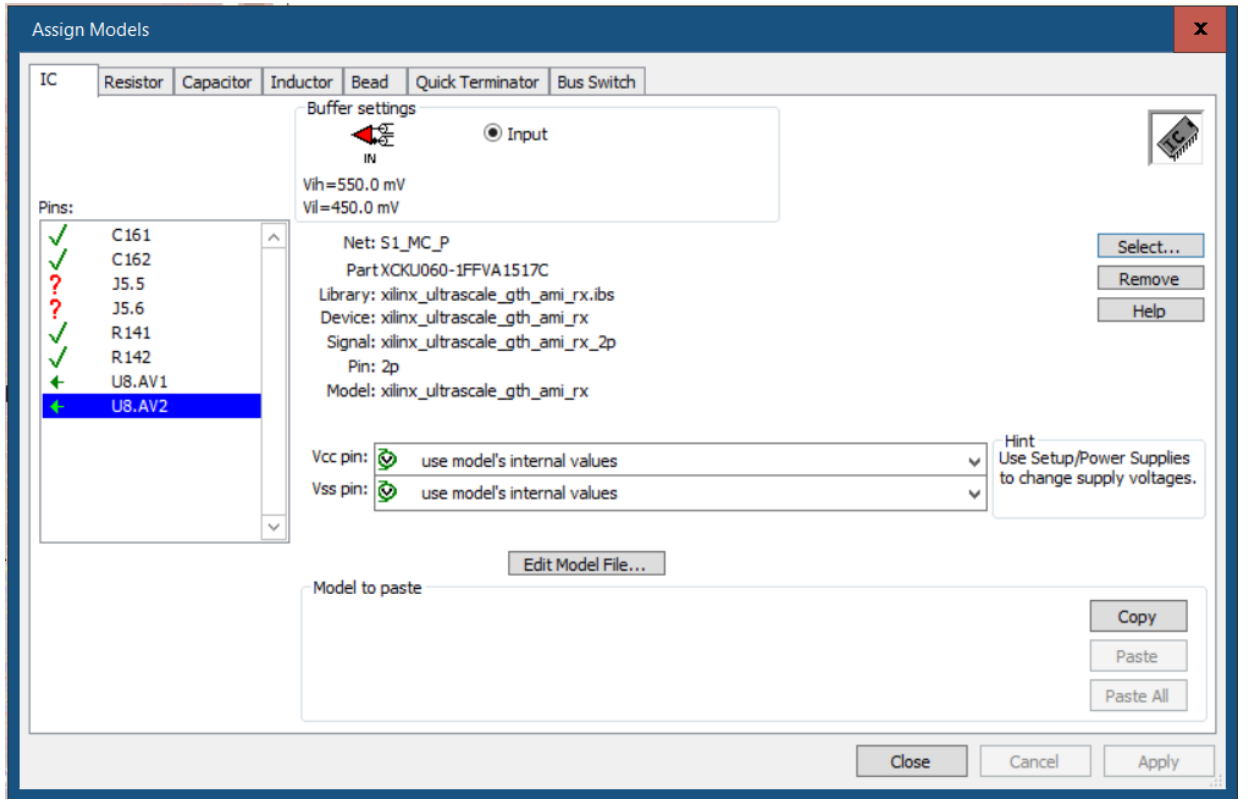
Voltage swing: 170 mV

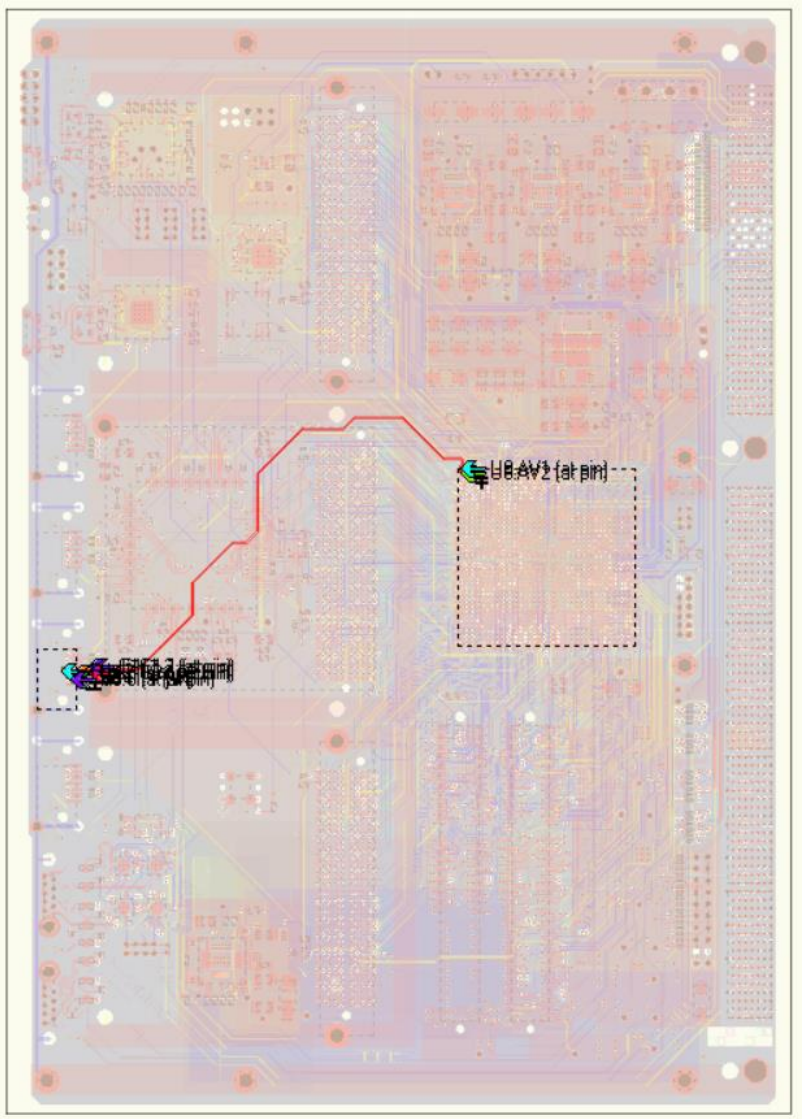
- PRBS signal from BERT
- Data rate: 6.25 Gbps
- Harness: 0.25 m cable
- Eye diagram measured after DFE equalizer
- PRBS checker**: 0 errors**

```
rmon3> spfi::print_lane_error_summary
               | Lane-00 | Lane-01 | Lane-02 | Lane-03 |
 ------------- | ------- | ------- | ------- | ------- |
 rx_err_cnt    |       0 |       0 |      78 |     139 |
 retry_cnt     |       0 |       0 |       0 |       0 |
 too_many_errors |       0 |       0 |       0 |       0 |
 rx_err_cnt_ov |       0 |       0 |       1 |       1 |
 far_end_los   |       0 |       0 |       0 |       0 |
 timeout       |       0 |       0 |       1 |       1 |
 far_end_standby |       0 |       0 |       0 |       0 |
 far_end_reset |       0 |       0 |       0 |       0 |
 seq_err       |       0 |       0 |       0 |       0 |
 crc8_err      |       0 |       0 |       0 |       0 |
 crc16_err     |       0 |       0 |       0 |       0 |
 frame_err     |       0 |       0 |       0 |       0 |
 protocol_error |       0 |       0 |       0 |       0 |
 fe_cap        |       7 |       7 |       0 |       0 |
 fe_los_cause  |       0 |       0 |       0 |       0 |
```

Simulation set-up

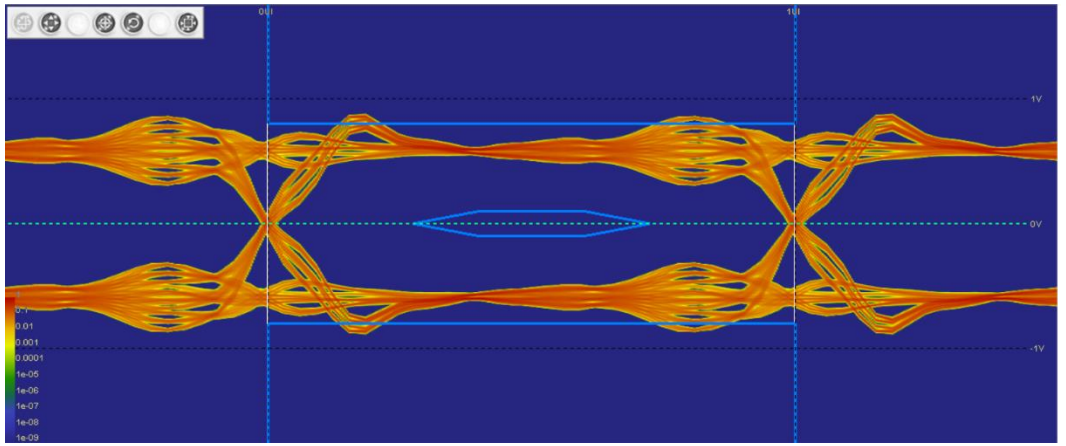
- Simulations were performed using Mentor HyperLynx software
- Xilinx UltraScale GTH IBIS and AMI models have been used



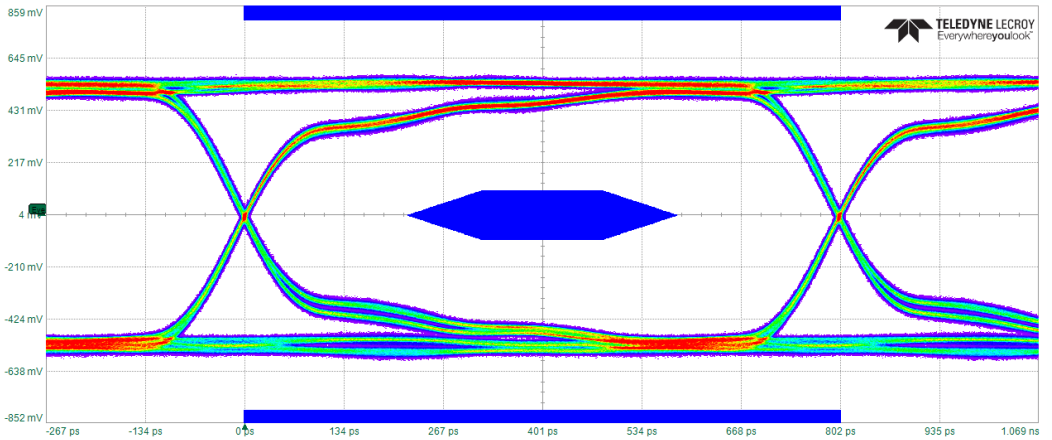


Simulation vs test results

Data rate:
1.25 Gbps
Voltage swing:
1080 mV

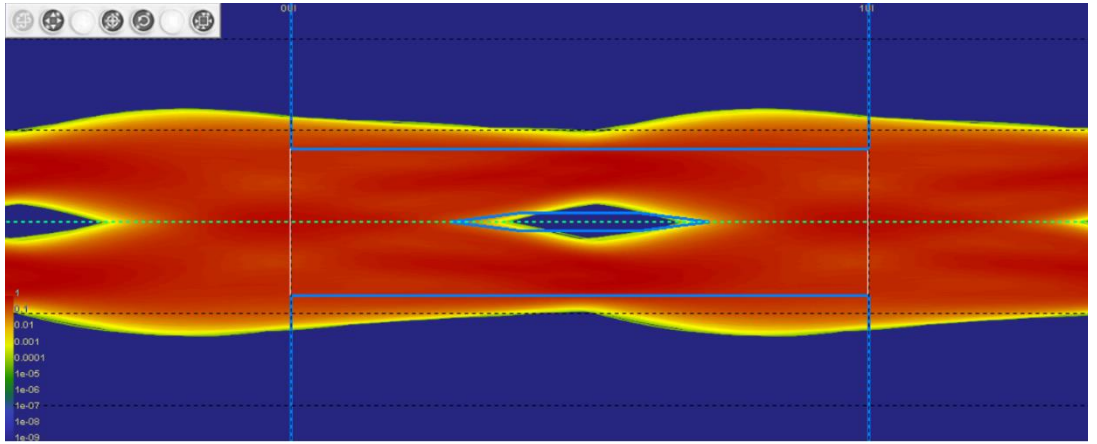


Eye height: 1007 mV

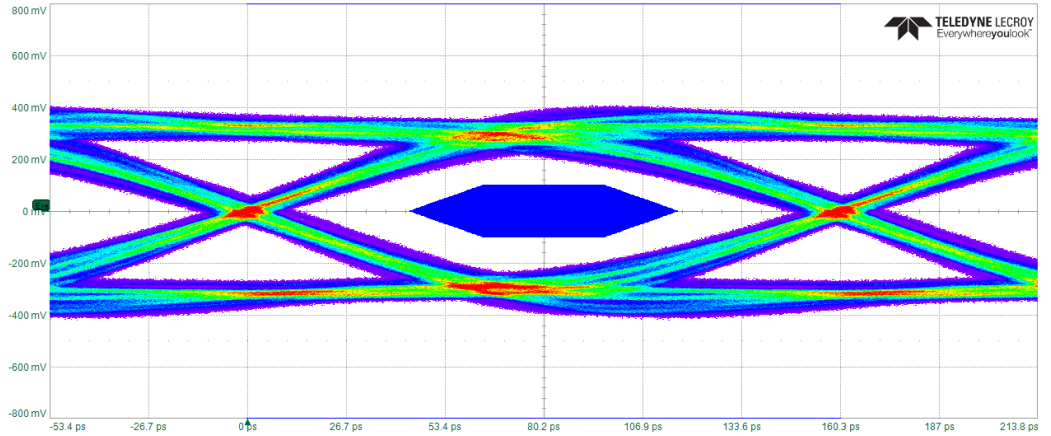


Eye height: 782 mV

Data rate:
6.25 Gbps
Voltage swing:
1080 mV



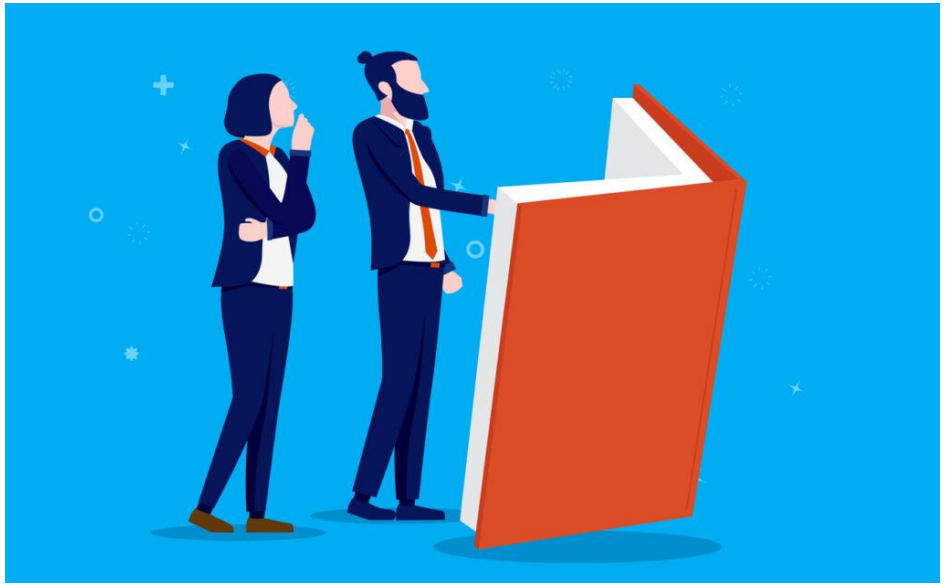
Eye height: 314 mV



Eye height: 382 mV

Future work

- Backplane connectors testing
- Optical testing
- Compliance Test Handbook similar to USB or DisplayPort for ADHA



Thank you for your attention!

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