



STAR-Dundee

20 Years of Spacecraft Networking Innovation

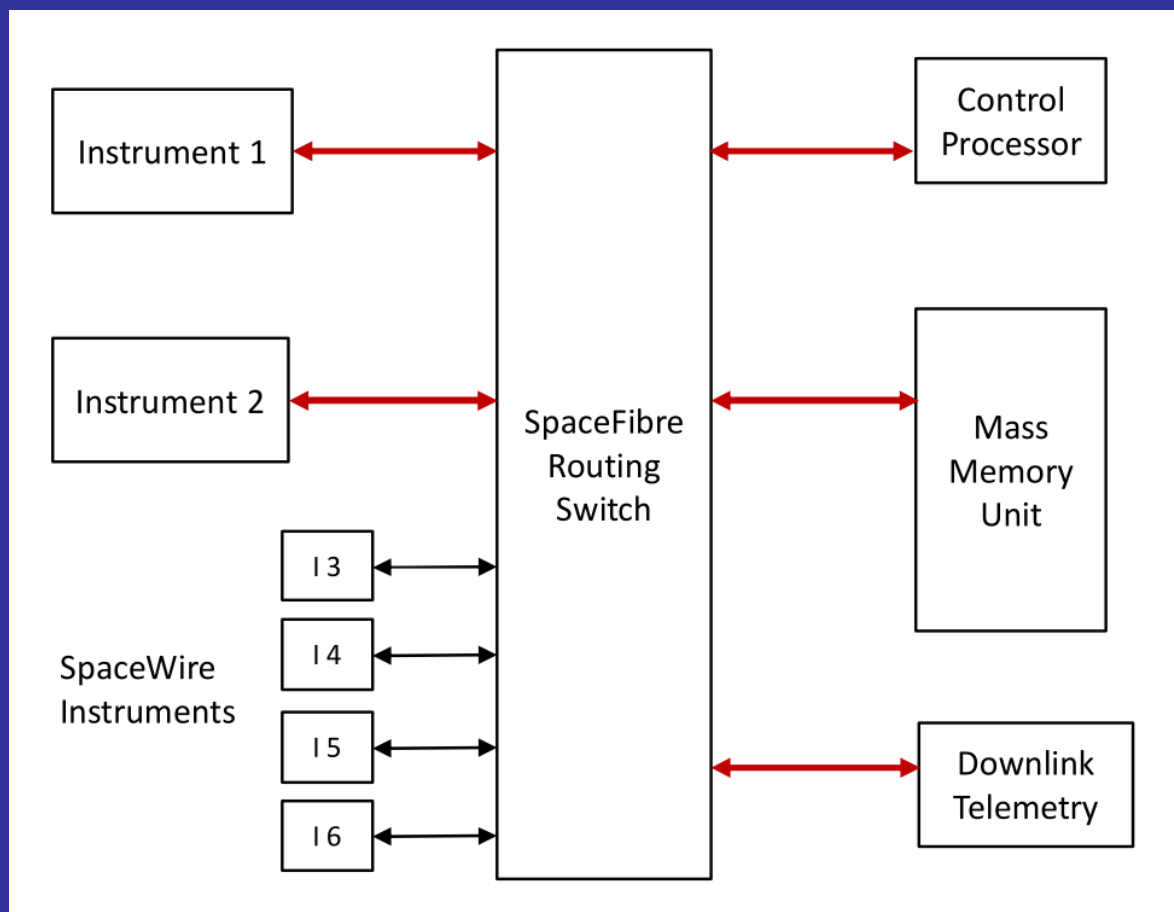
SpaceFibre Multi-Lane Routing Switch IP

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SpaceFibre Network

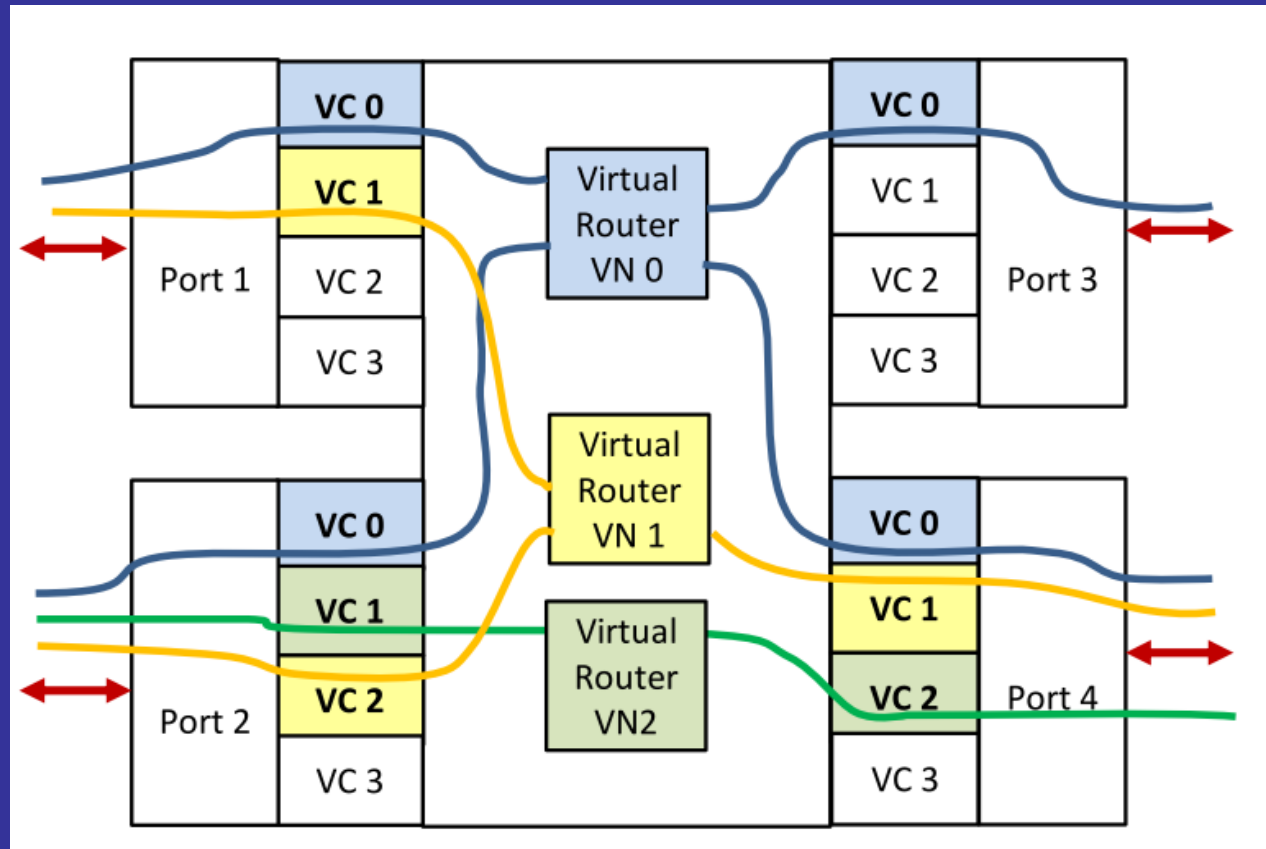


SpaceFibre links carries SpaceWire packets with much more functionality:

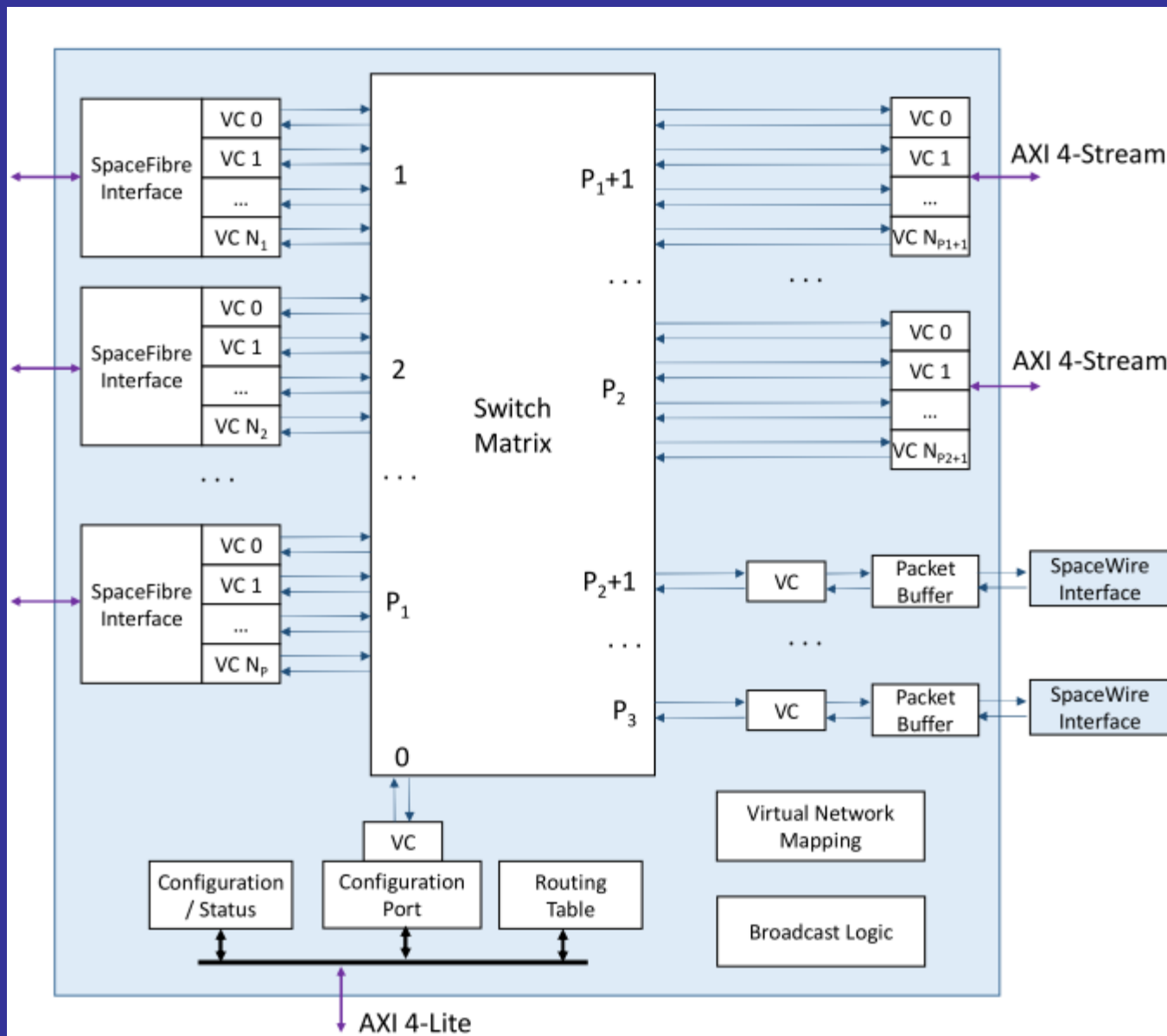
- Gigabit rates
- Multiple lanes
- Broadcast messages
- Reliable data transfer with error recovery
- virtual channels with QoS

SpaceFibre Virtual Networks

- A SpaceFibre Router IP implements a high performance SpaceWire Routing Switch for each virtual network defined.



Router Architecture



Routing Switch Features

- Technology independent (FPGA or ASIC) but optimised for radiation-hardened FPGAs.
- Configurable number of SpaceFibre, SpaceWire and internal AXI4-Stream ports.
- Configurable SpaceFibre lane rate, number of lanes, and number of virtual channels per port.
- Configurable target technology (RTG4, PolarFire, Xilinx Kintex/UltraScale/Versal, generic) for memory blocks and Serdes interface.
- Up to 64 virtual networks that can be statically or dynamically configured.
- Router configuration registers can be accessed via a configuration port using RMAP or using a dedicated AXI interface.

Routing Switch Features (2)

- High performance, full non-blocking switch matrix with deterministic switching latency. Virtual Networks do not share any switching resources.
- Round-robin arbitration with watchdog timeout for packets in the same virtual network requesting the same output port.
- SpW/SpFi network capabilities such as path and logical addressing with a routing table.
- Up to 256 broadcast channels with higher priority for time-critical broadcast messages.
- Simple and efficient integration with SpaceWire networks using SpaceWire packet buffers and automatic SpW to SpFi broadcast translation.
- Internal timer tracks time being distributed over the network.

Routing Switch Configuration

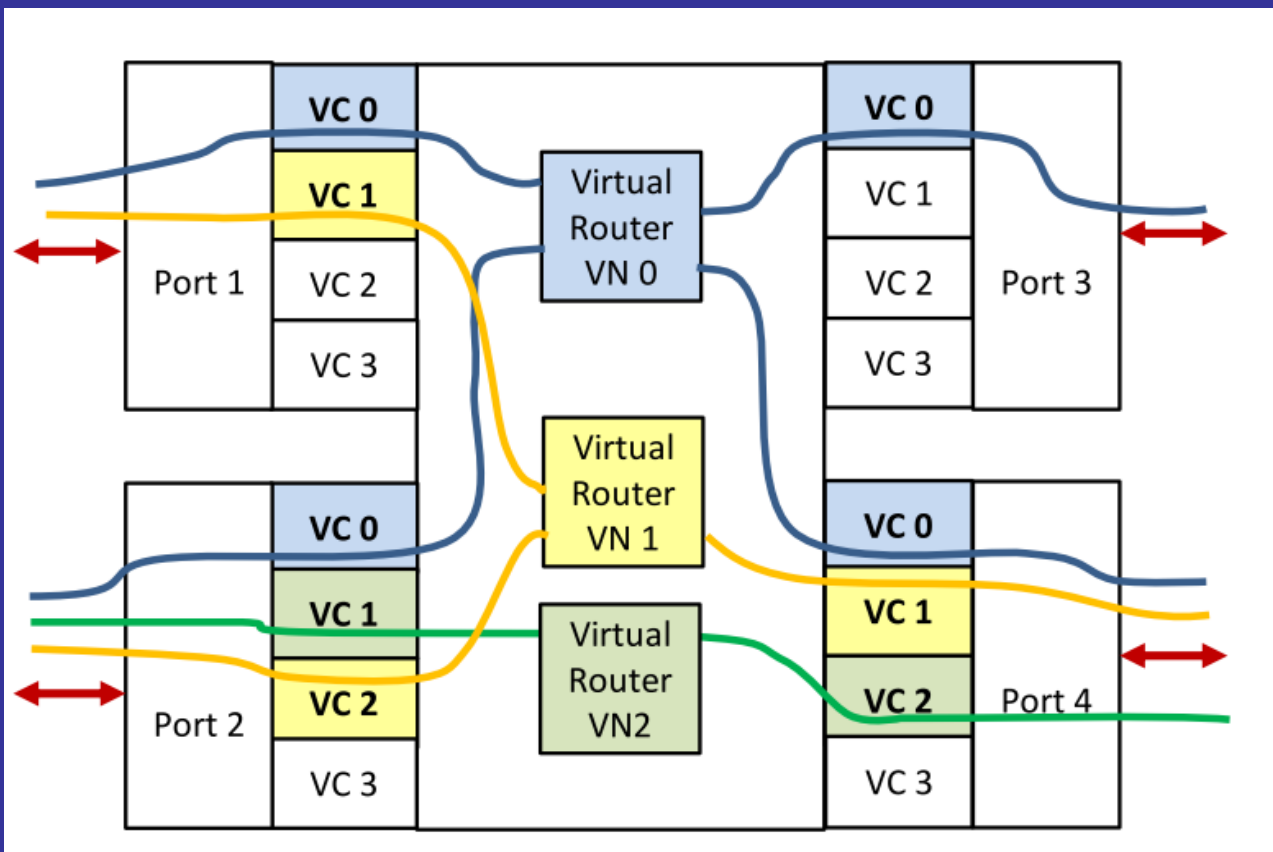
- Static VHDL parameters (before Synthesis)

- Target technology
- Number and type of ports (SpW, SpFi, AXI)
- Number of Lanes
- Lane rate
- VCs per port
- Default value of the routing table
- Virtual Network setup

- After Power-On

- Memory map accessible via:
 1. Port 0 with RMAP
 2. AXI4-Lite internal bus (for embedded CPU)

Virtual Network Configuration



VN number	Virtual channel number			
	Port 1	Port 2	Port 3	Port 4
0	0	0	0	0
1	1	2	-	1
2	-	1	-	2

Memory Map

Region																	Start
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Legacy support	0	0	Reserved														0x0
Device Information	0	1	0	0	0	0	0	Register Select									0x4000
Routing Table	0	1	0	0	0	0	1	Logical Address							Sel	0x4200	
Network Management	0	1	0	0	0	1	0	Register Select									0x4400
Broadcast Notification	0	1	0	0	0	1	1	Register Select									0x4600
Device Specific	0	1	1	Register Select												0x6000	
VC Information	1	Port Number					0	VC Number				Register Select				0x8000	
Port Information	1	Port Number					1	0	0	Register Select						0x8200	
Link Information	1	Port Number					1	0	1	Register Select						0x8280	
Lane Information	1	Port Number					1	1	0	Lane Number				Regs Select			0x8300
Reserved	1	Port Number					1	1	1	Reserved						0x8380	

Packet Addressing

- First byte of each received packet is the packet address.
 - Determines the destination port using logical or path addressing
 - Virtual channel within the destination port is determined by the Virtual Network
- Path addressing supports:
 - Leading Fill characters
 - Path address is replaced by a Fill character.
 - Path address removal when not leading fill is present

Source	1st Hop	Destination
01 02 FE 10 11 12 13 14	02 FE 10 11 12 13 14 15	FE 10 11 12 13 14 15 16
∅ ∅ 01 02 FE 10 11 12	∅ ∅ ∅ 02 FE 10 11 12	FE 10 11 12 13 14 15 16

SpaceWire Packet Buffers

- Each SpW port has:
 - A Packet Buffer on its receive side.
 - A FIFO Buffer on its transmit side.

- Packet Buffer:
 - Buffers packets arriving over the SpW port. It only forwards full packets to the SpFi VN.
 - The VC sending the SpW packet is not held up by the slower SpW interface.
 - If the incoming packet is larger than the size of the Packet Buffer there is a configurable option to spill the remaining of the packet.

- FIFO buffer:
 - Does not hold the full packet so it supports any packet size.

Watchdog Timeout Mechanism

- Packet blocking in a Virtual Network does not affect packets in another Virtual Network:
 - However, within the same Virtual Network, package blocking can still occur.
- Causes of packet blocking:
 - Source stalls and stops transmitting bytes of a SpW packet while the packet is being routed.
 - Destination stalls and stops receiving bytes of a SpW packet while the packet is being routed.
 - A package is blocked due to another packet being blocked.
 - This can only occur if both use the same Virtual Channel
- The Routing Switch implements a watchdog timer to prevent indefinitely packet blocking:
 - When the packets transfer stops the watchdog timer is started.
 - When the maximum time elapses, the packet is spilled.
 - Independent watchdog timer for each Virtual Channel.

Broadcast messages

- Broadcast messages types:

- SpaceWire Time-Code
- SpaceWire Interrupt
- SpaceFibre Time-Slot
- SpaceFibre CCSDS Time

- SpW broadcast codes are translated to SpFi broadcast message.

- SpaceFibre Routing Switch local time is synchronised with network time.

0	7	8	15	16	23	24	31
COMMA		SBF		Broadcast Channel		Broadcast Type	
Time-Slot or Time-Code Interrupt code		0x0		0x0		0x0	
Bit-Inverse		Bit-Inverse		Bit-Inverse		Bit-Inverse	
EBF		RSVD/LATE		SEQ_NUM		CRC	

0	7	8	15	16	23	24	31
COMMA		SBF		Broadcast Channel		Broadcast Type = 0	
DATA 1 LS Fractional Byte LS		DATA 1 Fractional Byte		DATA 1 Fractional Byte MS		DATA 1 MS Seconds Byte 0 LS	
DATA 2 LS Seconds Byte 1		DATA 2 Seconds Byte 2		DATA 2 Seconds Byte 3		DATA 2 MS Seconds Byte 4 MS	
EBF		RSVD/LATE		SEQ_NUM		CRC	

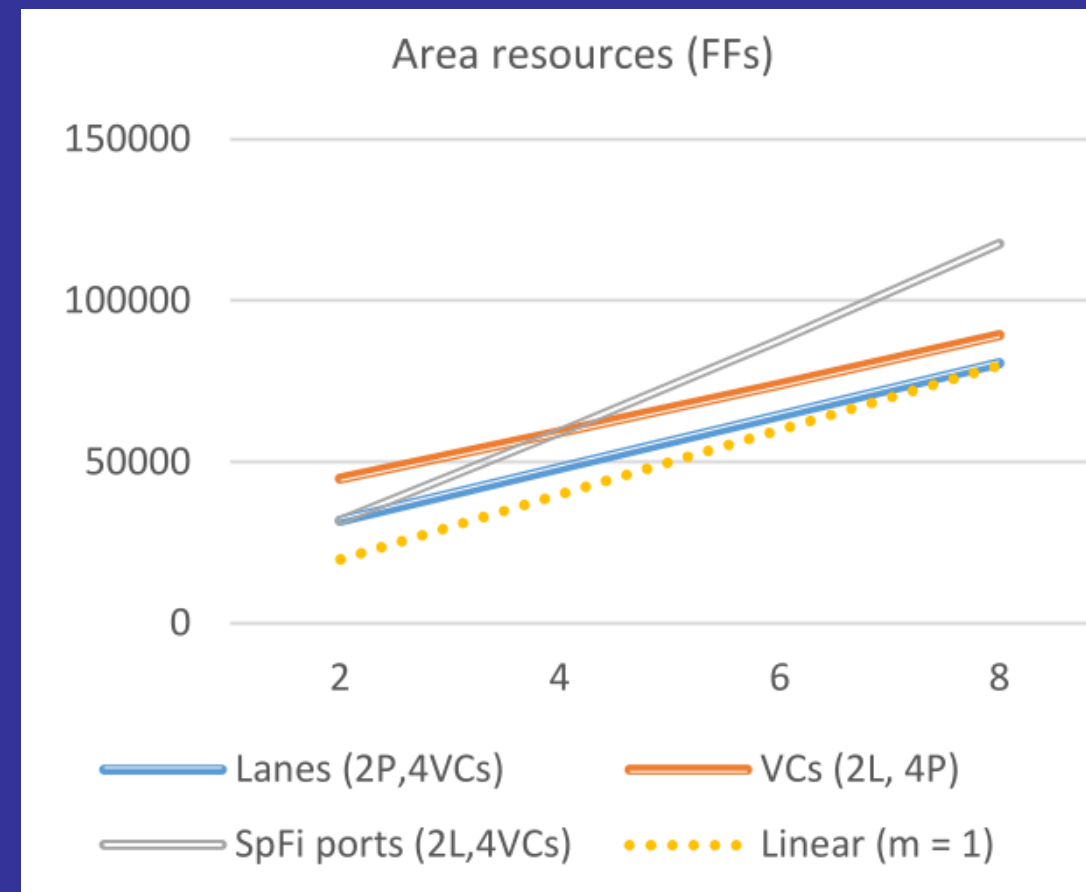
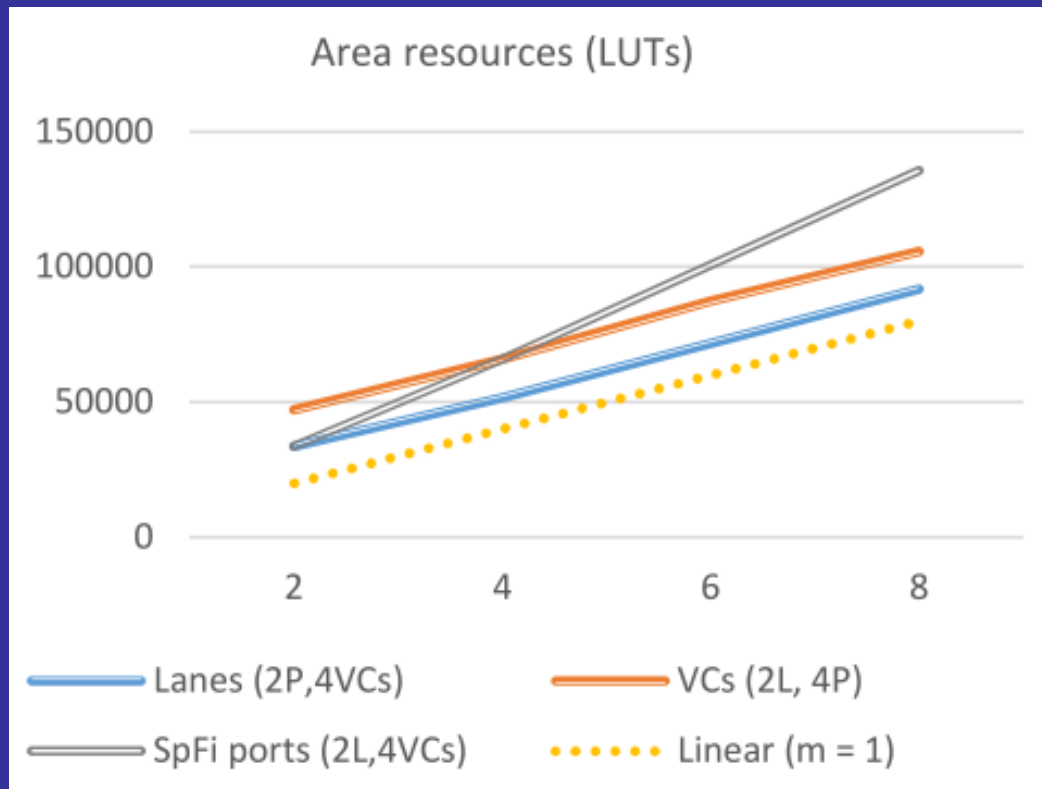
Synthesis Results

- The Routing Switch has been designed to achieve timing closure at the highest data rates supported by the transceivers available in existing radiation-tolerant technologies.
 - lane rates of 3.125 Gbps in RTG4
 - 6.25 Gbps in PolarFire FPGAs.
 - >6.25 Gbps in UltraScale and Versal Xilinx devices

	RTG4			XQRKU060 *		
	<i>LUT</i>	<i>DFF</i>	<i>LSRAM</i>	<i>LUT</i>	<i>DFF</i>	<i>RAMB36</i>
2L6P	48043	44434	59	28579	42829	33.5
2 VCs	31.6%	29.3%	28.2%	8.6%	6.5%	3.1%
2L10P	139644	116463	171	82625	109168	101.5
4 VCs	92.0%	76.7%	81.2%	24.9%	16.5%	9.4%
4L6P	77279	69216	117	46808	65607	61.5
2 VCs	50.9%	45.6%	56.0%	14.1%	9.9%	5.7%
4L10P	-	-	-	128600	158420	185.5
4 VCs	-	-	-	38.8%	23.9%	17.2%

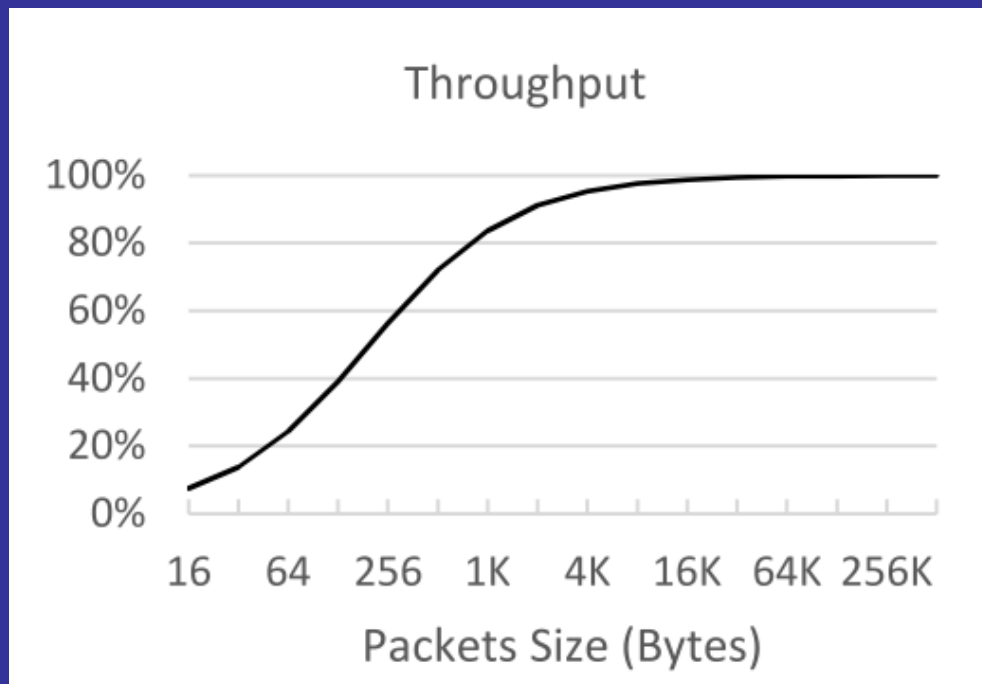
Synthesis Results in PolarFire

- The Routing Switch has been optimised for timing and to scale well when the number of lanes, ports, and VCs is increased.



Performance results

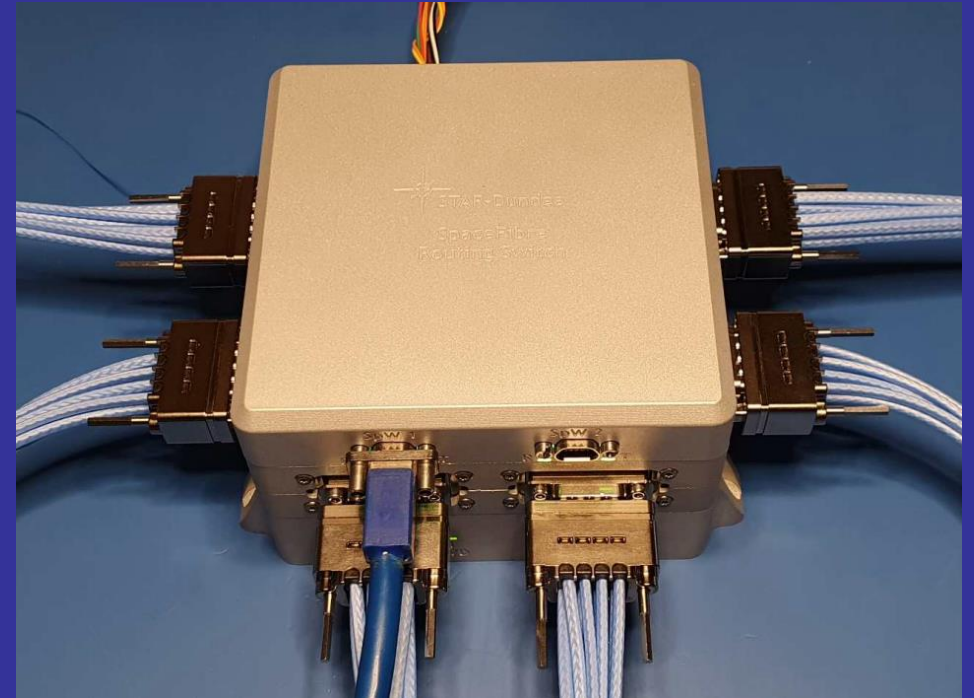
- Achieve full bandwidth of the SpFi interfaces without any dependency on the number of simultaneous data flows within the router.



	Path addressing	Logical Addressing
Packet Latency	34 clock cycles	38 clock cycles
Switching Latency	22 clock cycles	25 clock cycles
Broadcast Latency	10 Clock cycles	

Hardware Implementation

- STAR-Tiger implemented in the Hi-SIDE project with 10 SpaceFibre ports:
 - Two quad-lane ports
 - Eight dual-lane ports
 - Lane speed up to 6.25 Gbit/s
 - Port data rate 19.2 Gbit/s (quad-lane) and 9.6 Gbit/s (dual-lane port)



Conclusions

- STAR-Dundee has developed a SpFi Multi-Lane Routing Switch IP
 - Easy to use and highly configurable
 - Achieve the highest lane rates on space-grade FPGAs
 - Scales well with increasing number of lanes, ports and virtual channels.
 - Implements SpaceWire to SpaceFibre bridge
 - Validated within a full satellite data-chain technology demonstrator.