A SpaceWire/SpaceFibre architecture based on ADHA

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DEFENCE AND SPACE

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Agenda

- ADHA Introduction
- ADHA Rack Concept
- ADHA Standardization
- ADHA Internal SpaceWire Architecture
- ADHA Internal SpaceFibre Architecture
- Example ADHA Unit and Interconnection

ADHA Introduction

Advanced Data Handling Architecture (ADHA) Goals

- Reduce volume, mass, and power consumption of the data-handling system
- Reduce development time
- Increase cost efficiency
- Simplify adaption to new technologies

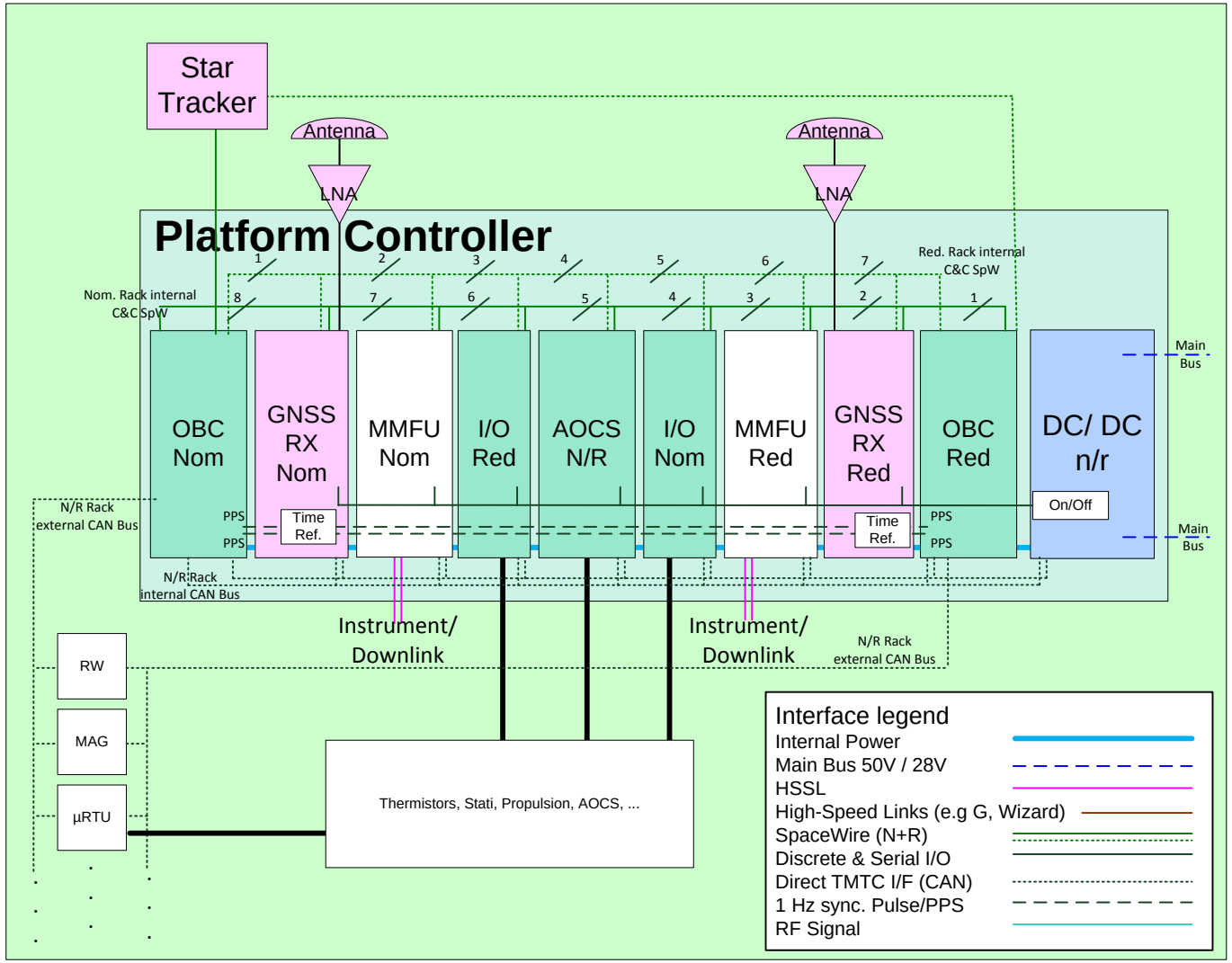
By the means of:

- Standardization (mechanical, thermal, electrical, communication protocols)
- Taking design decisions which are necessary to simplify compatibility
- ESA incorporating all major European industry representatives in the definition

ADHA Concept

Rack based solution

- Boards which are covering different functions (OBC, AOCS, MMFU, I/O) hosted in one rack (Unit)
- Interconnection (power and communication) via backplane
- Not several units distributed in S/C
- Reduced harness, housing, DC/DC converter
- Increased inter-functional data rates



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ADHA Standardisation (1/2)

- Front-panel for external connections
- Backplane based on Compact PCI® Serial Space Standard
- Backplane connector and PIN allocation standardized
- Mechanical boards size defined to 6U (ADHA rack) or 3U (Micro Remote Terminal Unit - µRTU)
- Standardisation shall allow different suppliers to manufacture boards for one rack
- Communication via well standardised CAN-Bus, SpaceWire and SpaceFibre to allow interoperability and interchangeability

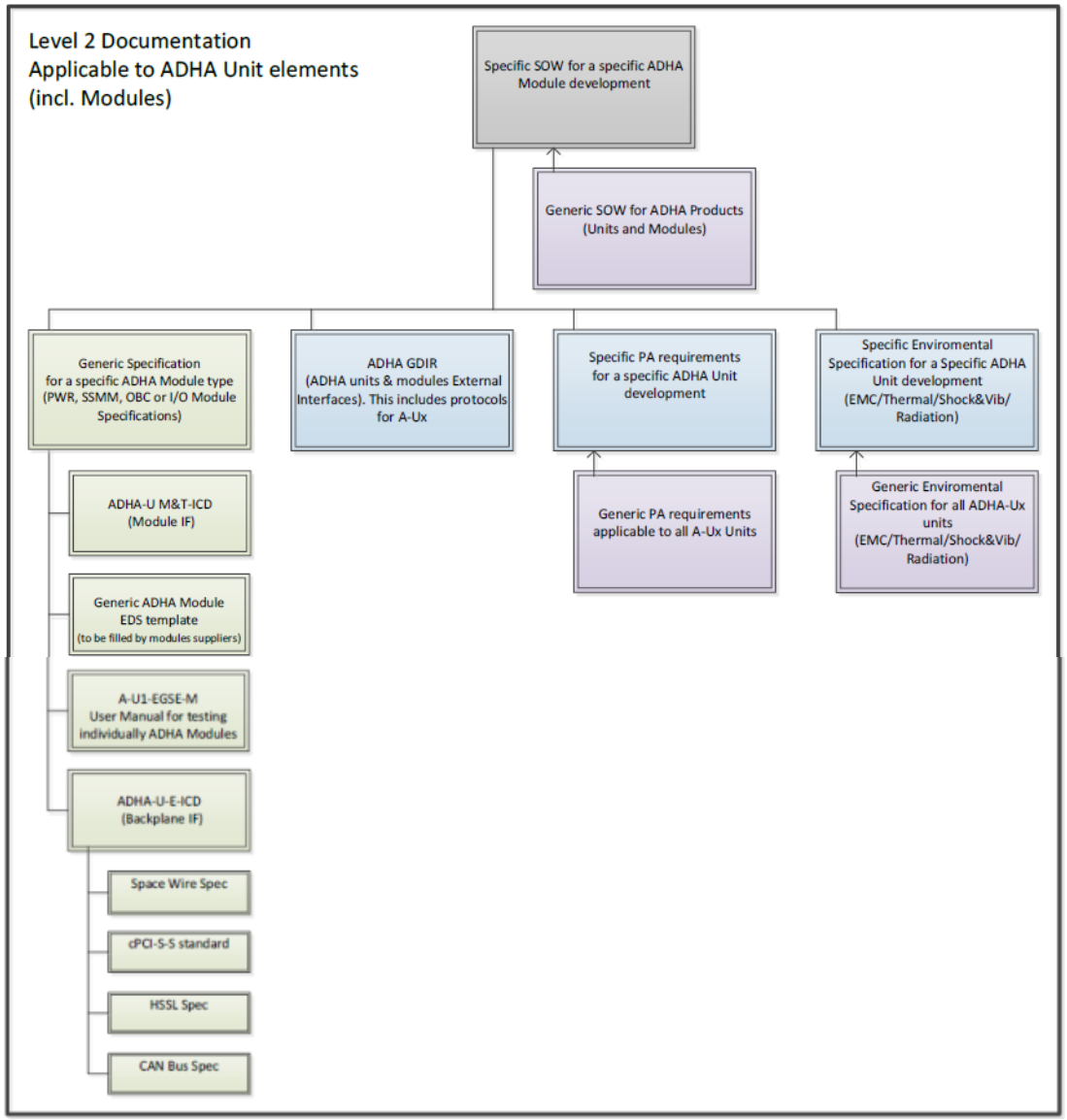
ADHA Standardisation (2/2)

Set of public and standardised (ITT) documents

- Units
- Modules
- EGSE
- Mechanical Housing
- Backplanes

Major documents

- Backplane Specification
- SpaceWire Specification
- SpaceFibre Specification
- CAN Bus Specification
- SOW
- PA requirements
- Environmental requirements
- Electrical Interface requirements
- Technical Specification
- EICD/EDS template
- Testing Manual



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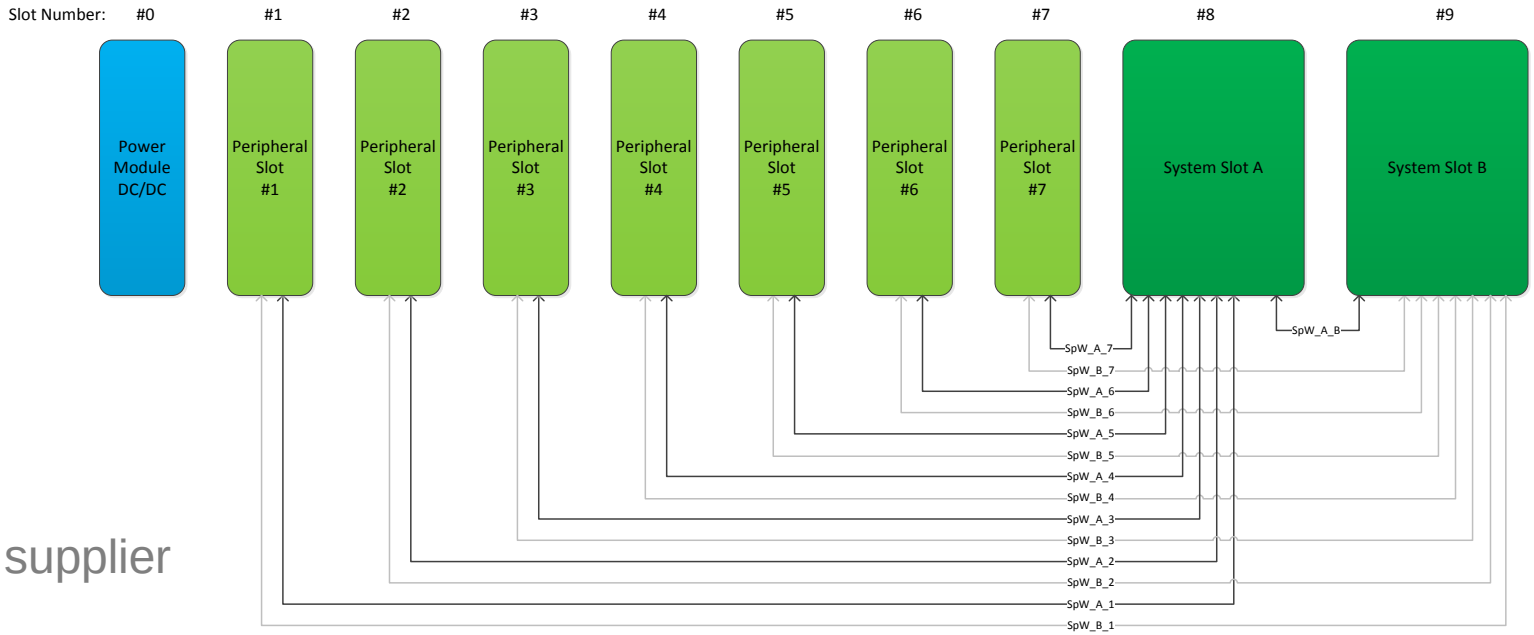
ADHA Internal SpaceWire Architecture

- 2 system controller slots
- 7 peripheral slots (e.g. STR, ICU)
- 1 DC/DC converter slot
  (not connected to SpW)
- Single point failure free dual star
  SpW topology
- 100 Mbps as targeted data rate
- Skew-Jitter budget managed by rack supplier
- Fault voltage requirements to allow
  direct SpW connection to FPGA/ASIC
  (without dedicated driver/receiver) to reduce footprint,
  simplify layout, manufacturing and process qualification



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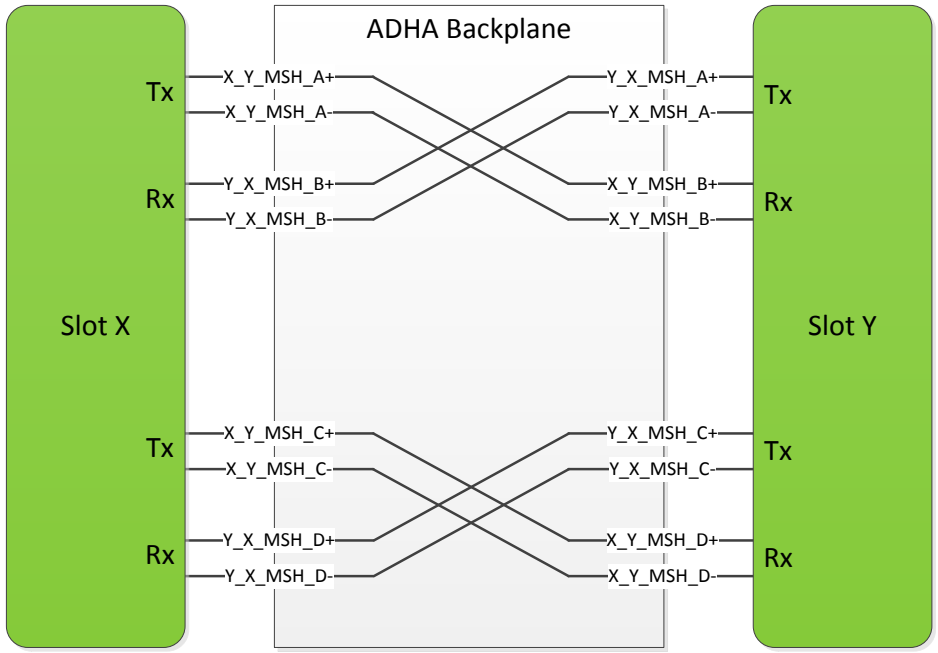
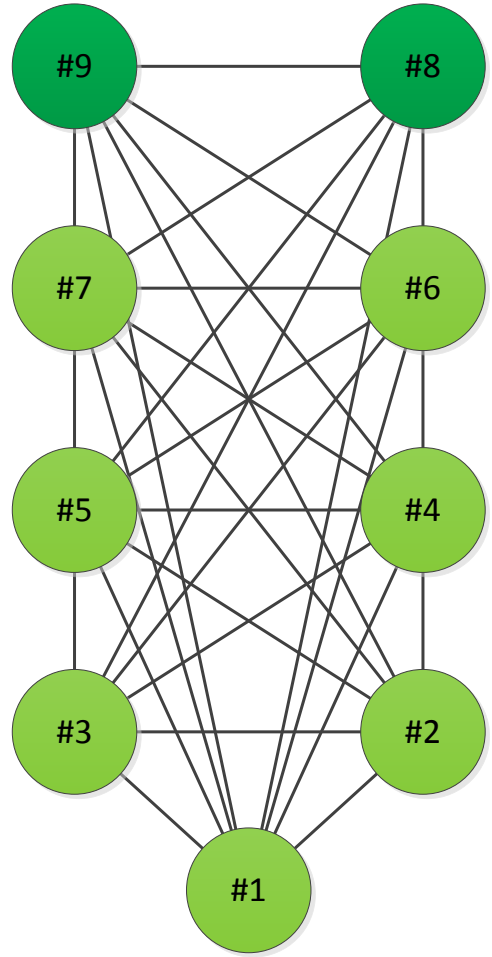
ADHA Internal SpaceFibre Architecture

- SpaceFibre selected for High Speed Serial Links in ADHA
- Full mesh network or router based star topology (first Engineering Model) integrated in the ADHA unit
- Two transmitting differential pairs and two receiving differential pairs for each line between two slots
- Traffic separation by virtual channel





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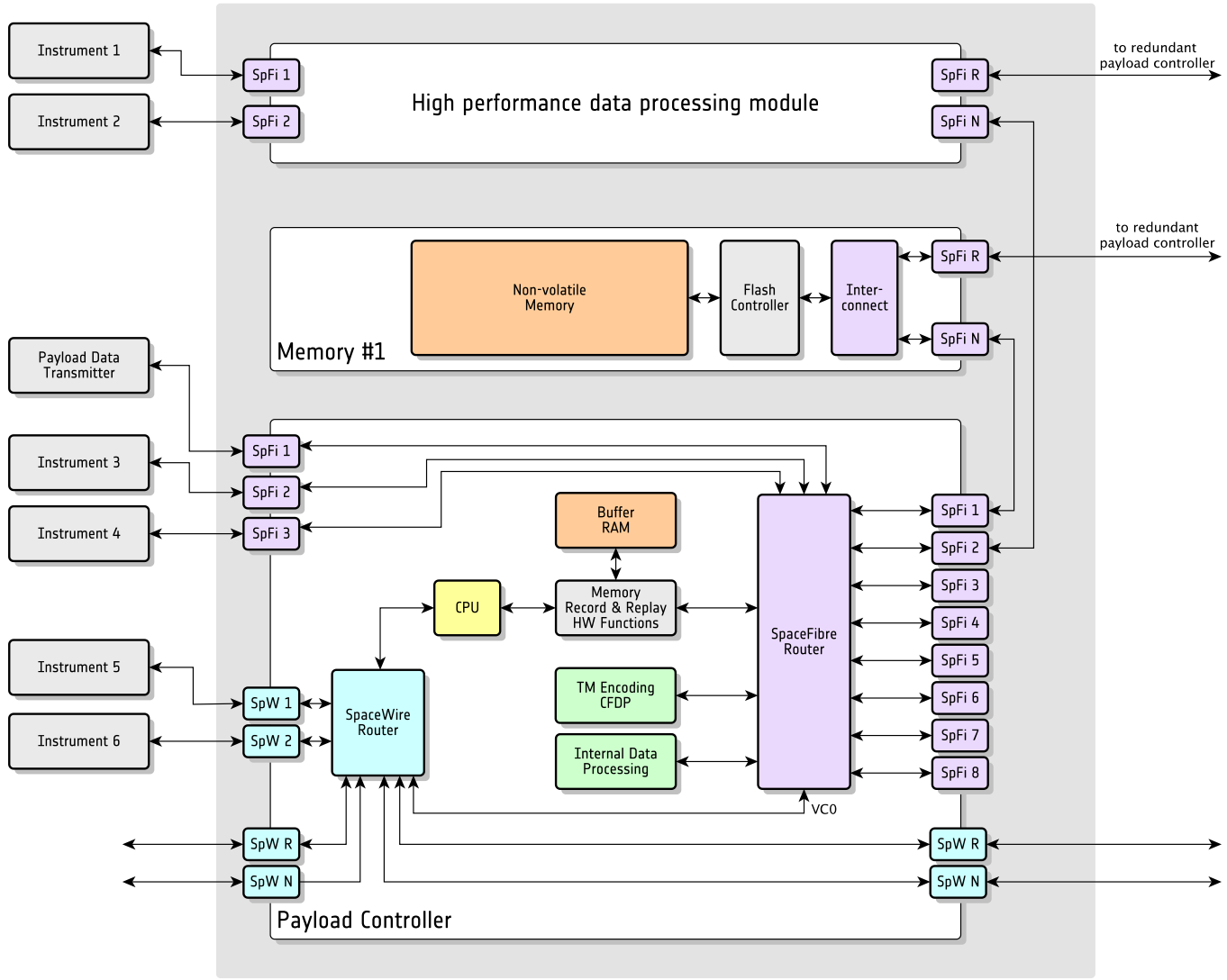
ADHA Example Payload Unit

- Payload Controller including router with SpW&SpFi I/Fs on Front-Panel (ADHA external) and Back-Plane (ADHA internal)
- Flash Memory Module
- Data Processing Module
- Full flexibility of data flow based on application needs (front and rear-panel)
- Different pre- &post-processing configurations possible
- Flash Memory Module is hosted on separate module (board) with low-level block access via backplane (SpW/SpFi)



ADHA Payload Unit

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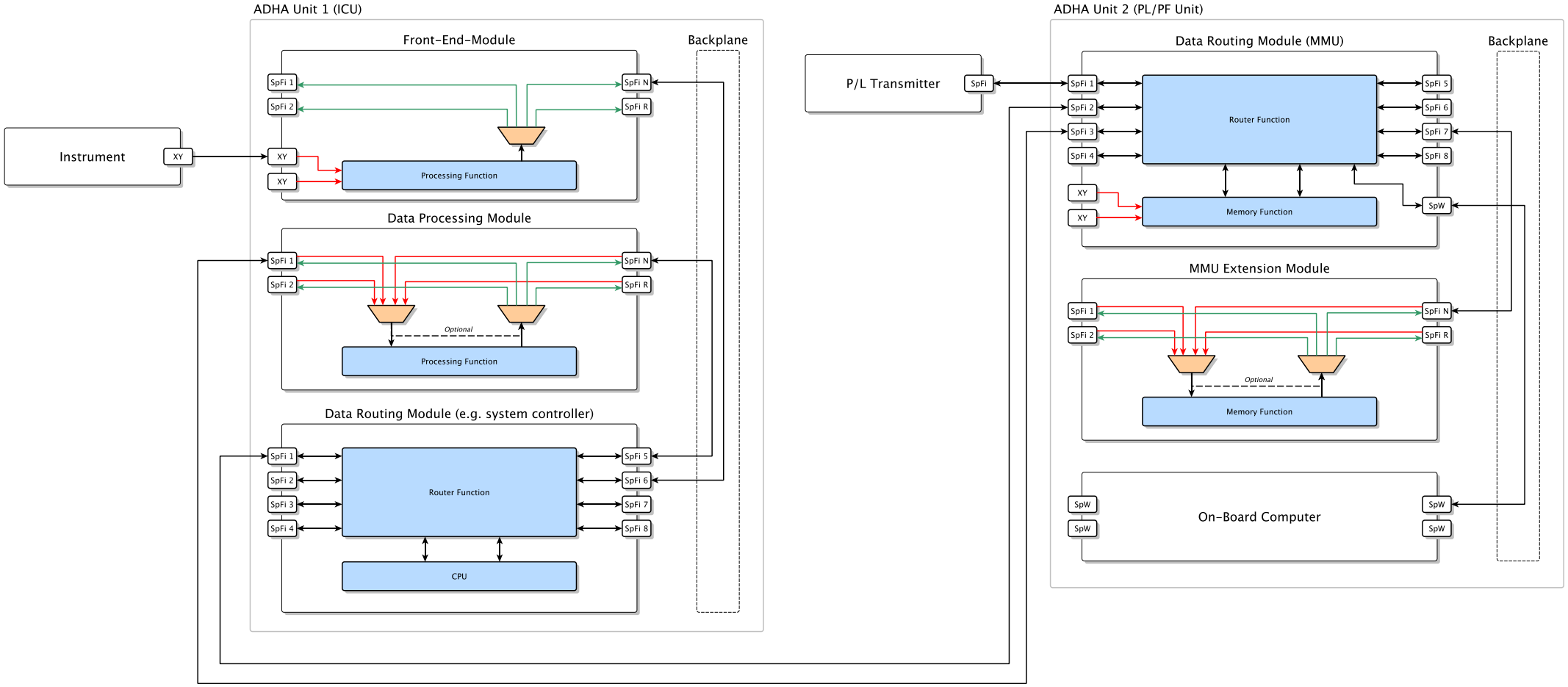
ADHA System of Two Racks (Example)



- I/F to Instruments via Front-End-Module
- I/F to P/L Transmitter via Data Routing Module
- Inter-ADHA-Rack-Link

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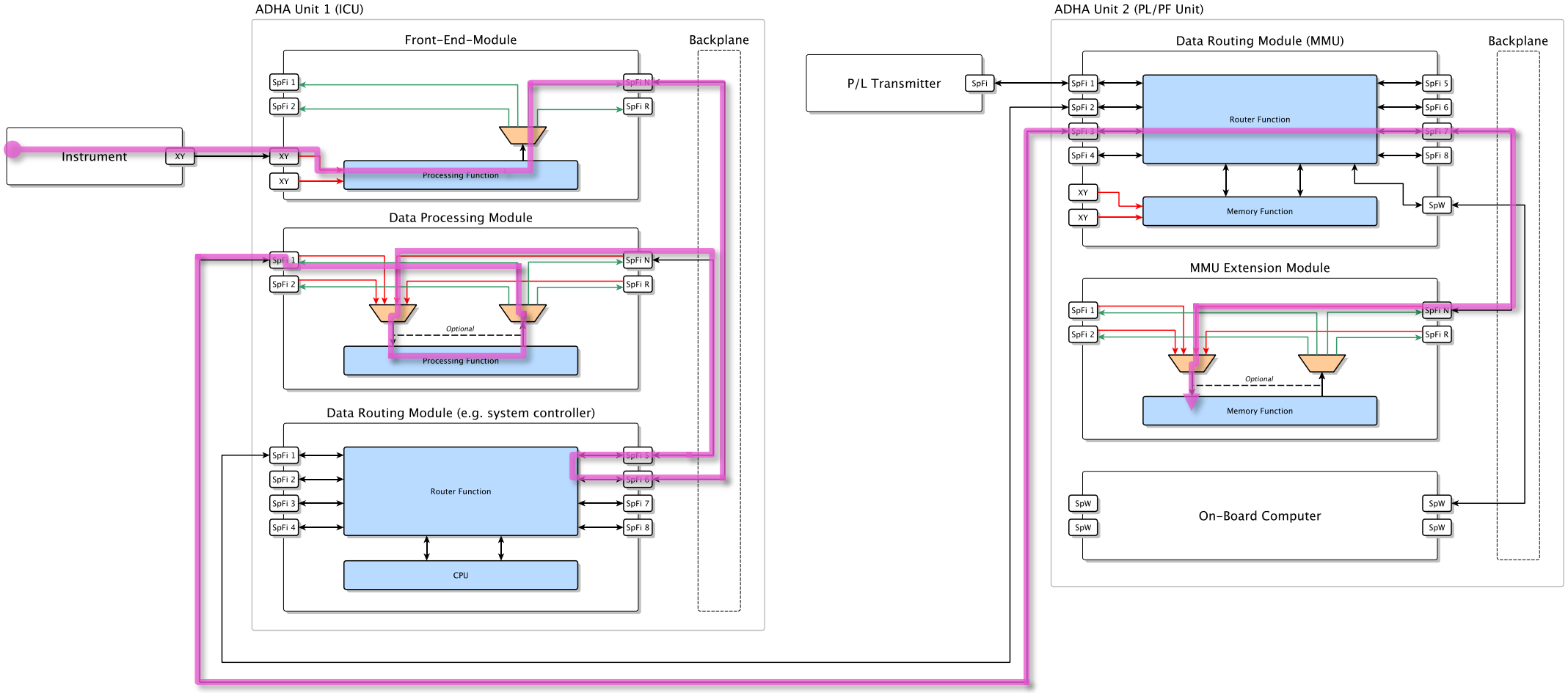
ADHA System of Two Racks (Example)



Pre-processing chain

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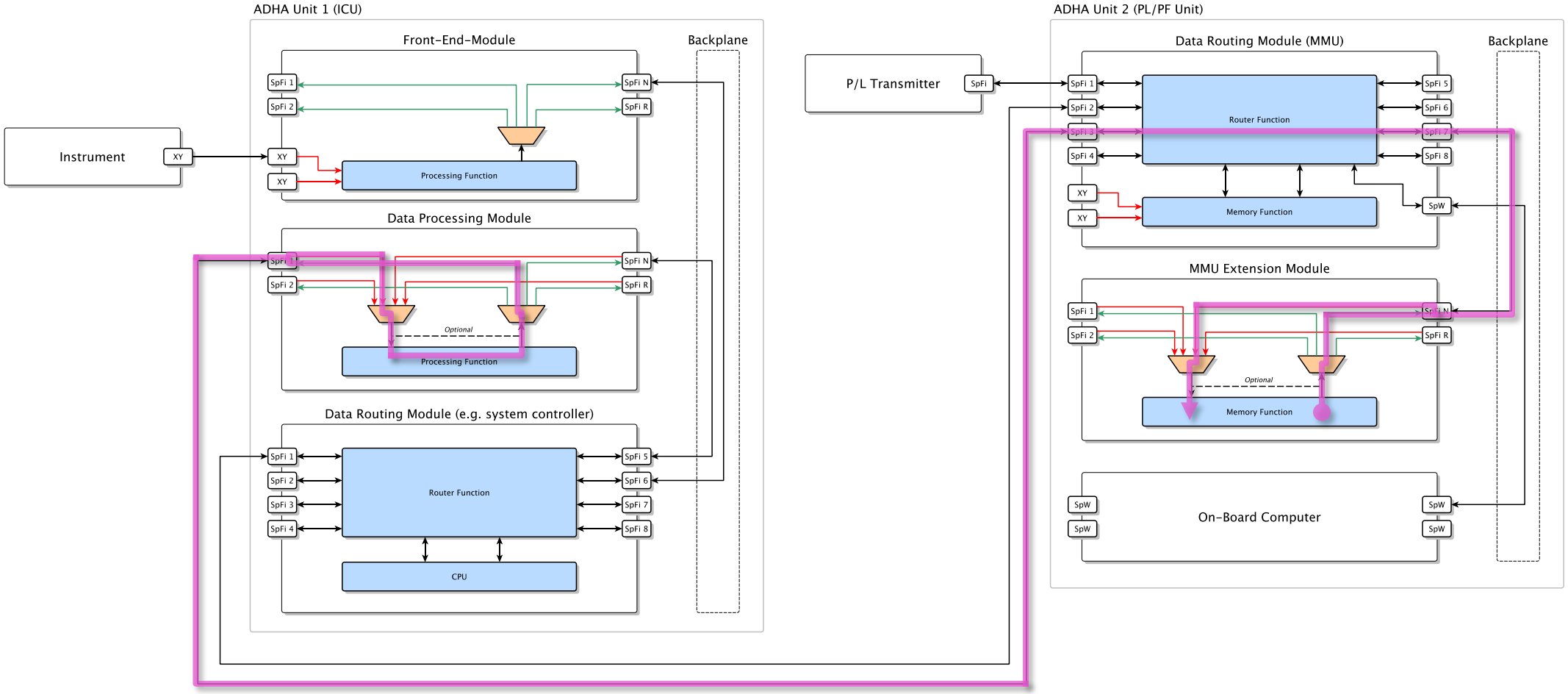
ADHA System of Two Racks (Example)



Offline processing chain

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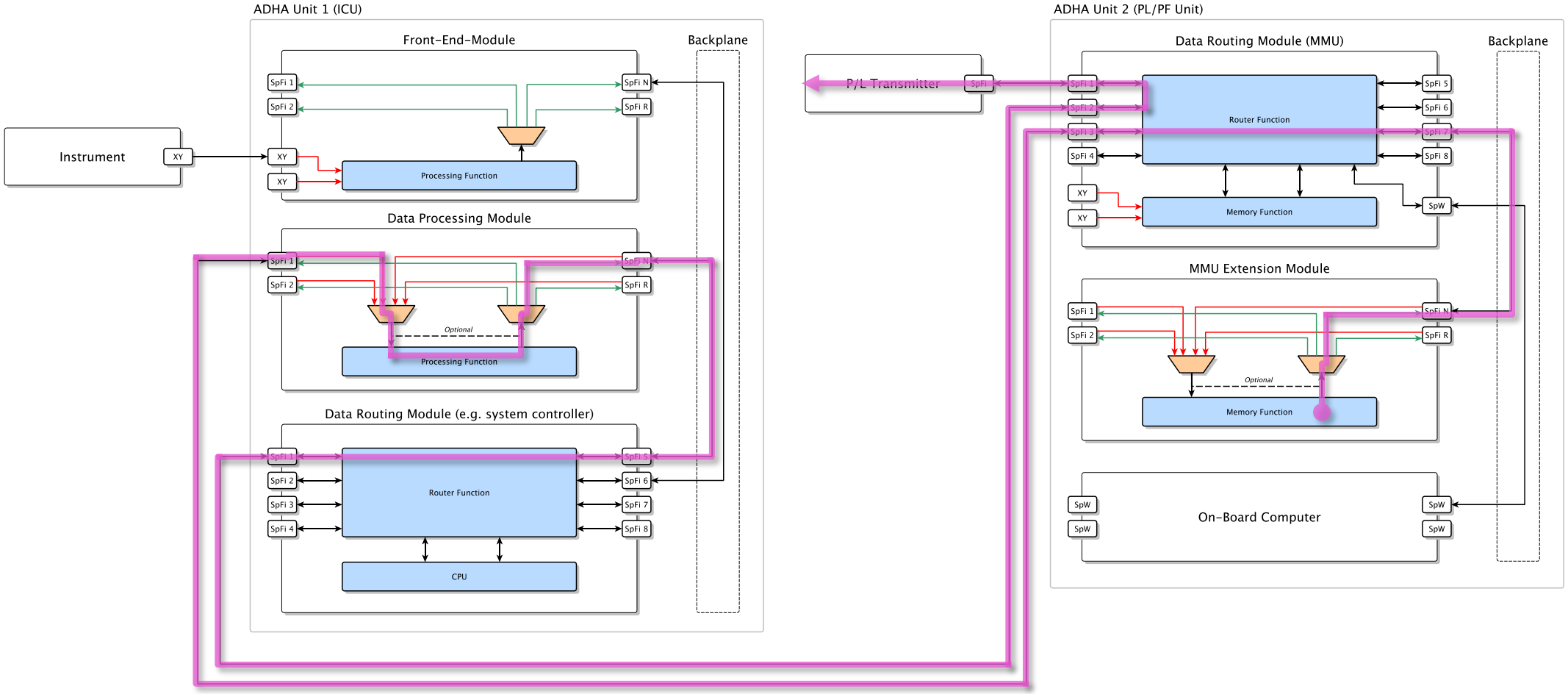
ADHA System of Two Racks (Example)



Post-processing chain

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Conclusion

- ADHA shall define On-Board Data Handling systems for future satellite missions
- ADHA based on simple, flexible, scalable concept with standardised, interchangeable, and inter-operable electronics modules
- High maturity of SpaceWire and SpaceFibre standardisation and heritage ideal for ADHA concept
- Rapid adaption to new technologies (modules based on multicore processors, machine learning and artificial intelligence techniques, COTS, etc.) and reduced development effort/time due to harmonized standardisation
- Target date for first EM Unit: 2025

Q&A

Thank you!

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