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20 Years of Spacecraft Networking Innovation

SpaceFibre IP Cores for the Next Generation of Radiation-Tolerant FPGAs

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Introduction - SpaceFibre

- Compatible with SpaceWire packet and network level
  - Because it transfers SpaceWire packets
    - Supports any packet length
- Provides data integrity and reliable data delivery
  - Automatically recovers from transient errors in less than 2 μs
  - Lane is automatically reinitialised if BER is worse than 10^{-5}
- Multiple concurrent data flows over the same link with QoS
  - VCs have priority, bandwidth allocation and scheduling QoS
- Low latency broadcast messages (< 1 μs)
  - Broadcasted to all nodes in a network
    - Guaranteed that same message is not received twice
- Multi-lane capabilities
  - Arbitrary number of lanes with graceful degradation when a lane fails.
  - Warm redundancy recovers from a lane failure in less than 80 μs
  - Hot redundancy recovers from a lane failure in less than 3 μs

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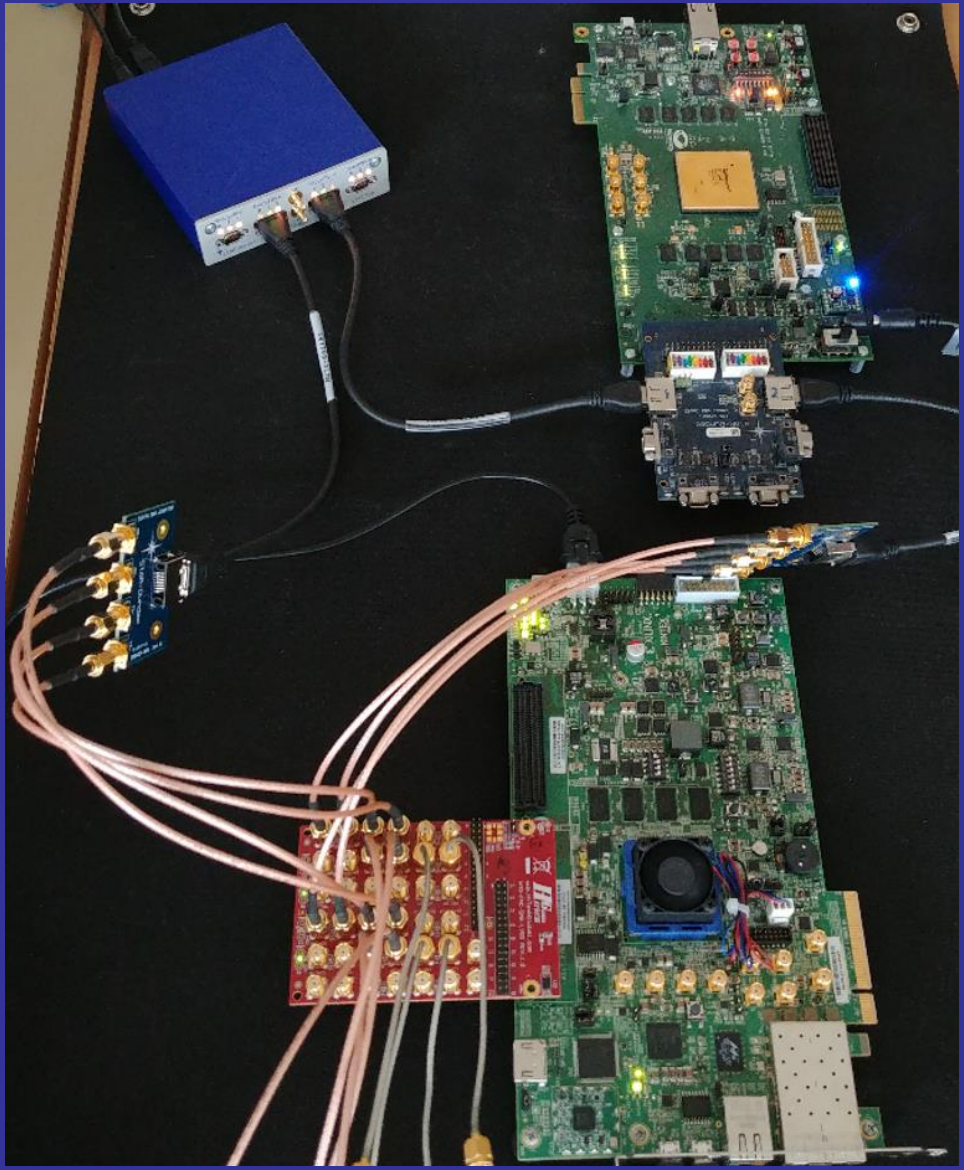
New Generation FPGAs for Space



- Microchip RTG4
  - 65 nm
  - Flash-based – Non-volatile
  - Radiation-hardened by design
  - 24x SerDes @ 3.125 Gbit/s

- Xilinx Kintex UltraScale
  - 20 nm
  - SRAM-based – Volatile
  - Radiation-tolerant
  - 32x SerDes @ 12.5 Gbit/s

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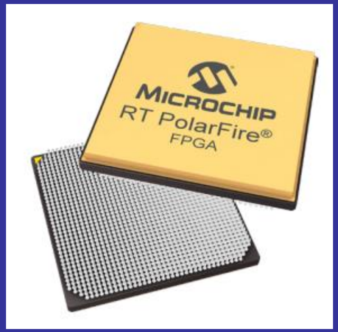
New Generation FPGAs for Space

- NanoXplore BRAVE family (NG-Large / NG-Ultra)
  - 65 / 28 nm FD-SOI
  - SRAM-based – Volatile
  - Radiation-hardened by design
  - 4x SerDes @ 6 Gbit/s / 32x SerDes @ 12.5 Gbit/s

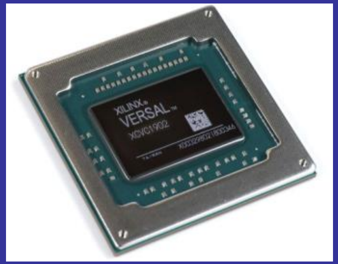
- Microchip RTG4
  - 65 nm
  - Flash-based – Non-volatile
  - Radiation-hardened by design
  - 24x SerDes @ 3.125 Gbit/s

- Microchip PolarFire
  - 28 nm
  - SONOS-based – Non-volatile
  - Radiation-tolerant
  - 24x SerDes @ 10 Gbit/s



- Xilinx Kintex UltraScale
  - 20 nm
  - SRAM-based – Volatile
  - Radiation-tolerant
  - 32x SerDes @ 12.5 Gbit/s

- Xilinx Versal
  - 7 nm FinFET
  - SRAM-based – Volatile
  - Radiation-tolerant
  - 44x SerDes @ 25 Gbit/s



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SpaceFibre IP Cores General Features

- Configurable
  - Number of lanes, virtual channels, ports
  - Type of SerDes and configuration interface
- High performance
  - Optimised for radiation hardened FPGAs
  - Low latency
- Easy to use
  - AXI4-Stream interface for each VC
  - Reference designs for RTG4, PolarFire, KUS, Versal, BRAVE...
  - ASIC-ready
- Safe
  - Extensive verification and validation
  - Tested in radiation environment

SpaceFibre IP Cores General Features

- Use of EDAC protection in memories

- Guaranteed, straightforward, timing closure
  - Lane rate only limited by Serdes (e.g. up to 3.125 Gbps on RTG4)
  - For the whole temperature and voltage range (i.e. fast & slow corners)
  - With EDAC and SET filters
  - Does not require specific placement or timing constraints.
  - Even with more than 80% FPGA utilisation

- Low latency
  - Less than 400 ns for Broadcasts (including 250ns due to SerDes latency)
  - Streaming frame sending option

- Compact design

SpaceFibre IP Interfaces

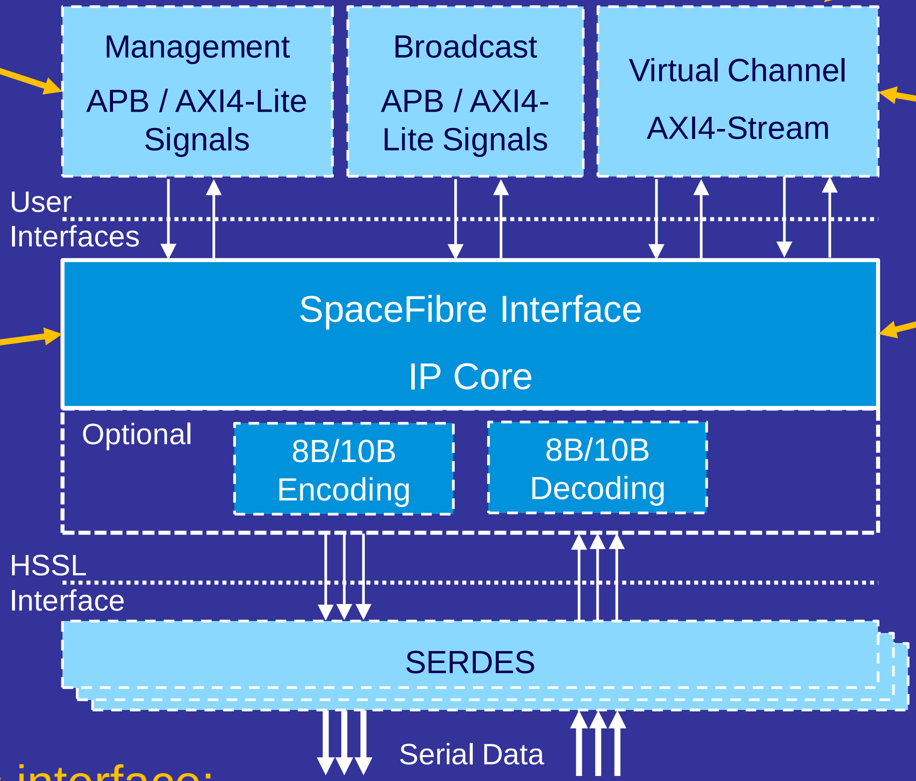
Use of an APB / AXI4-Lite with registers

Number of virtual channels

Independent clock for each AXI interface

Technology independent RTL with optimisations for specific FPGAs

Depth of internal buffering



Type of SerDes interface: RTG4, PolarFire, Xilinx, BRAVE, TLK2711, Parallel

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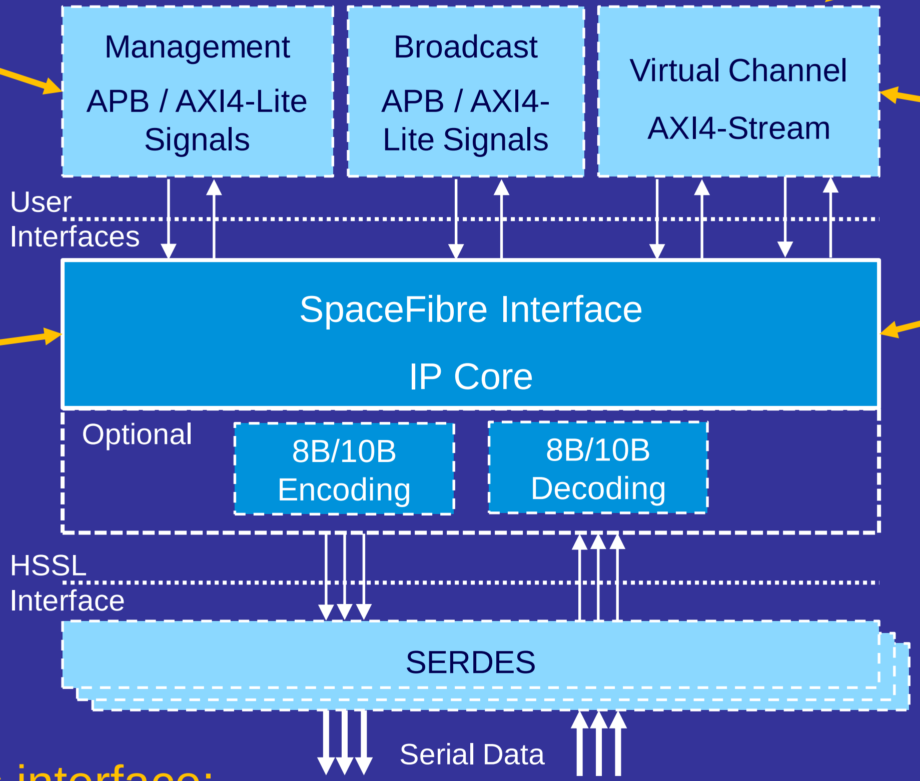
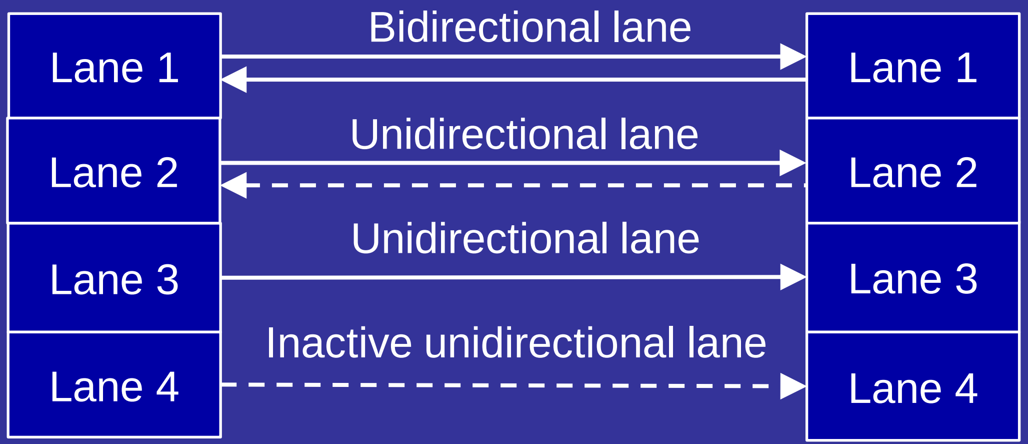


Type of SerDes interface: RTG4, PolarFire, Xilinx, BRAVE, TLK2711, Parallel

Number of lanes, Tx/Rx unidirectional lanes, hot/warm redundancy



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SpaceFibre IP @ BRAVE

- Successful link connection established with STAR-Fire unit
  - Correct data transmission <u>without any data errors</u>
- Retry events periodically appear ☹
- Currently debugging this problem in collaboration with NanoXplore
  - The final validation of the IP to be completed soon
  - Reference design with SerDes configuration, clock scheme details, memory instantiation (EDAC), etc. provided with IP

SpaceFibre Single-Lane Interface IP Resources

	RTG4			XQRKU060 *		
	LUT	*DFF*	*LSRAM*	*LUT*	*DFF*	*RAMB36*
1 VC	3316 2.2%	2365 1.6%	4 1.9%	1823 0.5%	2346 0.4%	4 0.4%
2 VCs	3960 2.6%	2946 1.9%	6 2.9%	2162 0.7%	2969 0.4%	6 0.6%
4 VCs	5389 3.5%	4114 2.7%	10 4.8%	2960 0.9%	4214 0.6%	10 0.9%

	RTPF500T *			XQRVC1902 *		
	LUT	*DFF*	*LSRAM*	*LUT*	*DFF*	*RAMB36*
1 VC	2796 0.6%	2226 0.5%	8 0.5%	1687 0.2%	2272 0.1%	2 0.2%
2 VCs	3400 0.7%	2801 0.6%	12 0.8%	1985 0.2%	2824 0.2%	3 0.3%
4 VCs	4653 1.0%	3972 0.8%	20 1.3%	2796 0.3%	3923 0.2%	5 0.5%

SpaceFibre Single-Lane Interface IP Resources

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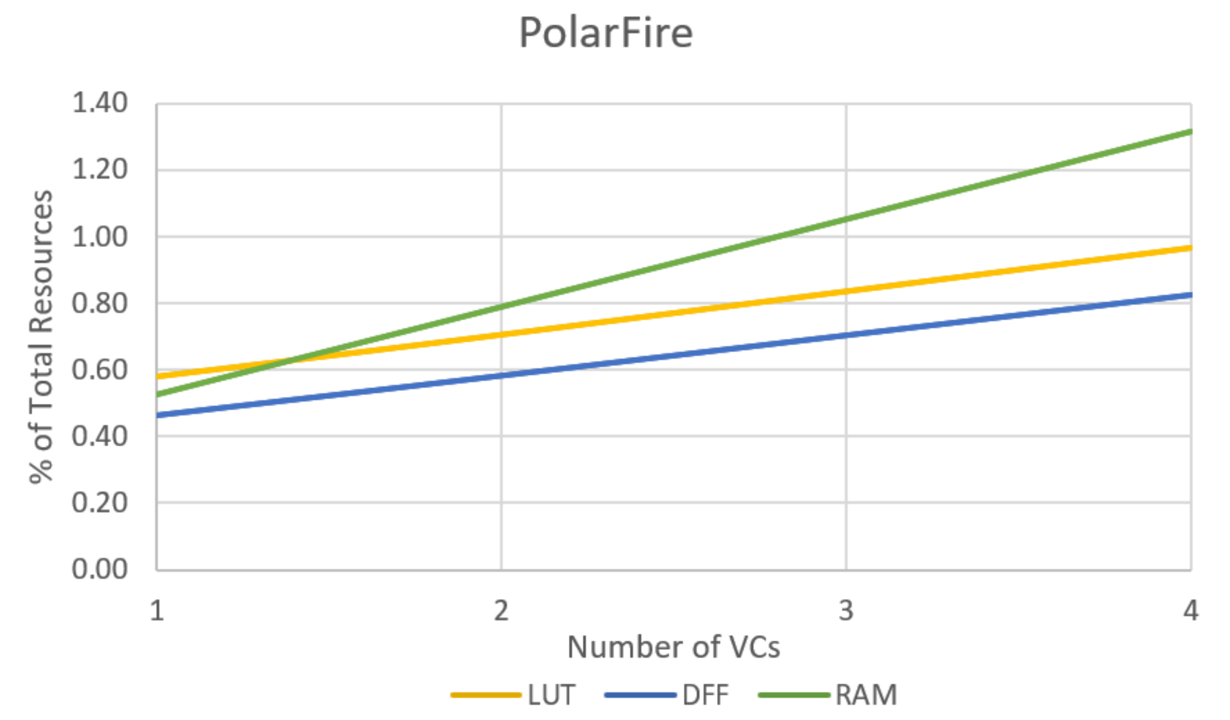
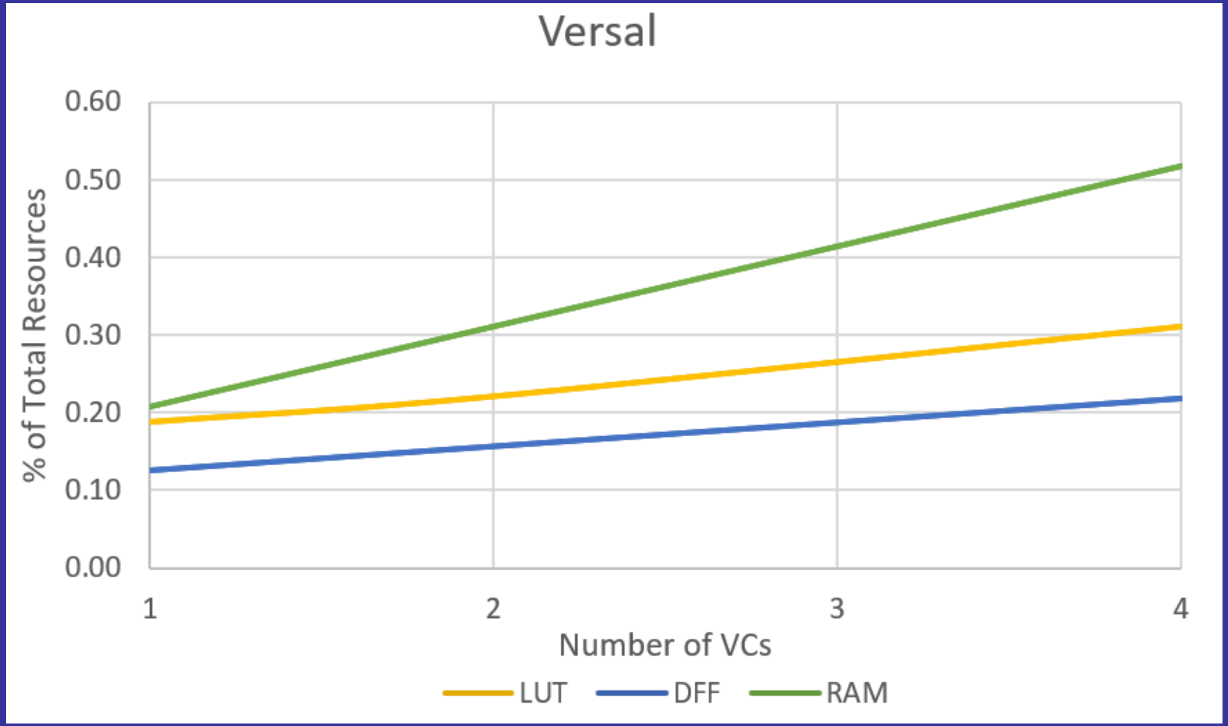
- TMR in PolarFire
  - DFF ~ x 2.8
  - LUT ~ x 2





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SpaceFibre Single-Lane Interface IP Resources

- NG family share the same type of fabric resources
  - IP implementation expected to use the same resources in NG-Large and NG-Ultra

- In terms of % of resource usage for the SpFi IP Core
  - NG-Large is equivalent to the RTG4
  - NG-Ultra is equivalent to the PolarFire

	NG-Large			NG-Ultra		
	LUT	*DFF*	*RAM*	*LUT*	*DFF*	*RAM*
1 VC	2703 2.0%	2496 1.9%	8 4.2%	2703 0.5%	2496 0.5%	8 1.2%
2 VCs	3275 2.4%	3068 2.4%	12 6.3%	3275 0.6%	3068 0.6%	12 1.8%
4 VCs	4350 3.2%	4220 3.3%	20 10.4%	4350 0.8%	4220 0.8%	20 3.0%

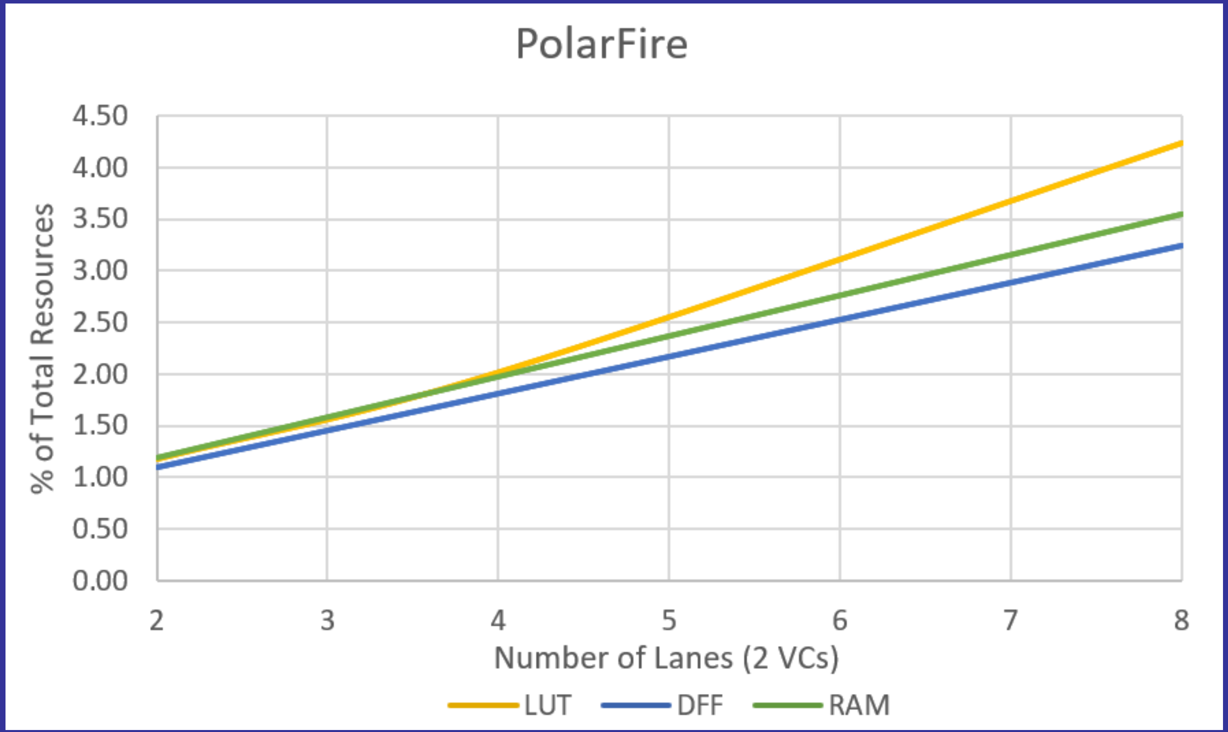
SpaceFibre Multi-Lane Interface IP Core

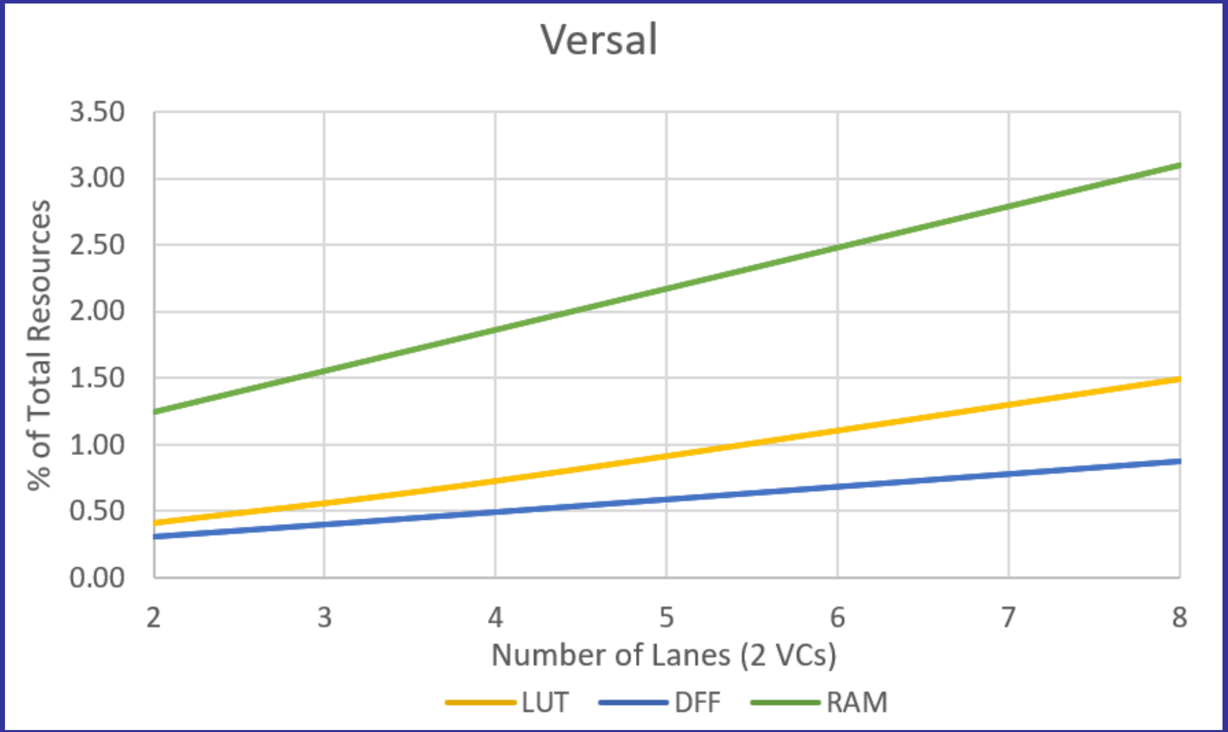
- Multi-Lane is an optional capability of the SpFi standard

- Allows several physical lanes to behave as a single logical link
  - Higher throughput
  - Redundancy
    - Hot (< 3 µs) & Warm (< 80 µs)

- Lanes can be operated independently
  - Any number of lanes supported
  - Unidirectional lanes supported

SpaceFibre Multi-Lane Interface IP Resources





- Values for different configurations (2/4/8 Lanes and 1/2/4 VCs) available the paper

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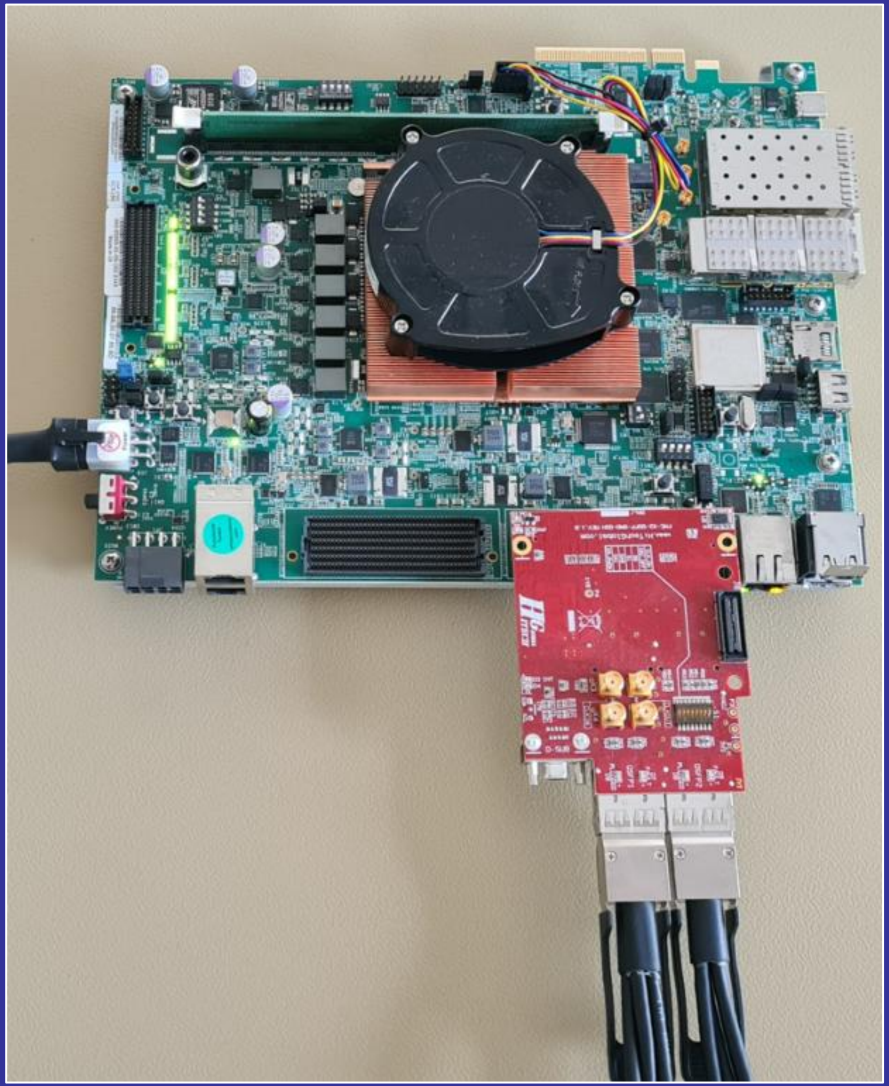
SpaceFibre Multi-Lane Interface IP Implementation



SpaceFibre Routing Switch IP Core

- Full non-blocking switch matrix
- Fully configurable
  - Port type
    - SpaceFibre → Number of lanes, VCs
    - AXI4-Stream Internal → Number of VCs
    - SpaceWire
  - Target technology
- Deterministic low latency switching
- Supports path, logical addressing and group adaptive routing

SpaceFibre Routing Switch IP Core

- Each virtual channel of each port can be configured to belong to any virtual network.
- Configuration port with RMAP protocol
- Isolates each virtual network using priority, scheduling and bandwidth reservation QoS.
- Within the same virtual network:
  - There is packet by packet round robin arbitration for packets going to the same output port
  - Automatic packet spill on timeout event caused by unexpected packet blocking, using a configurable virtual channel time-out period.
  - Additional timeout timers to detect a babling node

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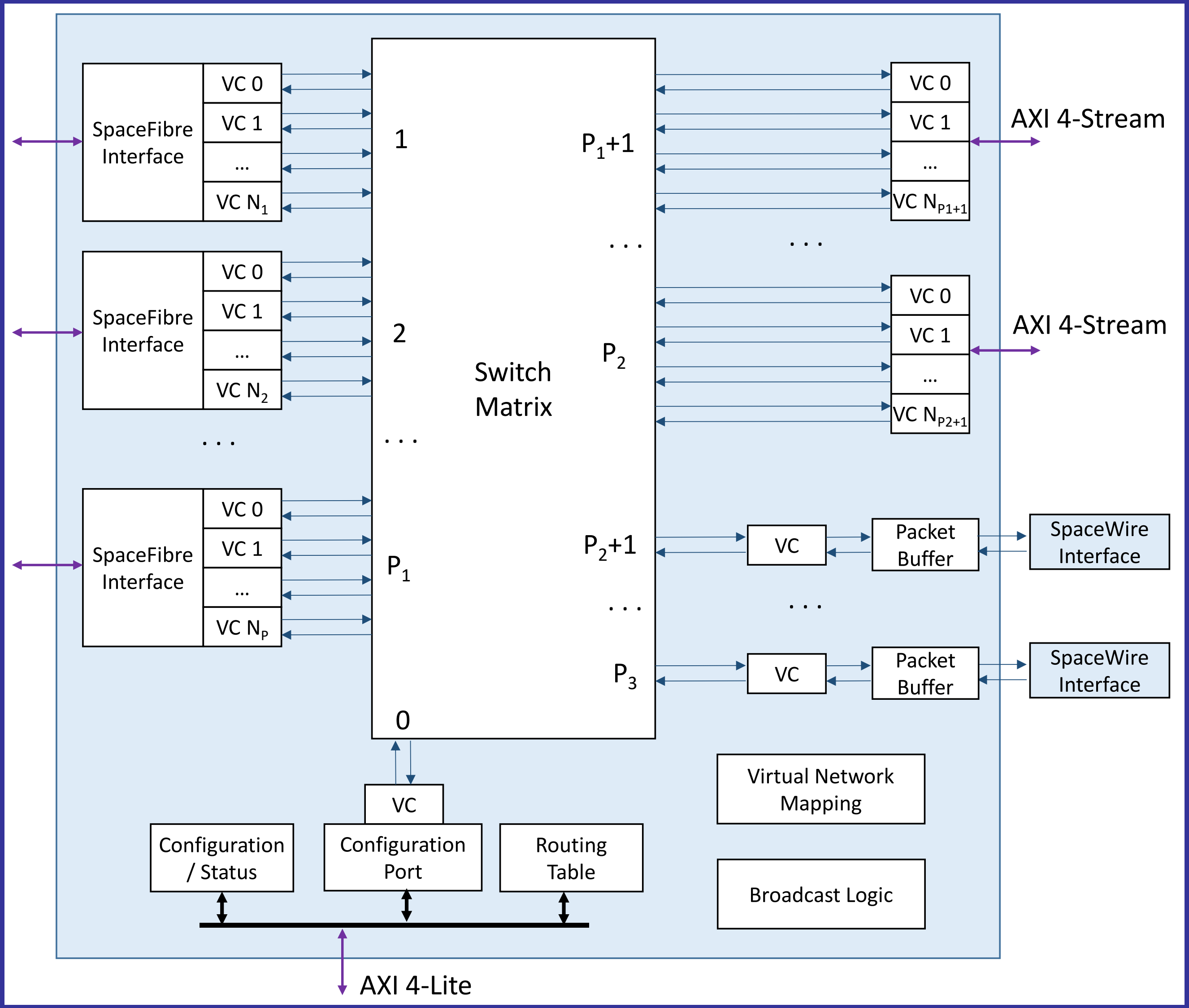
SpaceFibre Routing Switch IP Core



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SpaceFibre Single-Lane Routing Switch IP Resources

- SpFi Interface IP Cores are <u>included</u>
- Additional Configuration port and RMAP target is also included
- Port count includes 1x internal AXI4-Stream (2 VCs) and 1x SpW ports

	RTG4			XQRKU060 *		
	LUT	*DFF*	*LSRAM*	*LUT*	*DFF*	*RAMB36*
6 Port 2 VCs	31782 20.9%	27393 18.0%	47 22.5%	17984 5.4%	28090 4.2%	48 4.4%
10 Port 4 VCs	98540 64.9%	76035 50.1%	127 60.8%	55917 16.9%	78051 11.8%	128 11.9%

	RTPF500T *			XQRVC1902 *		
	LUT	*DFF*	*LSRAM*	*LUT*	*DFF*	*RAMB36*
6 Port 2 VCs	29938 6.2%	26943 5.6%	93 6.1%	17098 1.9%	27652 1.5%	48 5.0%
10 Port 4 VCs	93526 19.4%	75905 15.8%	253 16.6%	53800 6.0%	75867 4.2%	128 13.2%

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- 6 Port 2 VCs → 12 VCs
- 10 Port 4 VCs → 36 VCs

- DFF/VC ~ 2200
- LUT4/VC ~ 2600 (RTG4/PF)
- LUT6/VC ~ 1500 (KUS/Versal)

- Easy way to have a ROM of a design from the number of VCs required

SpaceFibre Multi-Lane Routing Switch IP Core

- Presentation coming next about this IP

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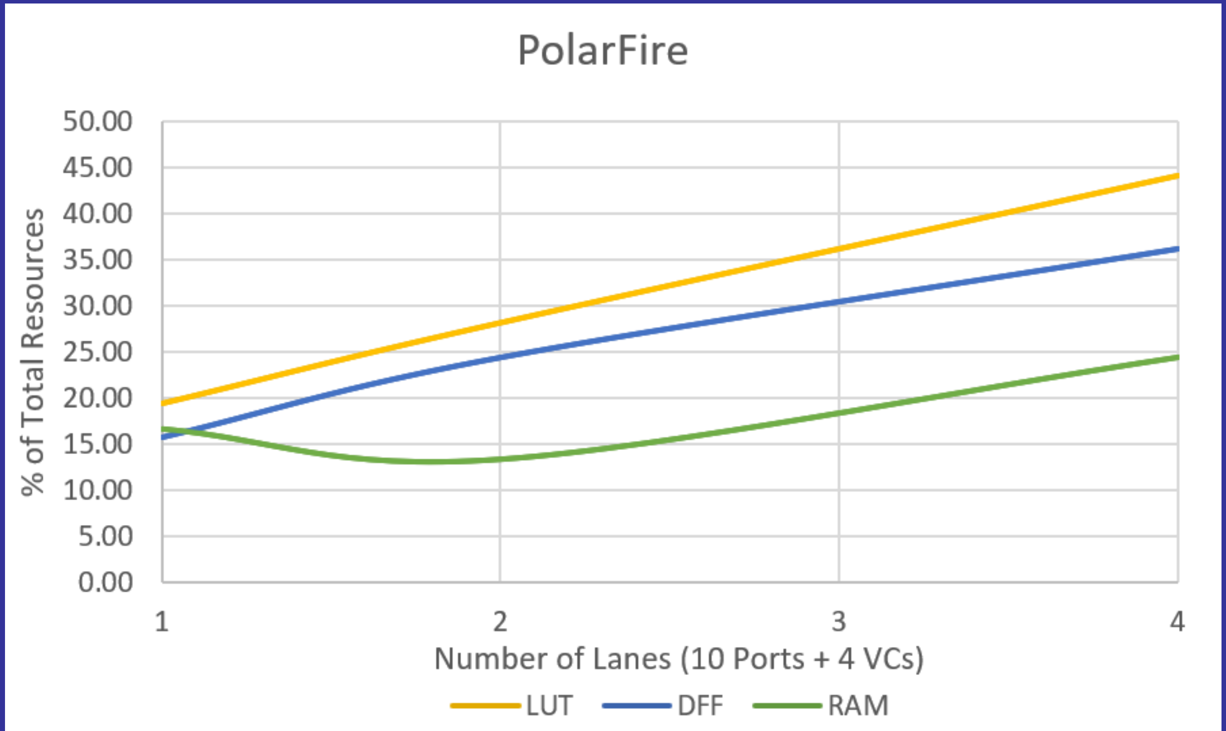
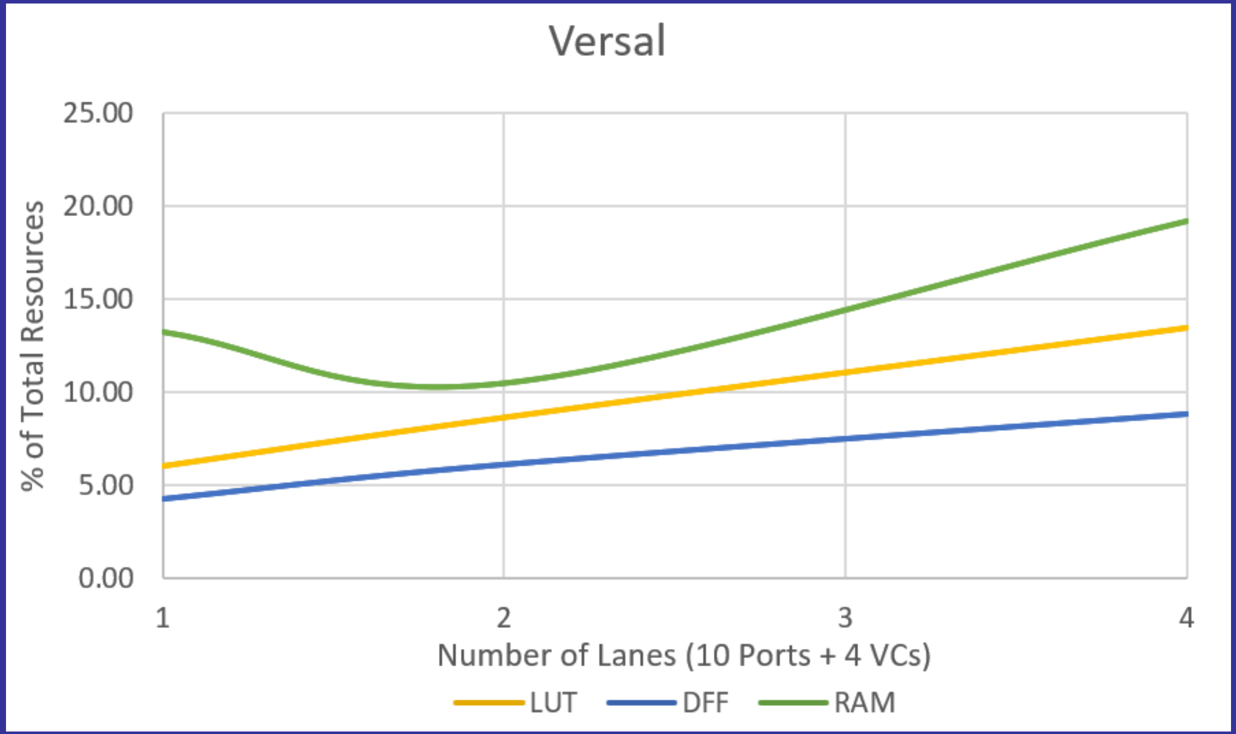
SpaceFibre Multi-Lane Routing Switch IP Resources





- Values for different configurations (2/4 Lanes and 6 Ports/2 VCs or 10 Ports/4 VCs) available the paper

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SpaceFibre Multi-Lane Routing Switch IP Resources

- Same number of VCs as before
  - 6 Port 2 VCs → 12 VCs
  - 10 Port 4 VCs → 36 VCs

- 1-lane Router
  - DFF/VC ~ 2200
  - LUT4/VC ~ 2600 (RTG4/PF)
  - LUT6/VC ~ 1500 (KUS/Versal)
- 2-lane Router
  - DFF/VC ~ 3500
  - LUT4/VC ~ 3900 (RTG4/PF)
  - LUT6/VC ~ 2200 (KUS/Versal)
- 4-lane Router
  - DFF/VC ~ 4500-5500
  - LUT4/VC ~ 6000 (RTG4/PF)
  - LUT6/VC ~ 3500 (KUS/Versal)

Conclusions

- STAR-Dundee provides SpaceFibre Interface and SpaceFibre Routing Switches IP Cores
  - Single-Lane and Multi-Lane *flavours* are both available

- The IPs have been designed specifically for space applications
  - Designed for the highest performance in RTG4 and other rad-had FPGAs
    - A simple SpFi interface only uses 2% of an RTG4 and ≤ 0.5% of the other FPGAs analysed
    - Multi-Lane can be implemented using 4% of an RTG4 and ≤ 1% of the other FPGAs
  - Exhaustive verification and validation, including radiation testing

Conclusions

- The IPs are easy to implement
  - IP Core can be used without knowledge of the internals of the SpaceFibre protocol
    - Very simple link management
    - Focus on how to process data, not on how it is transferred
  - Does not require specific timing or placement constraints
  - Reference designs available that show how to interconnect to different SerDes/Transceivers
  - End-user support by the same team that designed the IP and contributed to the SpaceFibre standard