Porting EagleEye to an ARM-based Processor

The Porting EagleEye to an ARM Based Processor project saw the porting of the Time and Space Partitioned (TSP) experimental EagleEye flight software from the SPARC to the ARM architectures.

The main advantage of ARM is primarily in the large software ecosystem with emulators, debuggers, compilers that is being actively maintained by both ARM and third parties. While most necessary tools exist for the SPARC based processors used in the European space segment, the SPARC architecture is these days essentially only maintained for the benefit of ESA based missions, leading to potential high tool upkeep costs. The ARM is one option to potentially share tool maintenance costs with other industries.

The second advantage of exploring ARM is the generally larger effort that has been spent on micro architectural CPU development, leading to in general higher clock frequencies (there exists ARM processors that run at more than 2 GHz).

The main disadvantage is that no current offerings come with 1553 or SpaceWire support on the SoC. The obvious routes to integrate such items is either to find discrete 1553 and SpW components, or to integrate an existing ARM design with existing 1553 and SpW IP cores supporting the AMBA busses (such as for example the devices available in GRLIB).

The porting showed that it is possible to not only port existing software, but also to integrate ARM instruction set simulators in existing simulation infrastructure.