# Microcontroller for embedded space applications

## TEC-ED & TEC-SW Final Presentation Day

**Cobham Gaisler**

**December 2018**

# GR716 – LEON3FT Microcontroller

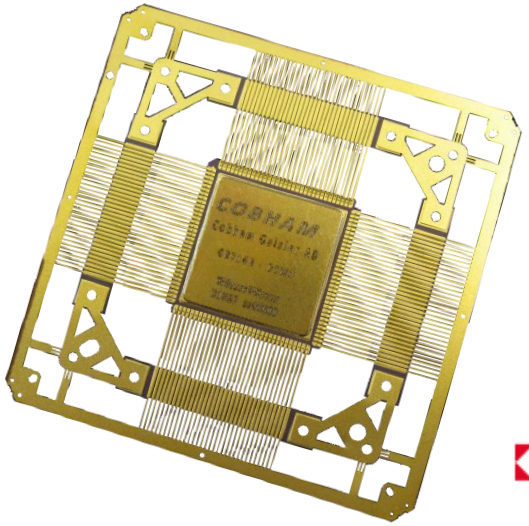
## Microcontroller for embedded space applications

### Objectives

The objectives of the activity are to define, design, manufacture and verify an ASIC containing the functionality of a mixed-signal microcontroller.

The device to be developed shall be easily accommodated in a large variety of platforms and payloads with moderate processing requirements, offering the possibility to distribute intelligence and I/O functionalities into the equipments, such as

- propulsion system control
- sensor bus control
- robotics applications control
- simple motor control
- mechanism control
- power control
- particle detector instrumentation
- radiation environment monitoring
- thermal control
- antenna pointing control
- remote terminal unit control
- simple instrument control



### Project information

- Contract: 40001117749/14/NL/AK
- TO: Claudio Monteleone
- Project Start: February 2014 (KO)
- Project End: March 2019 (FR – Planned)
- Contractor: Cobham Gaisler
- Companies and organizations involved:

esa

COBHAM Cobham Gaisler AB

imec

micross

KYOCERA

PENDER ELECTRONIC DESIGN

# GR716 – LEON3FT Microcontroller

## Microcontroller Introduction

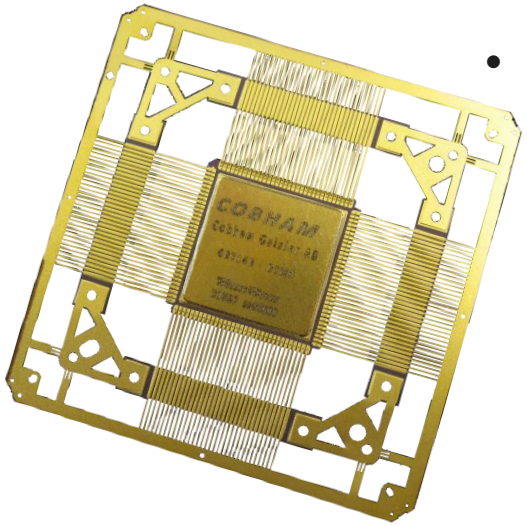
### Description

The GR716 features a fault-tolerant LEON3 SPARC V8 processor, communication interfaces and on-chip ADC, DAC, Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support for single 3.3V supply, ideally suited for space and other high-rel applications

### Applications

Support for many different standard interfaces makes the GR716 microcontroller is ideally fit for handling supervision and control in a satellite, such as

- propulsion system control
- sensor bus control
- robotics applications control
- simple motor control
- mechanism control
- power control
- particle detector instrumentation
- radiation environment monitoring
- thermal control
- antenna pointing control
- remote terminal unit control
- simple instrument control



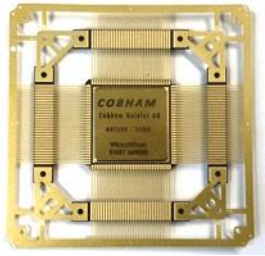

### Specifications

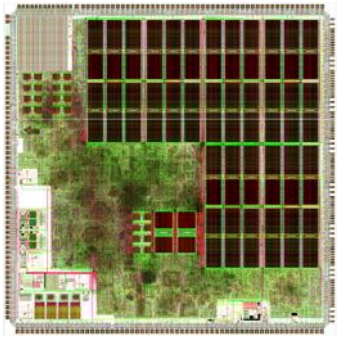
- System frequency up-to 50 MHz
- SpaceWire links up-to 100 Mbps
- CQFP132 hermetically sealed ceramic package
- Total Ionizing Dose (TID) up to 100 krad (Si, functional)
- Single-Event Latch-Up (SEL) to $LET_{TH}$ > 118 MeV-cm$^2$mg
- Single-Event Upset (SEU) below $10^{-12}$ bit error rate
- Support for single 3.3V supply

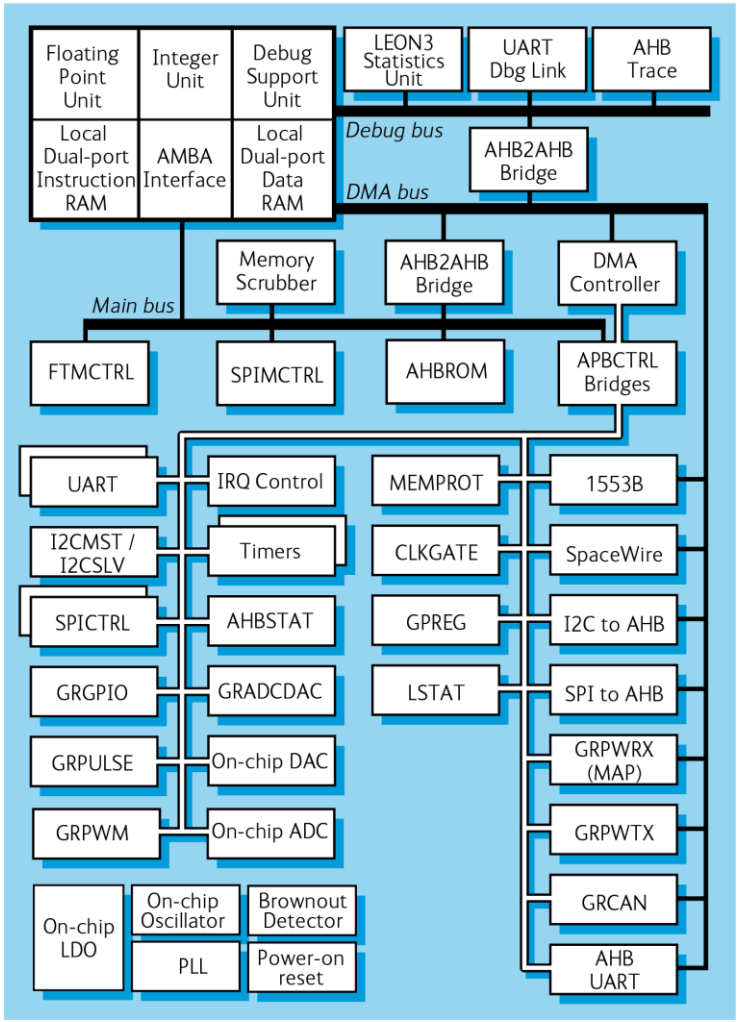
# GR716 – LEON3FT Microcontroller

## Microcontroller Features

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - 16-bit instruction set: LEON-REX - improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended
- DAC 12bits @ 3Msps, 4 channels
- Mixed General purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



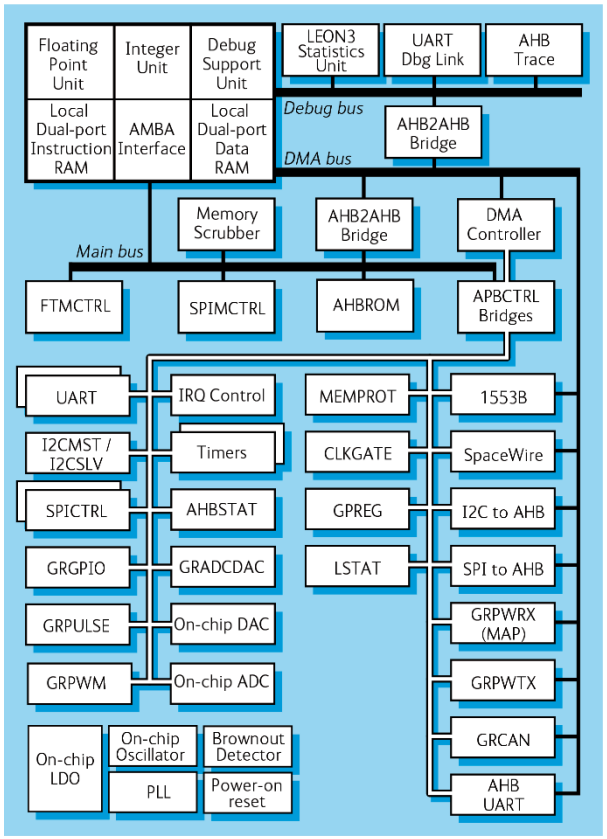




# GR716 – LEON3FT Microcontroller

## Key features – system support

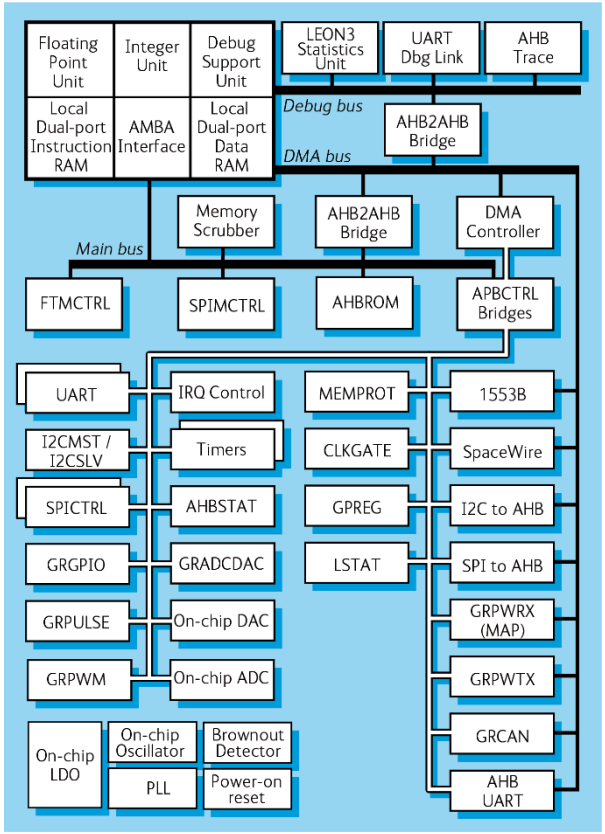
- On-chip voltage regulators for single supply support. Capability to sense core voltage for trimming of the embedded voltage regulator for low power applications.
- Power-on-reset, Brownout detection and Dual Watchdog for safe operation. External reset signal generation for companion chips.
- Crystal oscillator support and external clock reference
- One PLL for System and SpaceWire clock generation. In-application programming of system clock and peripheral clocks. System and SpaceWire clocks switches glitch free.
- Low power mode and individual clock gating of functions
- Temperature and core voltage sensor
- External voltage reference for precision measurement
- Statistics unit for profiling of the system



# GR716 – LEON3FT Microcontroller

## Key features - peripherals

- SpaceWire with RMAP and Time Distribution Protocol
- Redundant MIL-STD-1553B BRM (BC/RT/BM) interface
- Two CAN 2.0B bus controllers
- Six UART ports, with 16-byte FIFO
- Two SPI master/slave serial ports
- One SPI controller. Hardware support for SPI for Space slave
- Two I2C master/slave serial port
- PacketWire interface
- PWM with up-to 16 channels
- Up to 64 General input and outputs (GPIO) with external interrupt capability, pulse generation and sampling.
- 4x single ended Digital to Analog Converters (DAC), 12-bit at 3MS/s
- 4x differential or 8x single ended Analog to Digital Converters (ADC) dual sample and hold 11-bit at 200KS/s, with programmable pre-amplifier and support for oversampling
- External ADC and DAC support up to 16-bit at 1MS/s

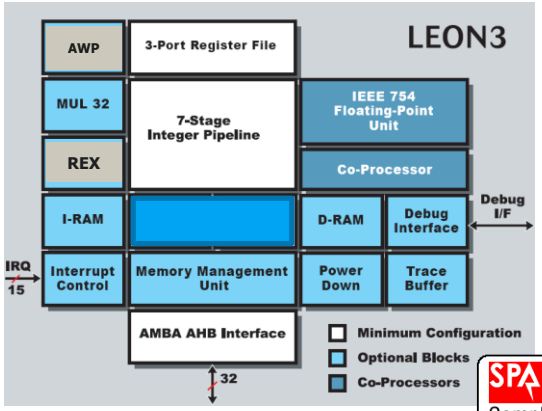


# GR716 – LEON3FT Microcontroller

## Key features – processor and memory

### Processor core

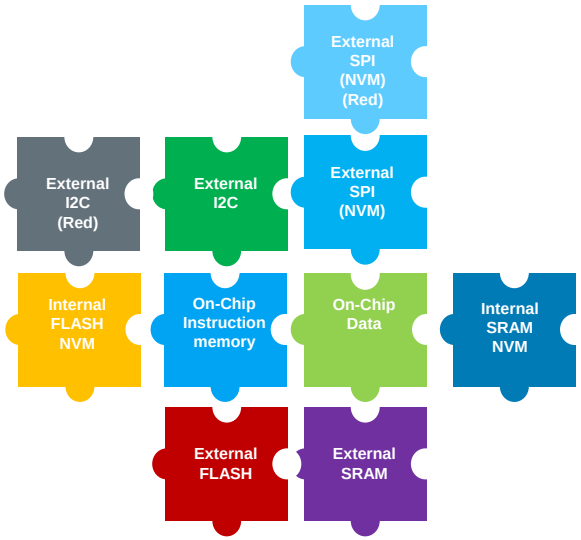
- Fault-tolerant SPARC V8 processor with 31 register windows and support 16-bit instruction operation (REX)
- Double precision IEEE-754 floating point unit
- Memory protection units with 8 zones and individual access control of peripherals
- Advanced on-chip debug support unit with trace buffers and statistics
- Deterministic software execution and non-intrusive debugging
- Fast context switching (PWRPSR, AWP, register partitioning, SVT, MVT)
- Interrupt zero jitter delay




*Fault-tolerant SPARC V8 processor*

### Memory support

- 192KiB EDAC protected tightly coupled memory with single cycle access from processor and ATOMIC bit operations
- Dedicated SPI Memory interface with boot ROM capability and EDAC
- I2C memory interface with boot ROM capability
- 8-bit SRAM/ROM I/F with support up to 16MiB ROM and 256MiB SRAM
- Scrubber with programmable scrub rate for all embedded memories and external PROM/SRAM and SPI memories
- Redundant boot memory (PROM/SRAM/SPI/I2C/NVRAM)
- Application software container for checking software integrity using CRC
- Boot from internal SRAM, external PROM/FLASH/SRAM/SPI/I2C memory




*Support of many variety of memory types*

# GR716 – LEON3FT Microcontroller

## Boot options

- Remote boot (no software or external memory required)
  - UART
  - SpaceWire RMAP
  - SPI / SPI4SPACE
  - I2C
- Internal Boot PROM supported boot (configures the I/0s):
  - External PROM/SRAM
  - External SPI Memory
  - Embedded NVRAM/PROM/SRAM in package (future option)
  - External I2C PROM
- Direct boot (bypass internal boot prom)
  - External PROM/SRAM
  - External SPI Memory
  - Embedded NVRAM/PROM/SRAM in package (future option)

**Select Boot option via external pins**

# GR716 – LEON3FT Microcontroller

## Key features – Processor Performance

- On-chip SRAM w/ Dual Port, EADC and Scrubbing, Radiation Tolerant
  - 192 KiB Instruction and Data – User defined mix of instruction vs data
- Integrated Floating Point Unit
  - IEEE-754 compliant floating-point unit, supporting both single and double precision operands
- Memory Protection Unit
  - 8 zones and individual access control of peripherals
- System Clock frequency: 50MHz
  - Dynamic reconfiguration of system clock for low power
- System Benchmark
  - Dryshtone: 1.24 Dhrystone / MHz
  - Whetstone: 0.43 Whetstone / MHz
  - CoreMark: 2.21 CoreMark / MHz
  - EDAC, Scrubbing, DMA transfers and debug are non-intrusive and do not affect performance

COBHAM
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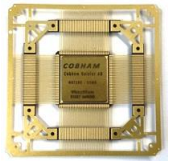


| | | |
|---|---|---|
| **Processor** | **Processor core** | LEON3FT |
| | **Architecture** | SPARC V8 w. V8e subset |
| | **RISC type** | 32bit |
| | **Instruction set** | SPARC V8(e), LEON REX |
| | **Pipeline stages** | 7 |
| | **Tightly coupled memory** | 192 KiB |
| | **FPU** | IEEE-754 |
| | **MPU** | yes |
| | **Mul/Div** | Mul/Div |
| | **Peripheral DMA** | multi-channel |
| | **Interrupt handling** | deterministic |
| | **Performance counters** | yes |
| | **Debug unit** | yes |
| | **Embeded trace buffer** | yes |
| | **Processor MHz** | 50 |
| **Performance** | **Dhrystone / MHz** | 0.93 / 1.24 / 1.46 |
| | **Whetstone / MHz** | 0.43 |
| | **CoreMark / MHz** | 2.21 |

** Dhrystone Performance: Compiler Versions and Ground Rules application note is available at https://www.gaisler.com/index.php/information/app-tech-notes*

## Real Time features and enhancements

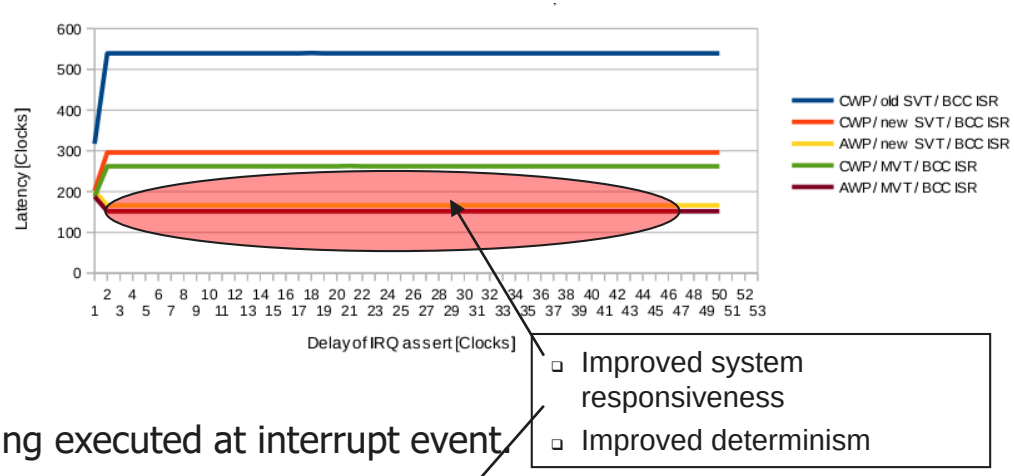
- Fast context switching (PWRPSR, AWP, Register partitioning, SVT, MVT)
  - Very low interrupt response time can be achieved by switching register window
  - A unique trap handler can executed in its own register window (Register partitioning)
  - Benefits from register partitioning:
    - Extremely low interrupt latency
    - All local and input registers are preserved
    - Nested interrupt are supported by hardware
- Interrupt zero jitter delay
- Deterministic software execution and non-intrusive debugging
  - Advanced on-chip debug support unit with trace buffers and statistic unit

- Custom flat register window model
- Typical flat register window model (MVT) using BCC 2.0.2
- Typical flat register window model (SVT) using BCC 2.0.2

| | Typical | | Worst | |
|---|---|---|---|---|
| | IRQ to ISR | ISR EXIT | IRQ to ISR | ISR EXIT |
| BCC 2.0 Custom ISR | 11 | 6 | 11 | 6 |
| BCC 2.0 flat ISR | 22 | 15 | 37 | 15 |

## Real Time features and enhancements

- Fast context switching (PWRPSR, AWP, Register partitioning, interrupt mapping, SVT, MVT)
- Interrupt zero jitter delay
- Advanced on-chip debug support unit with trace buffers and statistic unit
- Deterministic software execution and non-intrusive debugging
- Interrupt Service Routine (ISR) is a user function
  - Normal C function
  - Nesting and chaining with libbcc
- Fast interrupt
  - SPARC assembly
  - CPU register limitations
- Measurements on LEON3 GR716:
  - Unit: #cycles.
  - (cycles have to be added)
    for long instructions (FPU, DIV, etc) being executed at interrupt event.




| | Typical | | Worst | |
|---|---|---|---|---|
| | IRQ to ISR | ISR EXIT | IRQ to ISR | ISR EXIT |
| BCC 1.0 ISR | 196 | 139 | 322 | - |
| BCC 2.0 ISR | 100 | 73 | 200 | 146 |

## Flat register Model

- Very low interrupt response time can be achieved by switching register window (Flat Register Window)
- Each unique trap handler is to executed in its own register window
- Benefits from flat register window:
  - Extremely low interrupt latency
  - All local and input registers are preserved
  - Nested interrupt are supported by hardware
- Examples is provided with Software environment version 2.0.2 and later

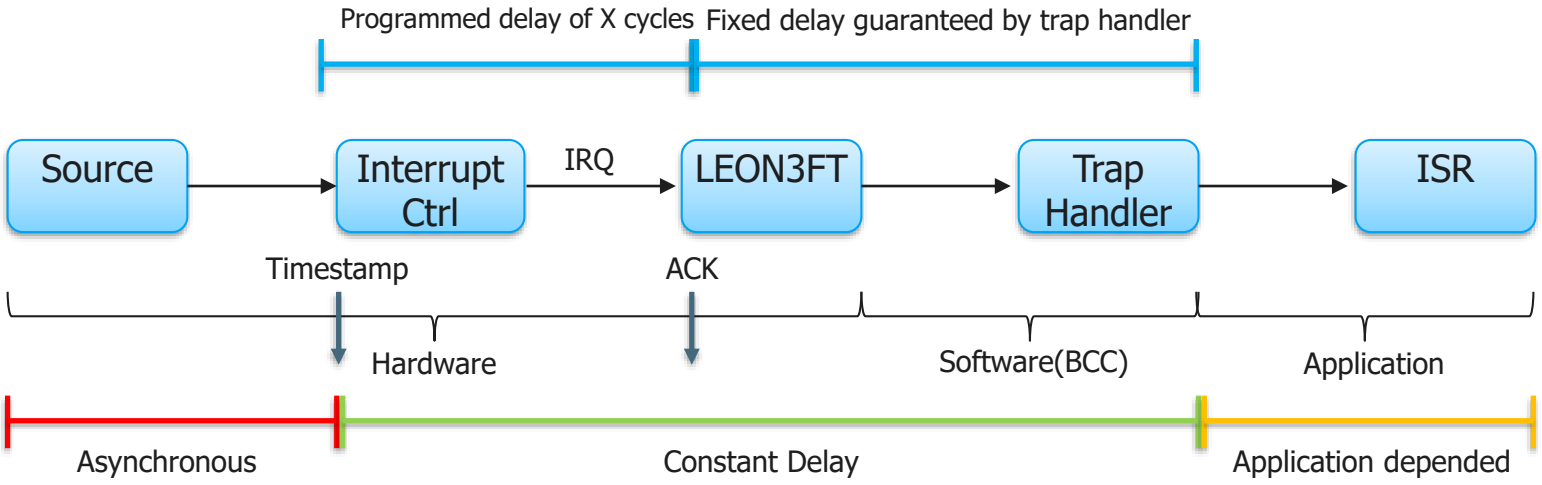
- Custom flat register window model
- Typical flat register window model (MVT) using BCC 2.0.2
- Typical flat register window model (SVT) using BCC 2.0.2

| | Typical | | Worst | |
|---|---|---|---|---|
| | IRQ to ISR | ISR EXIT | IRQ to ISR | ISR EXIT |
| BCC 1.0 ISR | 196 | 139 | 322 | - |
| BCC 2.0 ISR | 100 | 73 | 200 | 146 |
| BCC 2.0 Custom ISR | 11 | 6 | 11 | 6 |
| BCC 2.0 flat ISR | 22 | 15 | 37 | 15 |

# GR716 – LEON3FT Microcontroller

## Key features - constant interrupt delay

- Support for applications requiring constant interrupt delay
- Programmable delay in processor from interrupt assertion -> start of trap handler.
  - Ongoing instruction will finish but 'jump' instruction to trap handler will be held for time set by user. (worst case is floating point instructions)
- Timestamp of interrupts and local counter in processor
  - Access to counter in processor and single cycle access to local instruction memory guarantees no extra delay or jitter
- Possible to set fix delay for trap handler to increase system determinism
- Make use of all 31 available register windows not to get window overflow or overflow



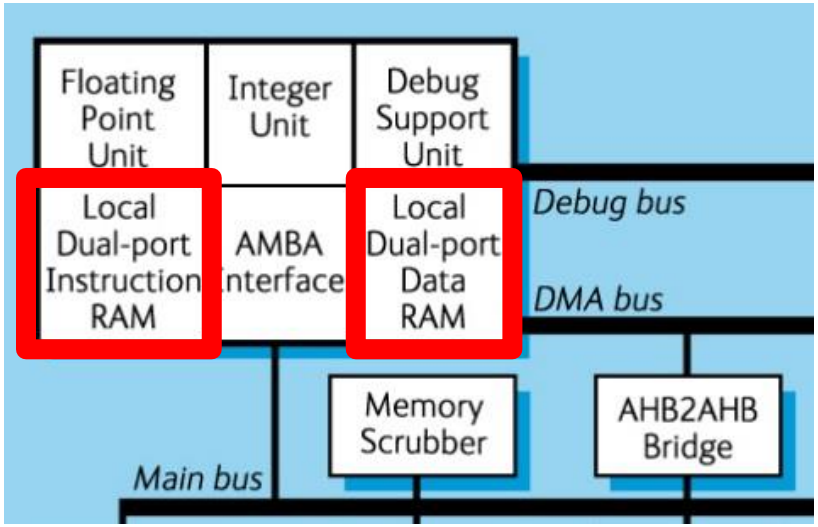
# GR716 – LEON3FT Microcontroller

## Key features – tightly coupled local memory

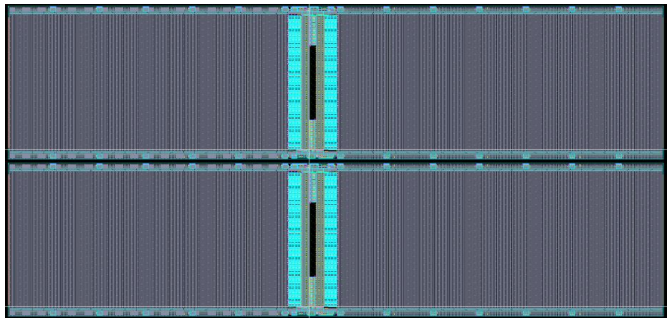
The microcontroller has **local instruction** and **data** on-chip RAM connected to the LEON3FT processor

Local RAM features:

- 128KiB Instruction memory
  - single cycle access
- 64KiB Data memory protected by EDAC
  - single cycle access
- Scrubber support
- Dual port access enables
  - seamless uploading of new program
  - DMA traffic direct into data memory without affecting program execution or data fetch
  - scrubber access and EDAC correction without affecting program execution or data fetch
- Support atomic bit-filed operations
  - OR, AND, XOR, Set & Clear
- Instructions can be executed from data memory and data can be stored in instruction memory




*Local instruction and data memory is located close to LEON3FT processor for single cycle access*

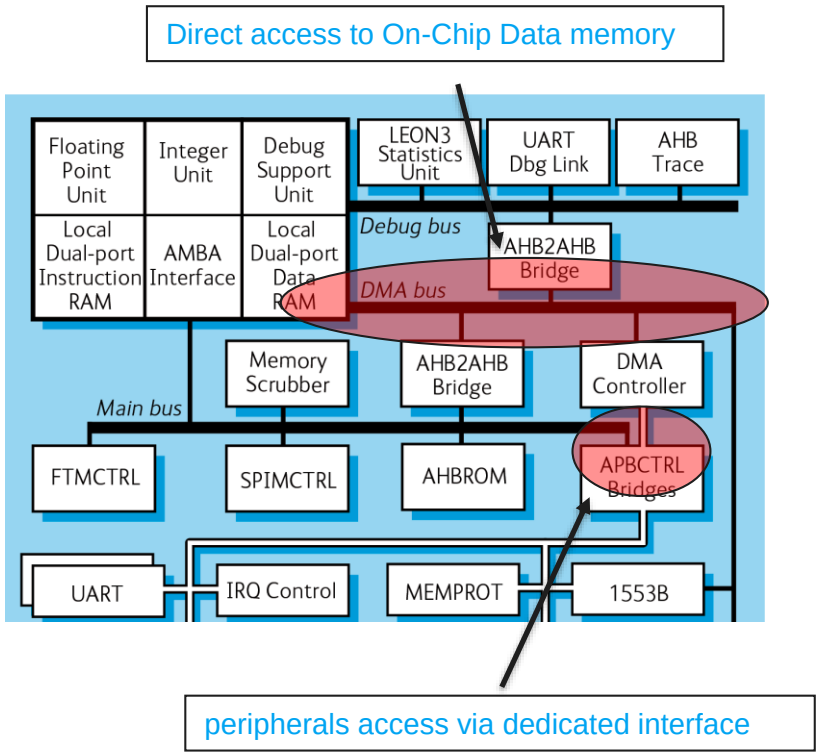


*Rad Hardened High density SRAM Integration - Integrated error detection and correction. One error can be corrected and two errors can be detected, which is performed by using a (32, 7) BCH code*

# GR716 – LEON3FT Microcontroller

## Key features - Direct Memory Access Controller

- System DMA overview
  - 4 individual DMA cores (each core has multiple channels)
  - Multiple AHB interface and direct access to APB Peripheral
- Programmable DMA transfers through stand-alone DMA controller
  - Responds to Interrupts, Polling register, Loop support
  - Responds to combination of interrupt and register polling
- Programmable DMA user scenarios
  - Offload processor
  - Autonomous transfers from/to ADC/DAC without CPU intervention
  - Autonomous transfers between: UART to UART, SPI to SPI or I2C to I2C
  - Transfer data, update register synchronous to event e.g. PWM output levels

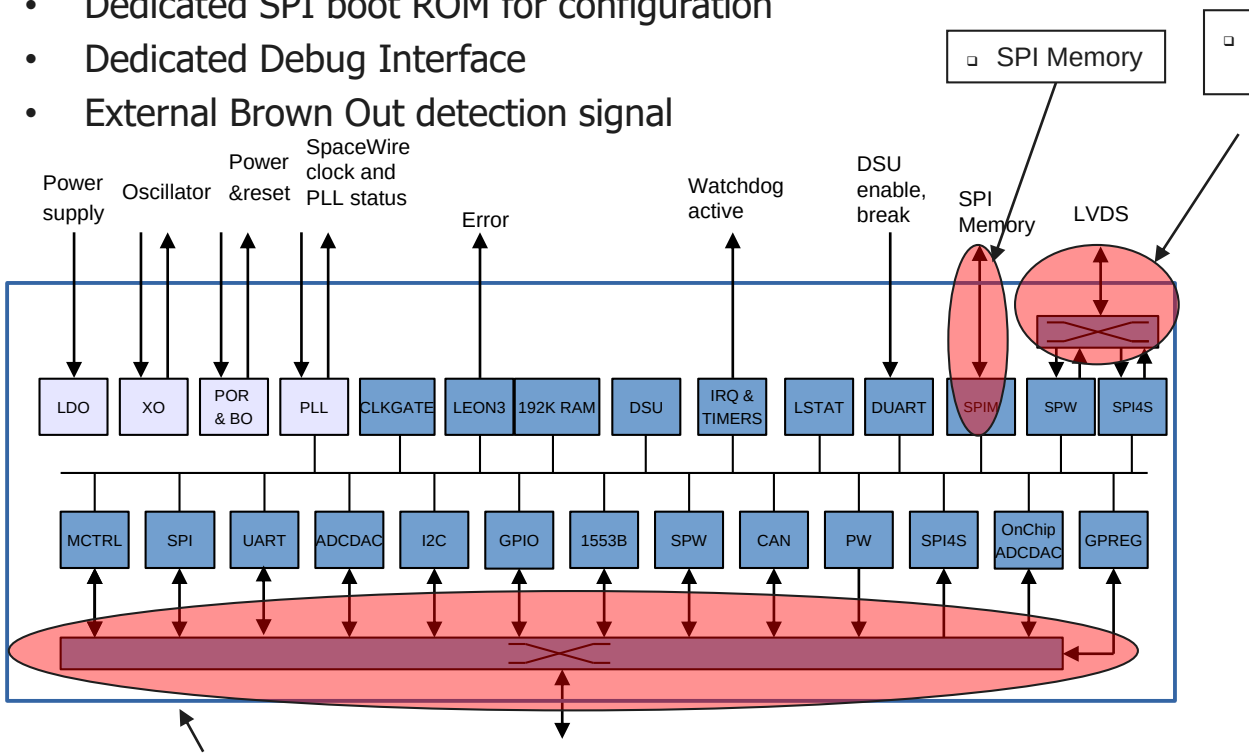


# GR716 – LEON3FT Microcontroller

## Key features – inputs/outputs

### I/O

- Configurable I/O selection matrix with mixed signals, internal pull-up/pull-down resistors
- LVDS transceivers for SpaceWire or SPI4Space
- Clock and reset for companion chips e.g. GPIO-expander, external RAM etc.
- Dedicated SPI boot ROM for configuration
- Dedicated Debug Interface
- External Brown Out detection signal

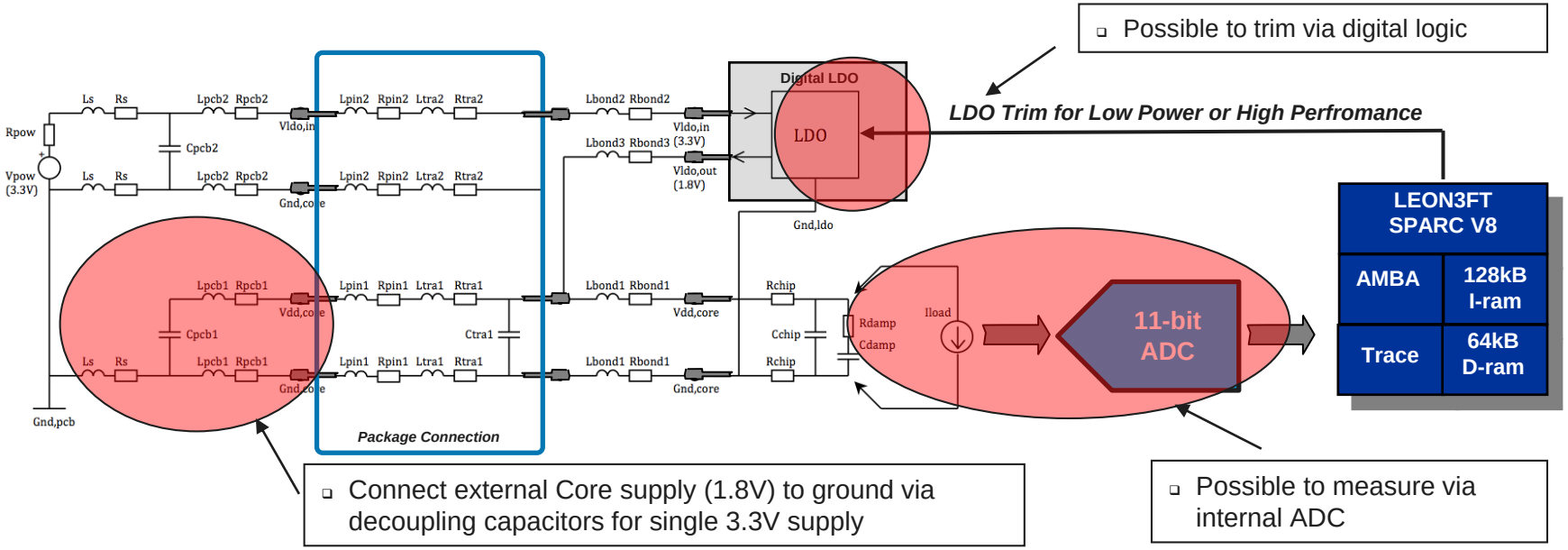


# GR716 – LEON3FT Microcontroller

## Key features – single supply

- Single 3.3V±0.3V supply or separate Core Voltage 1.8V±0.18V, I/O voltage 3.3V±0.3V
- Brown-Out detection for all supplies (sense in package)
- On-chip Linear regulators with possibility to trim core voltage for lowest power consumption
- Core Voltage sense via internal ADC.

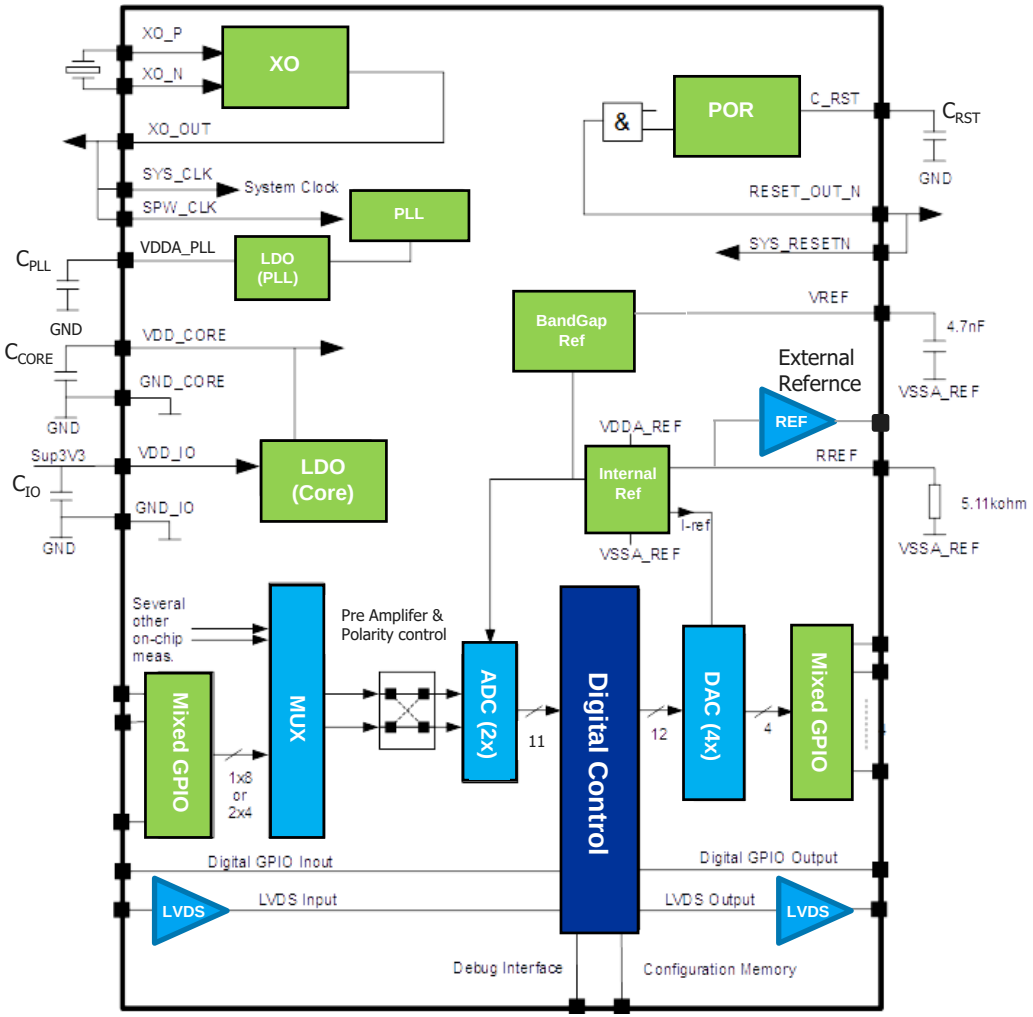
- Monitoring of core voltage for detecting aging
- Core temperatur can be measured simultaniuously



# GR716 – LEON3FT Microcontroller

## Key features – a minimum of external parts

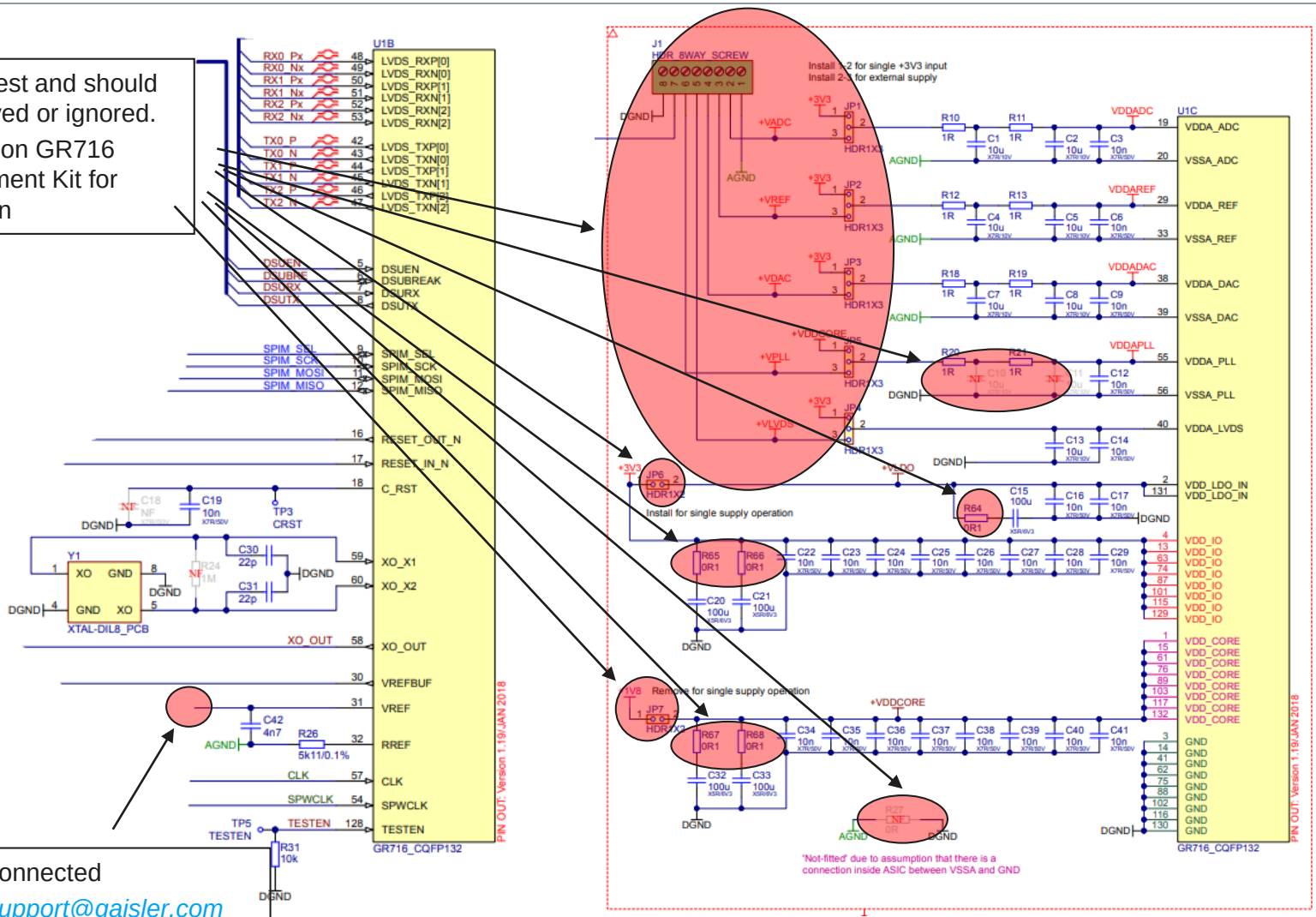
- Minimum application requirements:
  - 3.3V supply
  - frequency resonator in the range of 5MHz to 25MHz
  - de-coupling capacitor
  - reference resistor
- Minimum application enables
  - system clock and reset
  - remote access to GR716 via SpaceWire, SPI, UART and I2C
  - access to all functions



# GR716 – LEON3FT Microcontroller

## Key features – a minimum of external parts – In practice…

- Internal test and should be removed or ignored.
- Avaiable on GR716 Development Kit for evaluation




- Keep unconnected
- Contact *support@gaisler.com*

# GR716 – LEON3FT Microcontroller

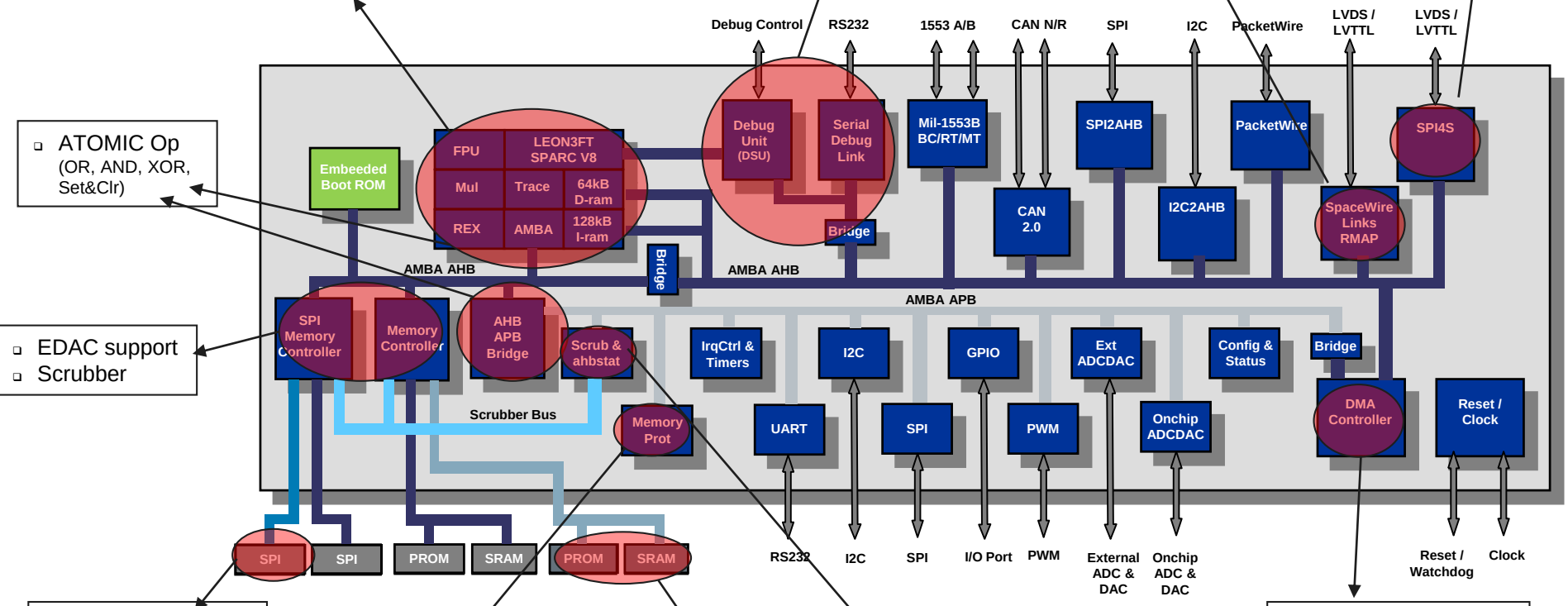
## Digital architecture – plenty is not enough

- Support for AWP and fast context switch
- FPU and 32bit MUL
- 192KiB EDAC Protected Memory
- Single cycle instruction execution
- Determenistic execution and interrupt latency

- Debug Link
- Instruction/AHB trace
- Non-Intrusive

- RMAP Support
- TDP Support

- HW support for Protocol level 0,1 and 2




- ATOMIC Op (OR, AND, XOR, Set&Clr)

- EDAC support
- Scrubber

- Dedicated I/O pins available

- Memory Protection
- Access Restriction

- Support for future RAM in package

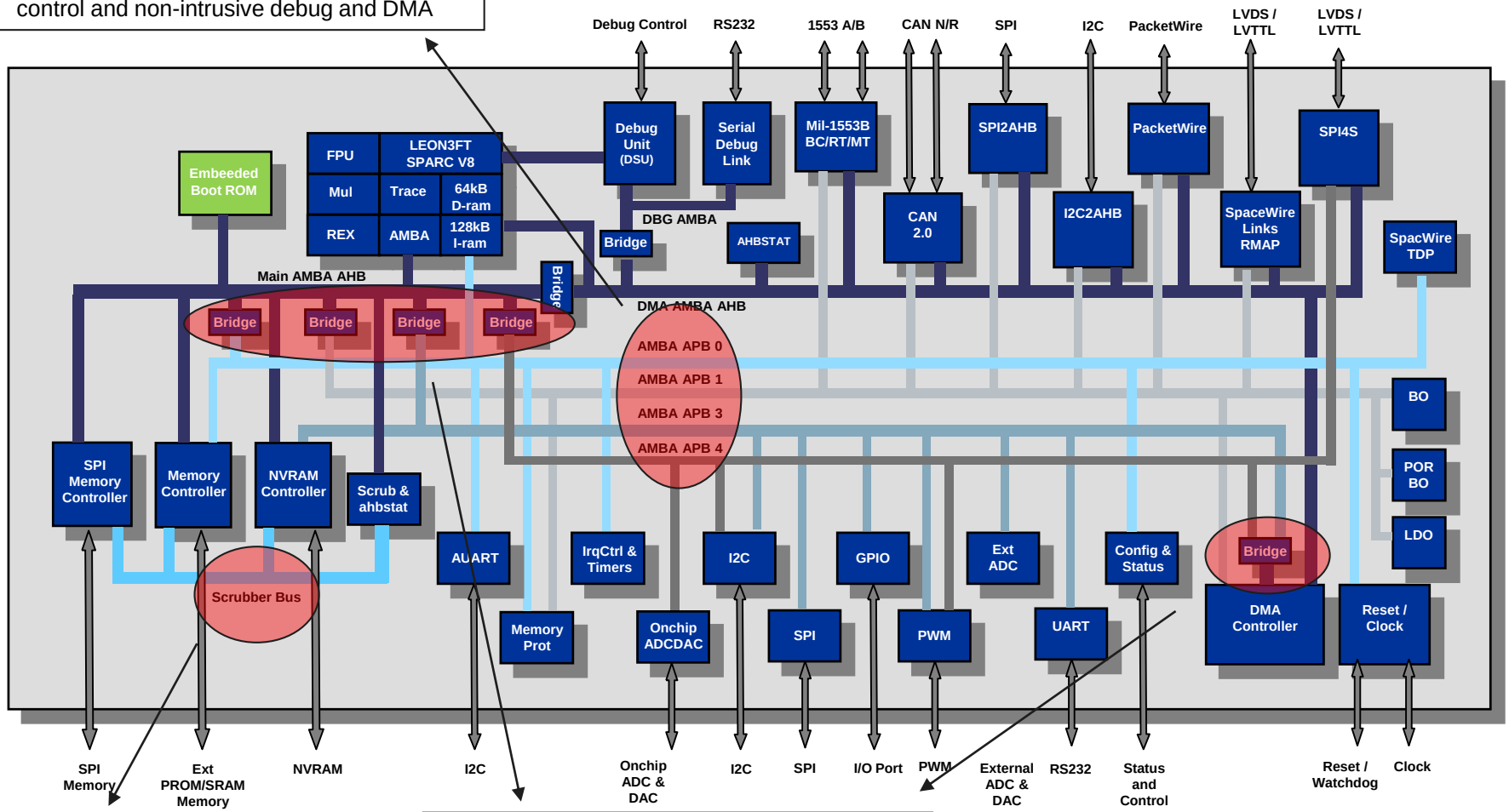
- Scrubber Direct Access
- Statistics for profiling
- System Error detection

- DMA with direct access to periherals

# GR716 – LEON3FT Microcontroller

## Digital architecture – bus structure

- Multiple APB busses for master access control and non-intrusive debug and DMA

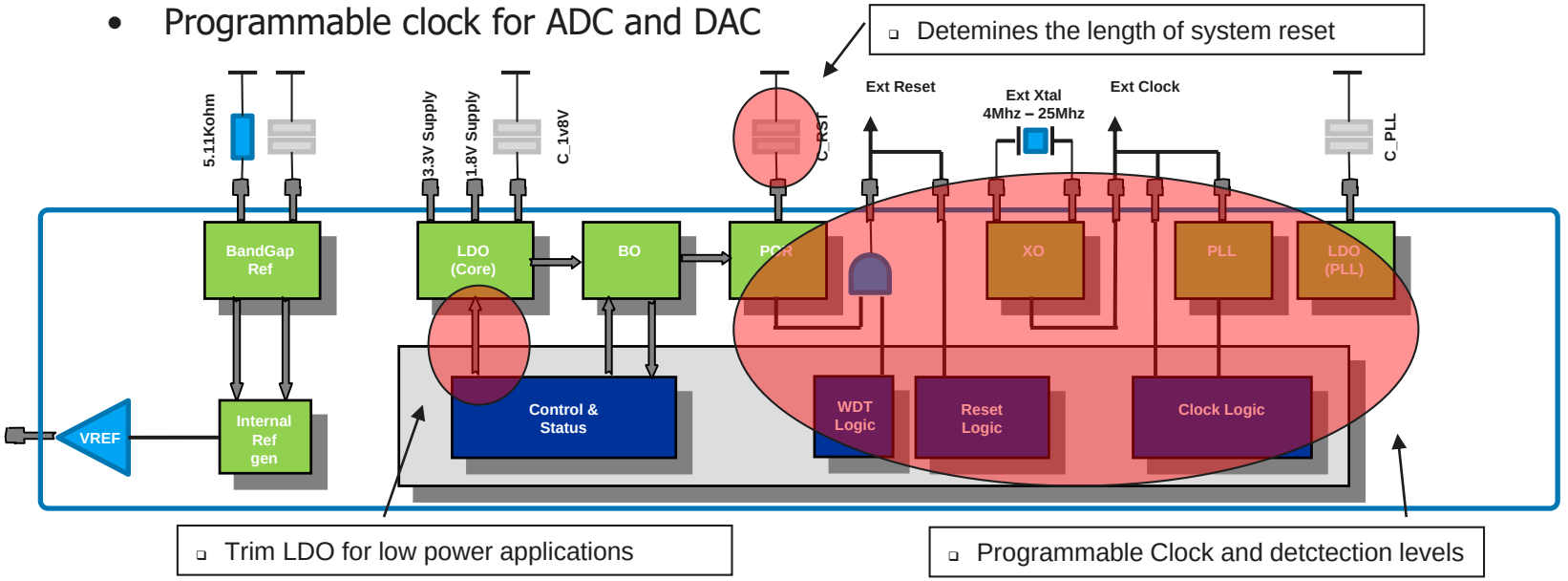



- Scrubber do not affect master bus
- Access control build-in to APB controller

# GR716 – LEON3FT Microcontroller

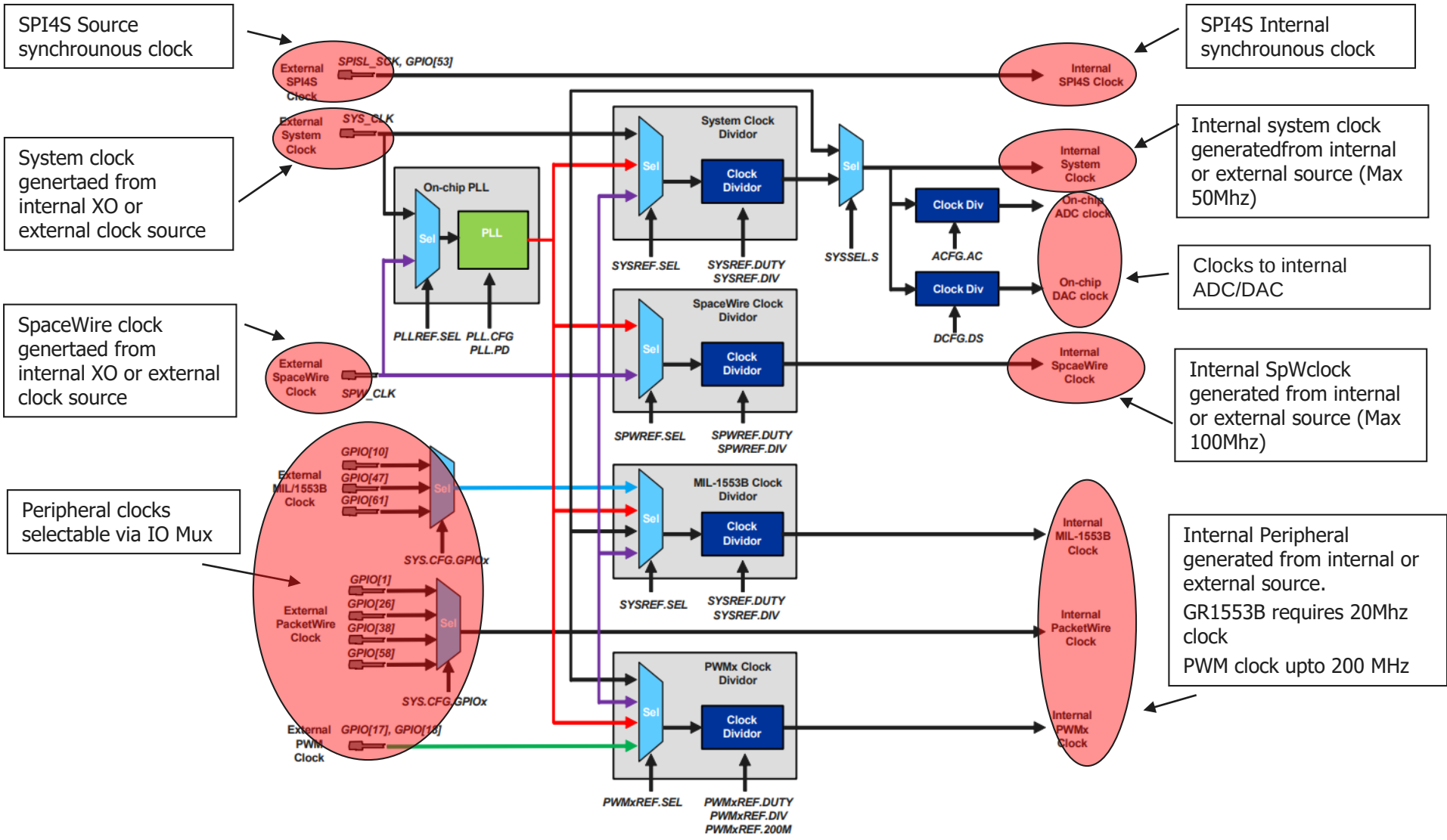
## Reset and Clocking Scheme

- Integrated XO, PLL, Power On Reset(POR) and Brown-Out(BO)
  - External system clock and reset
  - Crystal Oscillator support for frequencies from 4Mhz to 25Mhz
  - Programmable Rad-Hard PLL for generation of system and SpaceWire clock
  - Brown out detection on all major power domains (IO, Core, ADC, DAC, REF and PLL)
- Programmable Peripherals clocks
  - Select internal generated clock or external clock for flexibility
  - Programmable clock for ADC and DAC



# GR716 – LEON3FT Microcontroller

## Reset and Clocking Scheme – Internal Clock Generation



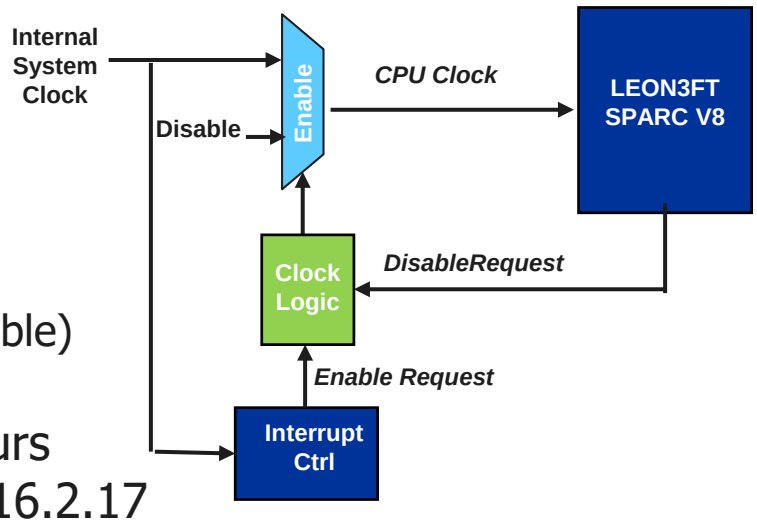
# GR716 – LEON3FT Microcontroller

## Reset and Clocking Scheme – Internal Clock gate and reset

- Processor Idle state (Deep Sleep)
  - Processor and Memories can enter idle state at any time

```
// Call Idle state from Software
bcc_power_down();

// .. Or Request power down mode
wr %g0, %asr19
```




  - Processor will wake up on events (programmable)
  - Disable processor clock to save power
  - Pipeline is halted until next interrupt occurs
  - More information see Datasheet section 16.2.17

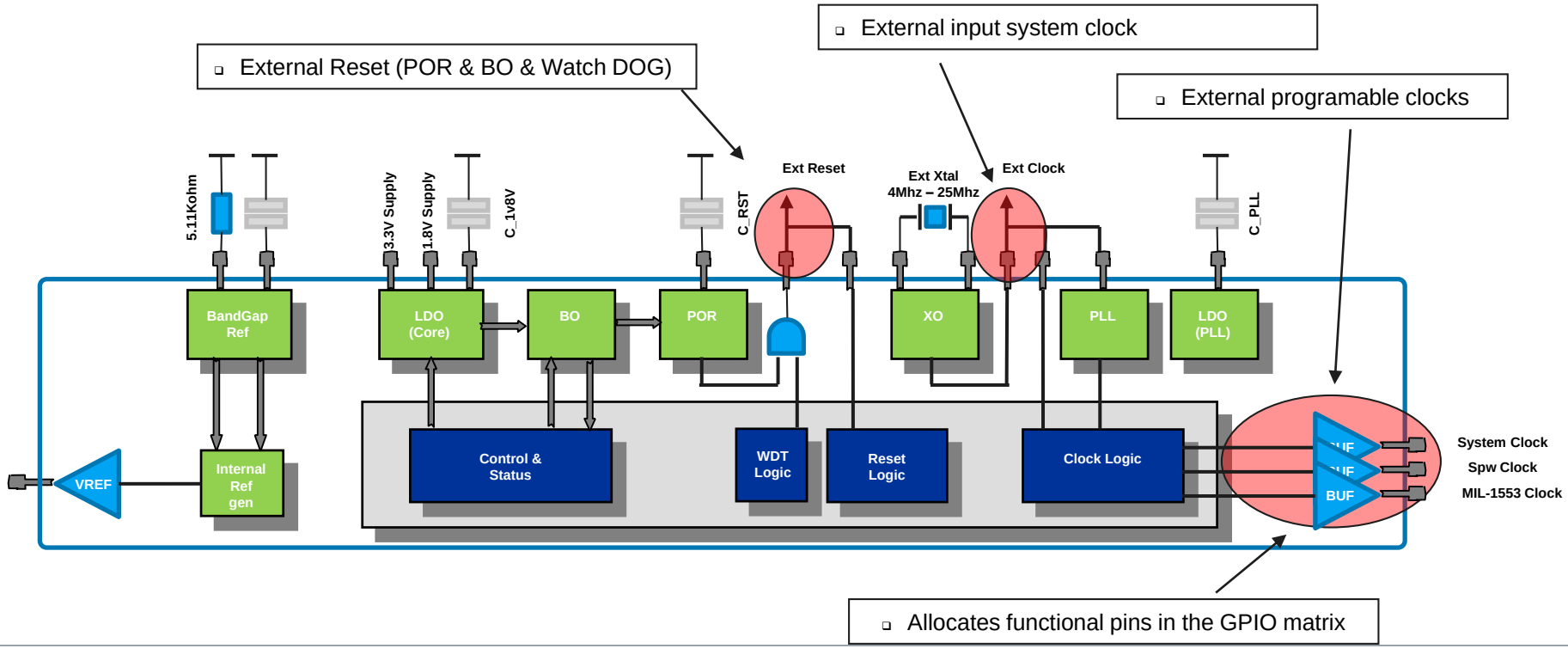
- Peripheral clock and reset control
  - Individual clock and reset control of all peripherals and functions
  - After startup minimum number of peripherals and functions are enabled

- System, SPW, MIL-1553B and PWM clock control
  - Individual control of clocks using internal dividers

# GR716 – LEON3FT Microcontroller

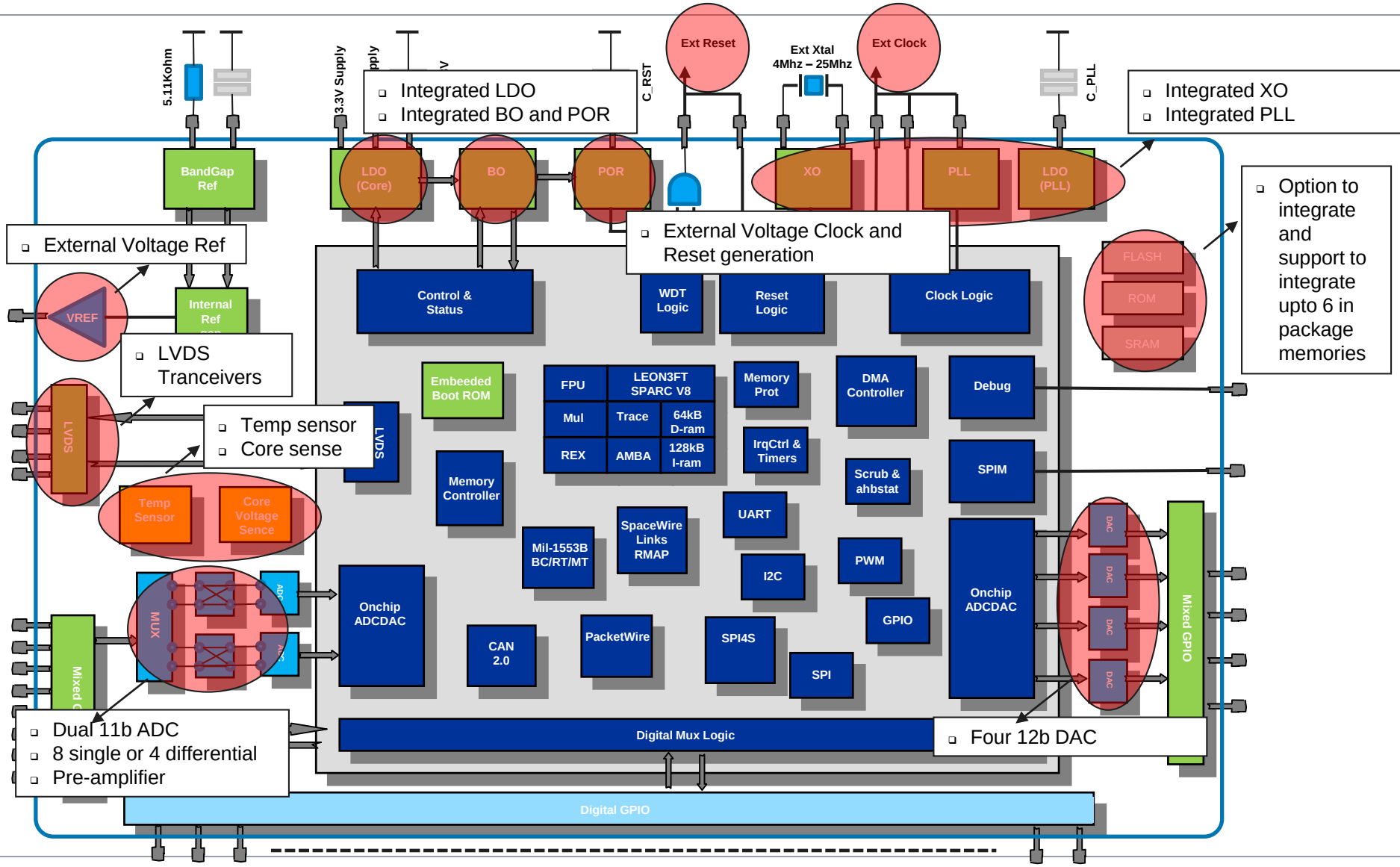
## External Reset and Clocking Scheme

- External Reset
  - Power on reset
  - Brown Out detection and Watch Dog
- Internal programmable clocks
  - Possible to output internal generated System, SpaceWire and MIL-1553 clock



# GR716 – LEON3FT Microcontroller

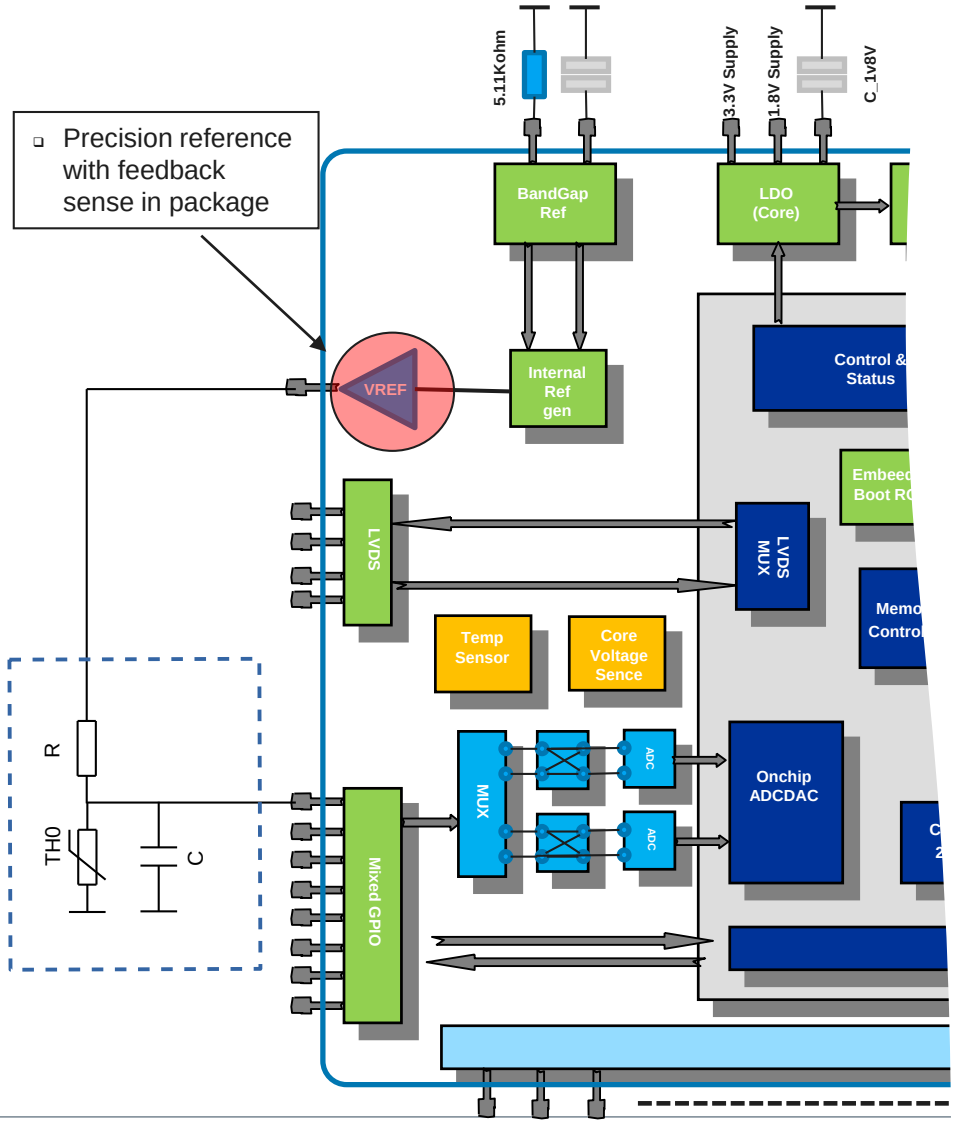
## Analogue architecture – Schematic Overview



# GR716 – LEON3FT Microcontroller

## Analog feature Overview – External precision reference

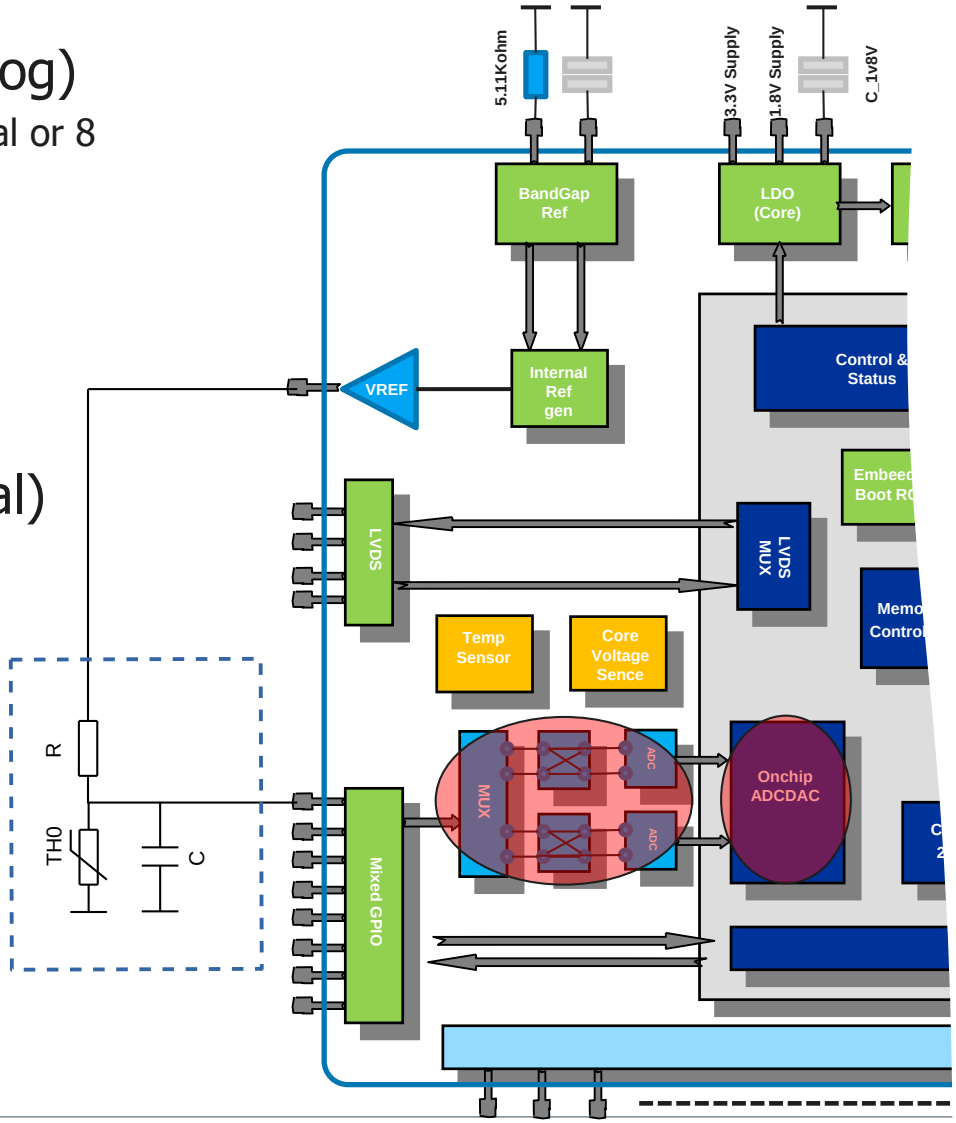
- Thermistor Measurements Application
- Internal ADC and External Thermistor use the same precision voltage reference
- Internal precision voltage reference can be used as external voltage reference on PCB. (Max 2mA load. Higher load application requires external buffer)
- Sense in package for precision reference



# GR716 – LEON3FT Microcontroller

## Analog feature Overview – On-chip Analog to Digital – Digital Help Functions

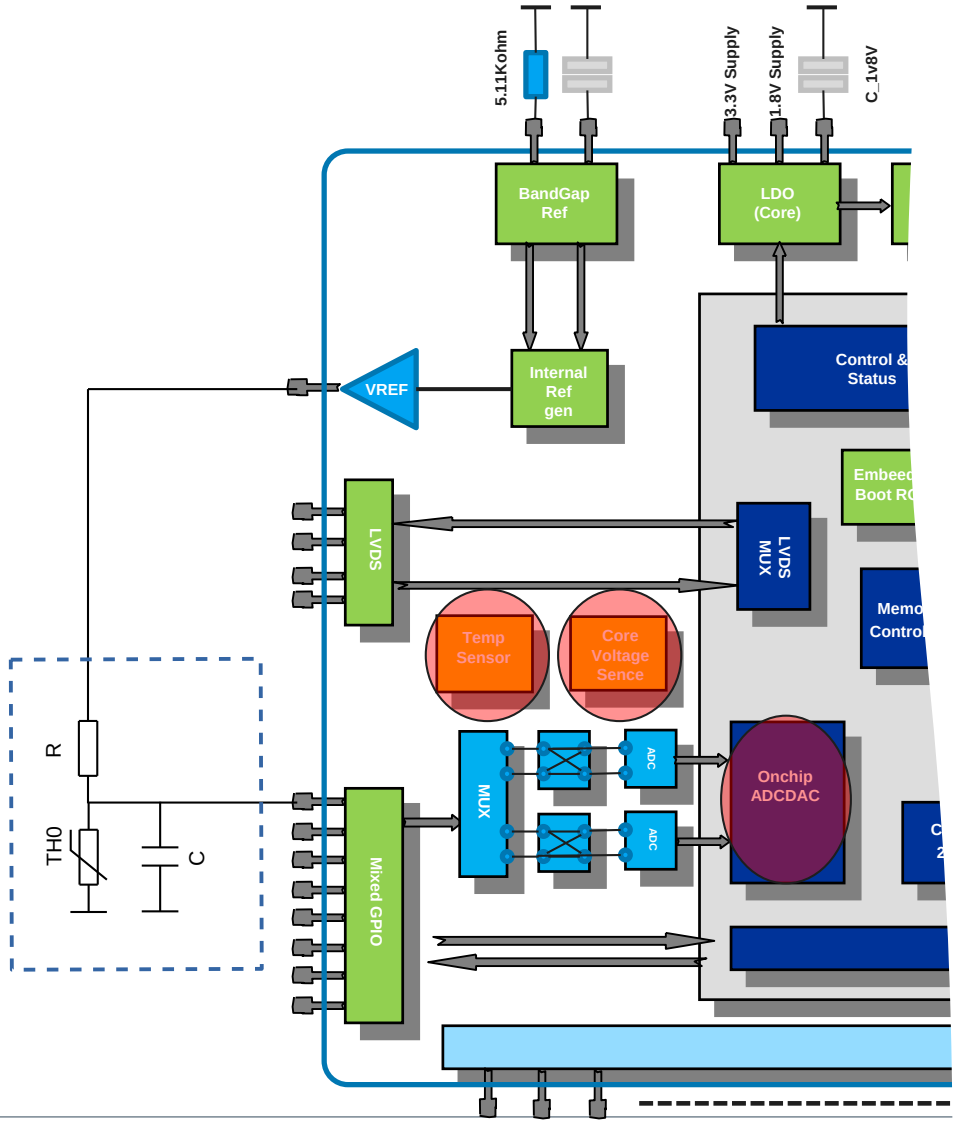
- Analog to Digital Converter (Analog)
  - 11bits @ 300Ksps, 4 channel differential or 8 channel single ended (possible to mix)
  - Pre-amplifier (0dB, 6dB or 12dB)
  - Dual Sample and hold circuits
  - Temperature sensor
  - Monitor core voltage
- Analog to Digital Converter(Digital)
  - Oversampling support
  - Sequence programming
  - Automatic level supervision
  - Automatic pre-amplifier control
  - Programmable sample triggers. Possible to trigger on internal and external events
  - Automatic channel arbitration
  - DMA support, automatic transfer of data to local or external RAM
  - Low noise sampling support



# GR716 – LEON3FT Microcontroller

## Temp Sensor and Low Power Mode (Core Voltage)

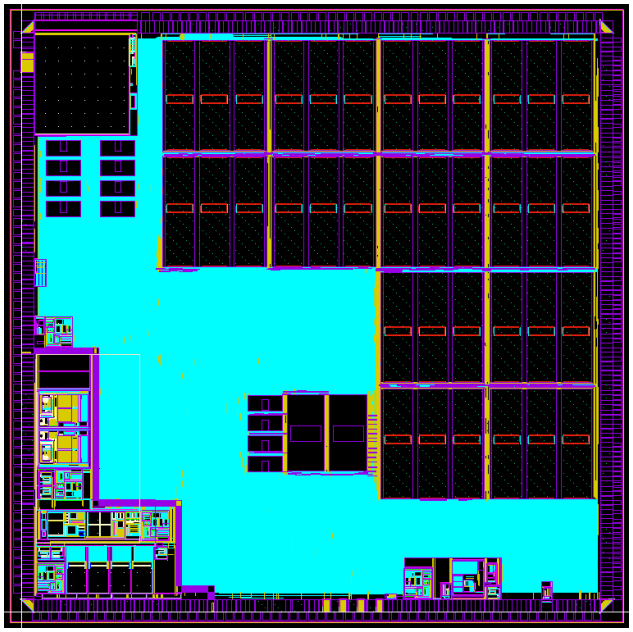
- Onchip Temperature Sensor
  - Temperature sensor
  - Measured via on chip ADC #0 (connected via separate channel)
- Core Voltage Sense
  - Monitor core voltage
  - Trim Voltage for low of high power applications
  - GR716 always starts up using high power mode
  - Measured via on chip ADC #1 (connected via separate channel)



# GR716 – LEON3FT Microcontroller

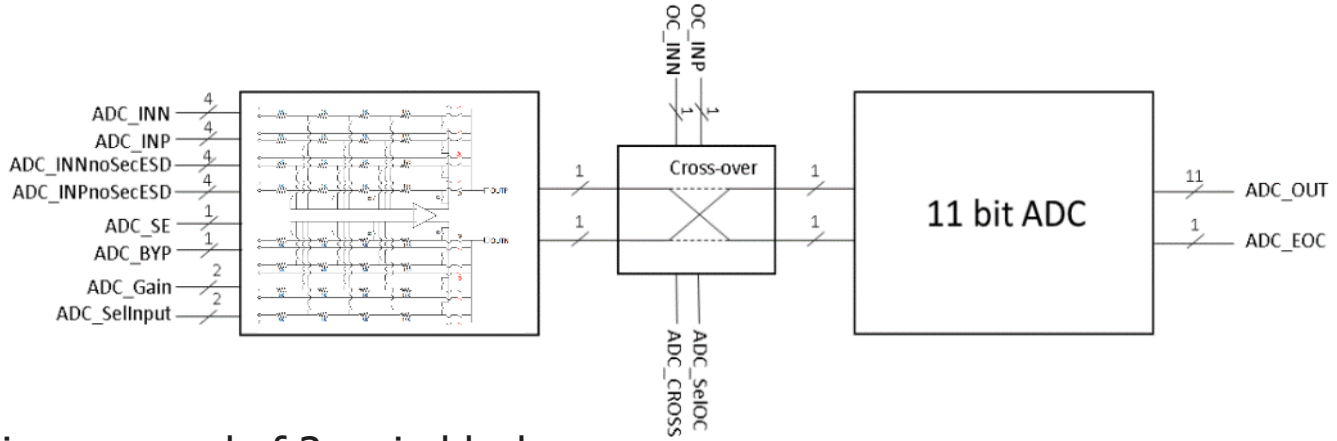
## Key features – Integrated Analogue features

- RadHard 11 bits 300KS/s SAR ADC with Pre-amplifier
- RadHard 12 bit 3.75MS/s DAC
- RadHard Crystal Oscillator
- RadHard Power On Reset
- RadHard 1.8V and 3.3V voltage monitors
- RadHard GPIO with local Power on Control
- RadHard LVDS transceivers with build-in reference
- RadHard voltage and current reference
- RadHard Low-drop regulators
- RadHard external voltage references
- RadHard high density RAM with EDAC protection
- RadHard PLL
- Temperature sensors and core voltage sense

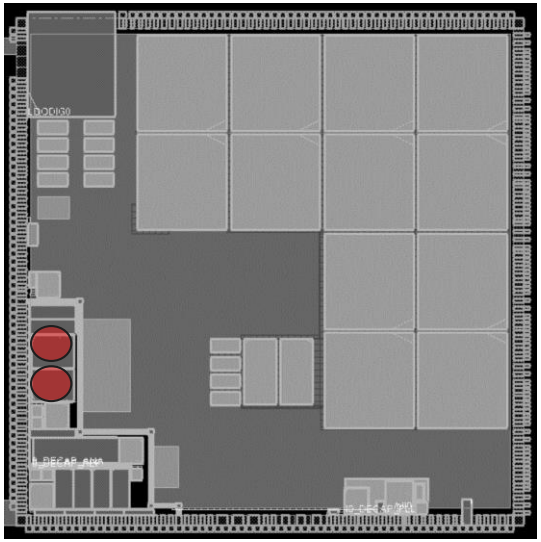


# GR716 – LEON3FT Microcontroller

## Analogue architecture – Dual 11 bits 300KS/s SAR ADC with Pre-amplifier



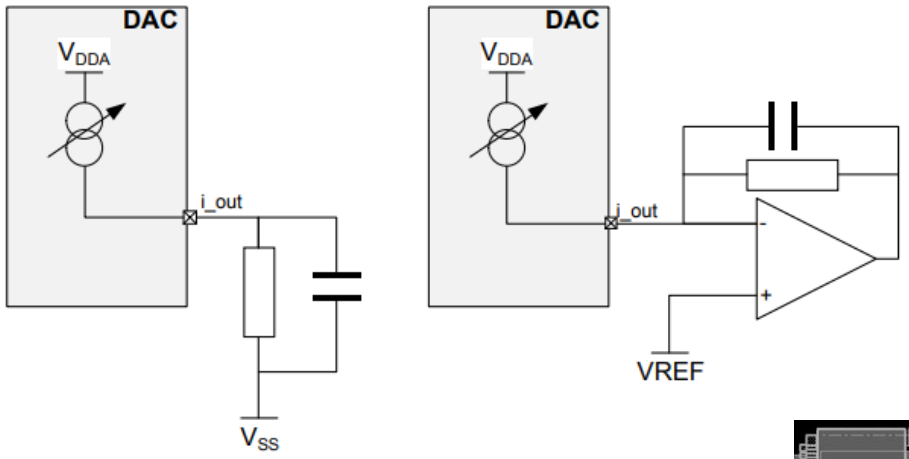

- The ADC is composed of 3 main blocks:
  - An analog mux 8:2 combined with an auto zeroed-amplifier (0dB, 6dB and 12dB)
  - Cross-over block for swapping inputs
  - A differential and single ended SAR ADC (11b, 300kS/s) with internal voltage reference.
- Design is hardened against SET and SEU:
  - Control logic use exclusively rad-hard Flip-Flops (HIT)
  - Data out bits are hardened via Muller-C filter.
  - Clock paths hardened via IMEC DARE180 clock driver cells
  - Analog filters to prevent SET events on configuration inputs



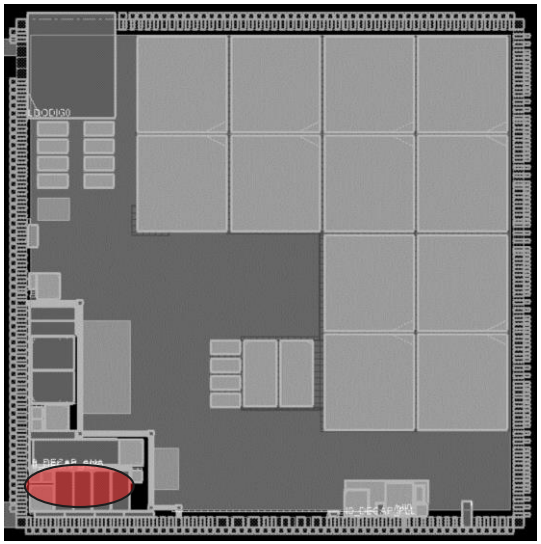
*Dual RadHard 11 bits SAR ADC Integration*

# GR716 – LEON3FT Microcontroller

## Analogue architecture – 12 bit 3.75MS/s RadHardDAC




- Four individual current steering DAC with dedicated supply
- Two operation modes available:
  - High accuracy with maximum data rate of 58.6kS/s (DEM mode)
  - Fast mode with maximum sampling data rate of 3.75Ms/s (Non-DEM mode)
- The fast mode and the high precision mode need to use virtual ground

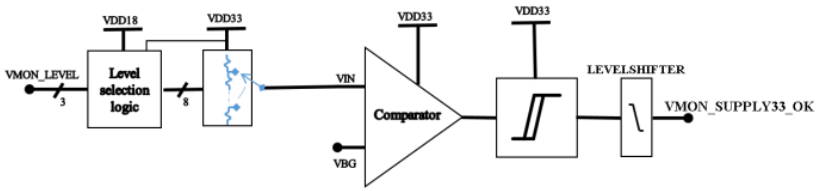


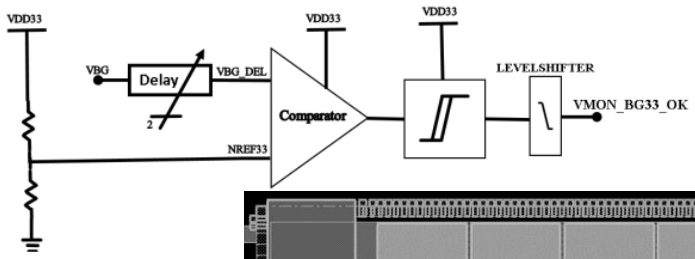
*RadHard DAC Integration*

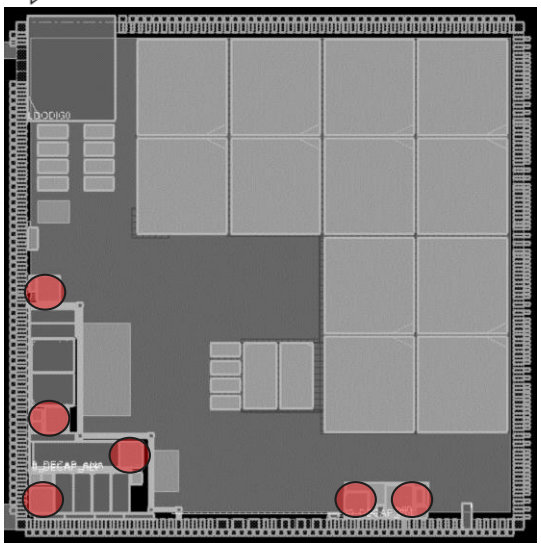
# GR716 – LEON3FT Microcontroller

## Analogue architecture – Voltage monitor

- 1.8V and the 3.3V supplies monitored with internal filtering (~20µs).
- 3 bits threshold configuration:
  - From 1.6V till 1.8V.
  - From 2.9V till 3.24V.
- Voltage sense is made in package to detect failure as early as possible.
- Voltage monitor implemented for external and internal voltage supplies.
  - 6 separate voltage monitor for monitoring each separate voltage domain
- Voltage monitor can disable output drivers to avoid malfunction or driver contamination.



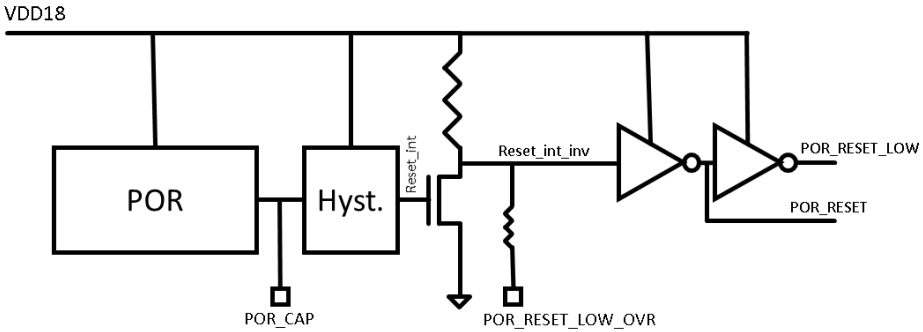



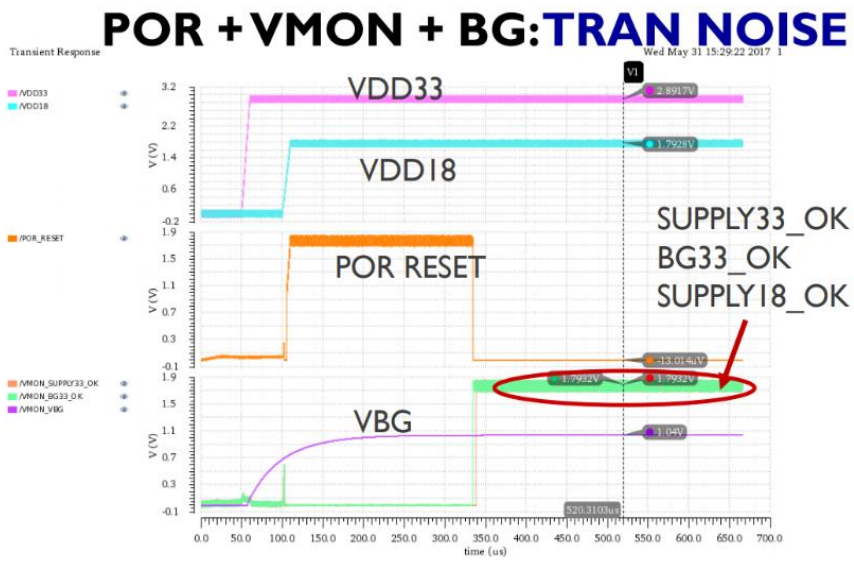
*Voltage Monitor Integration*

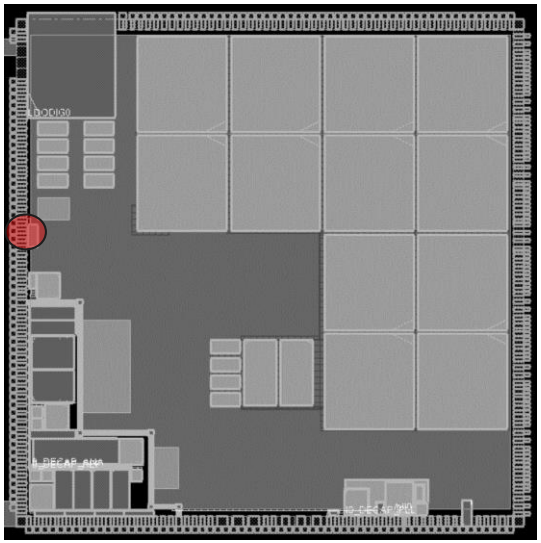
# GR716 – LEON3FT Microcontroller

## Analogue architecture – Power On Reset

- Programable reset pulse duration:
  - 235 µs without external capacitor
  - 150 ms with external capacitor of 220nF
- SET free at 60 MeV*cm$^2$/mg
- External reset is glitch free and can be used as system reset



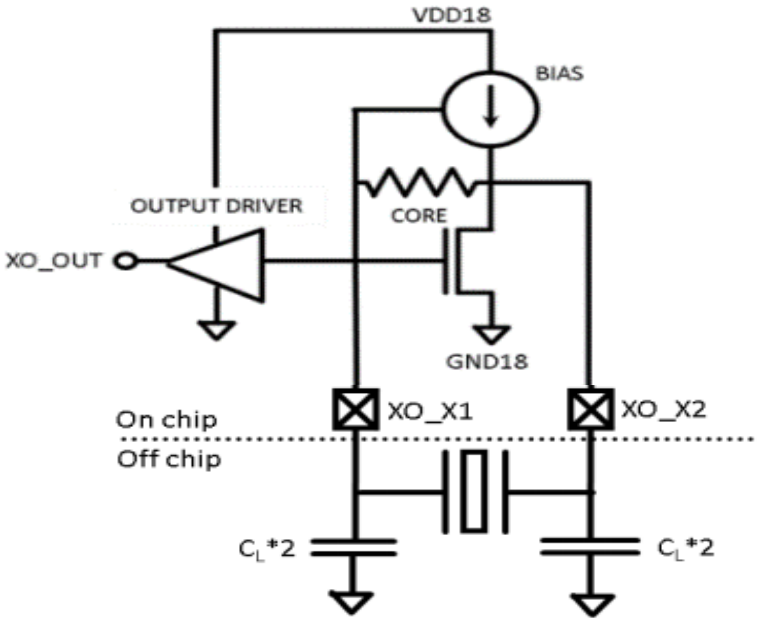



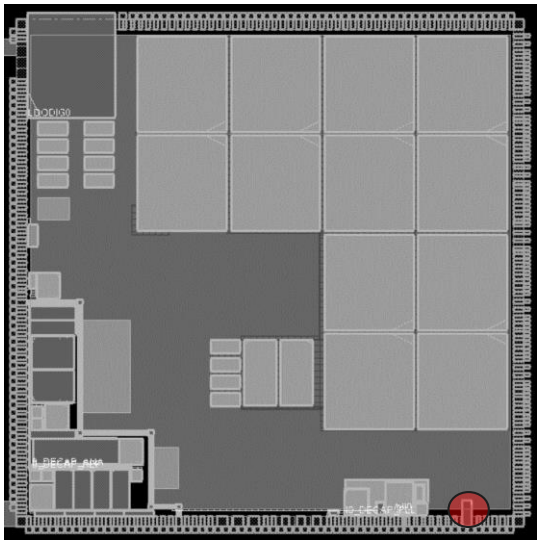
*Power On Reset Integration*

# GR716 – LEON3FT Microcontroller

## Analogue architecture – Crystal Oscillator



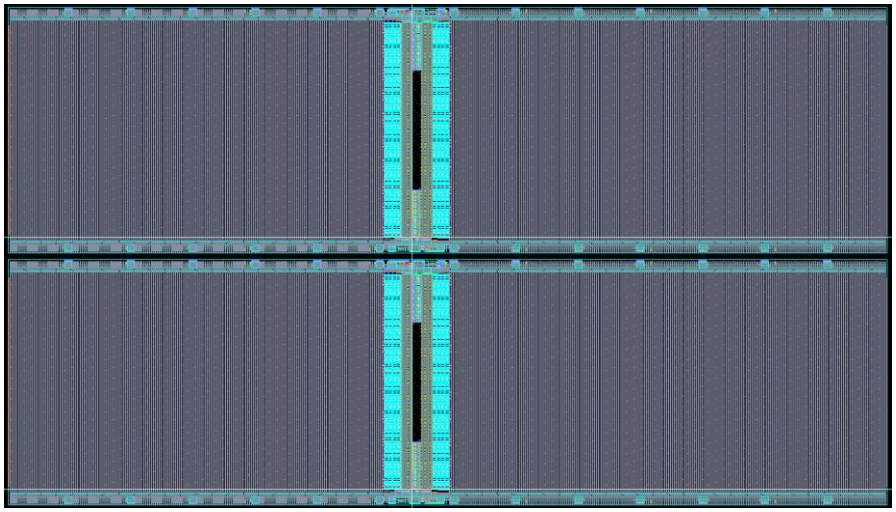

- External clock generated from the crystal is available for the system.
- Support Space Grade and commercial crystals in the range of 5MHz to 25MHz.
- SET hardened:
  - no false edge on the clock can happen
  - maximum period error due to SET of 1.1ns and 3.8ns when respectively running at 25 MHz and 5 MHz (60MeV*cm2/mg)



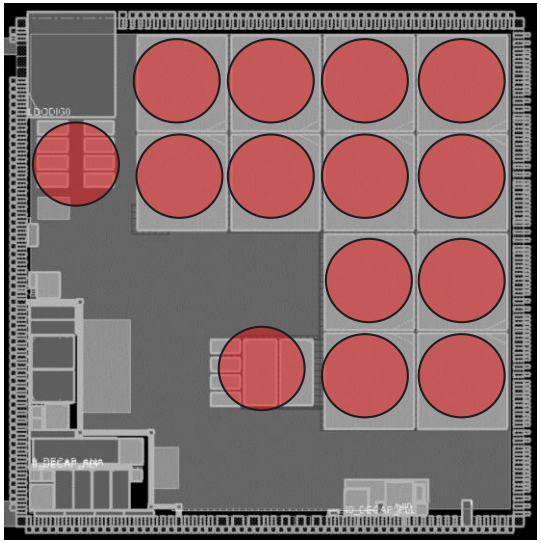
*Crystal Oscillator Integration*

# GR716 – LEON3FT Microcontroller

## Analogue architecture – High density SRAM



- 192KiB on-chip tightly coupled data and instruction RAM for the processor
- Integrated error detection and correction. One error can be corrected and two errors can be detected, which is performed by using a (32, 7) BCH code
- Programmable Scrubber
- Build-in memory test for device boot report and production test using March C- test algorithm

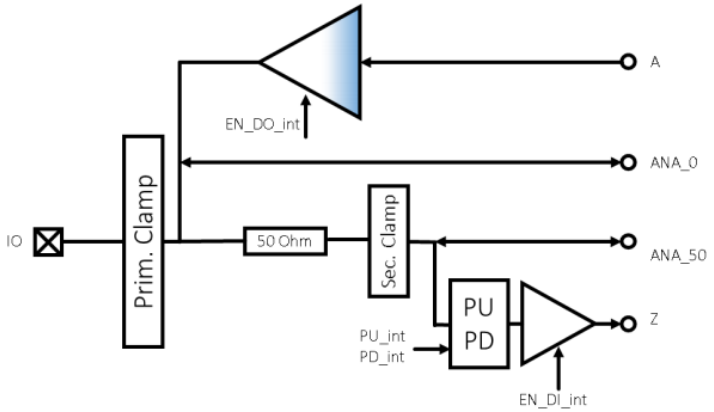


*RadHard High density SRAM Integration*

# GR716 – LEON3FT Microcontroller

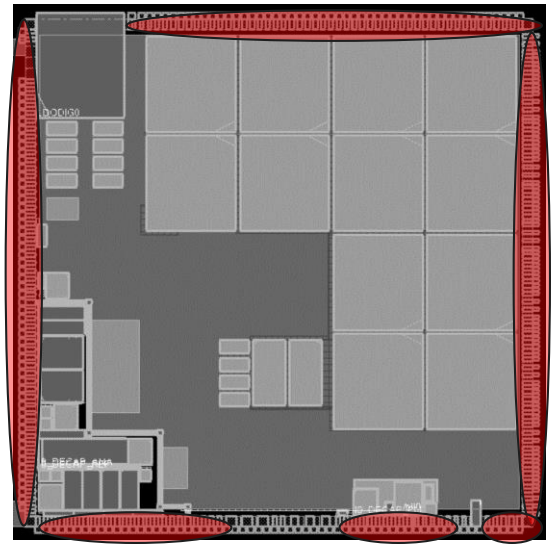
## Analogue architecture – GPIO with local Power On Control

- Can be used as:
  - Digital input (Schmitt trigger) with programmable pull up/down
  - Digital output (4mA)
  - Analog input (serial impedance of 50 Ohms)
  - Analog output




- When configured in digital input/output mode the GPIO is completely SET free and use only ELT layout for the NMOS transistors to make it insensitive to radiation effect.

- Its local Power On Control force the IO output in high impedance mode as long as the core voltage is not turned-on. Practically this high impedance mode will be maintained after the ramp-up of the core voltage thanks to the Power On reset



*Mixed Analog and Digital GPIO Integration*

# GR716 – LEON3FT Microcontroller

## Analogue architecture – LVDS transceivers with build-in reference

**Typical applications**

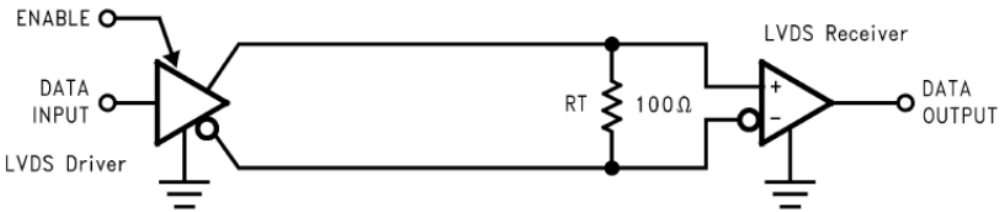
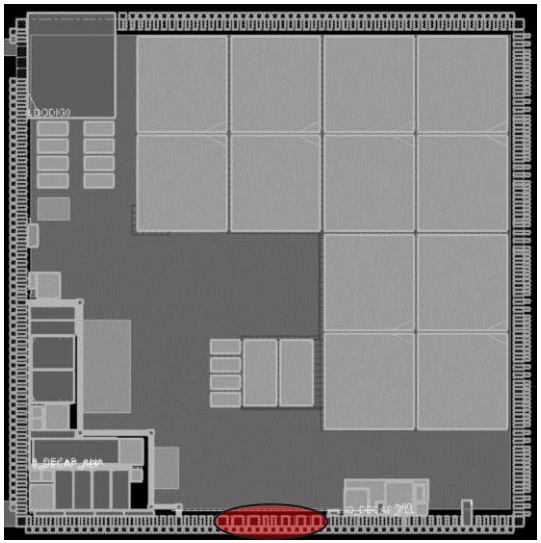



**Figure Point-to-point Application**

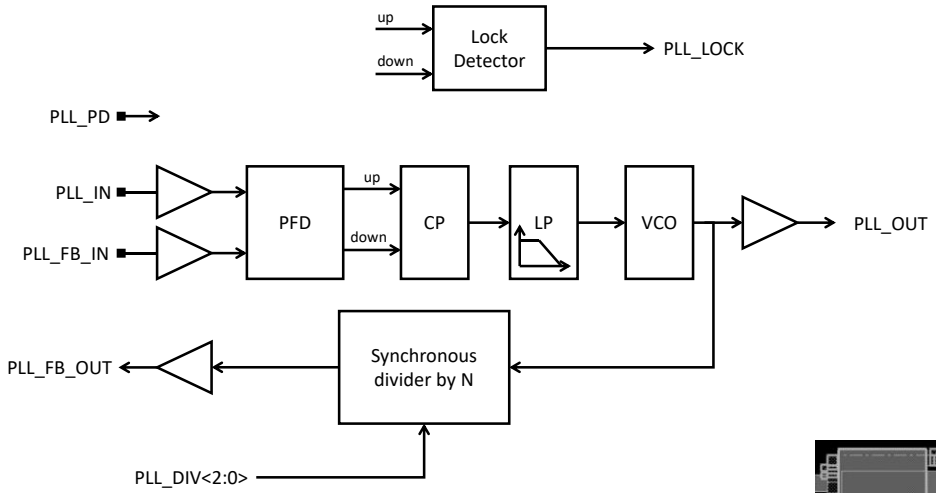
- LVDS driver, transmitter and bias reference are radiation hardened and compliant with the TIA/EIA-644-A standard
- Precision on-board reference for integration and performance
- On-chip LVDS transceivers for SpaceWire and SPI for Space and dedicated pins for external SPI boot ROM are available and can optionally be used



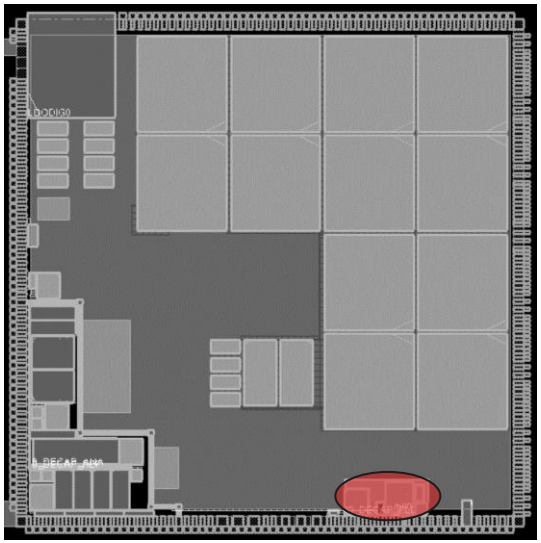
*LVDS with precision reference Integration*

# GR716 – LEON3FT Microcontroller

## Analogue architecture – 400 MHz PLL




- Programable clock divider: 8, 16, 20, 32, 40 and 80
- Low jitter: 600fs in typical condition
- VCO hardened against SET (60MeV*cm$^2$/mg):
  - No false edge
  - Max phase error of 160ps at 400MHz
  - Max phase error of 600ps at 280MHz

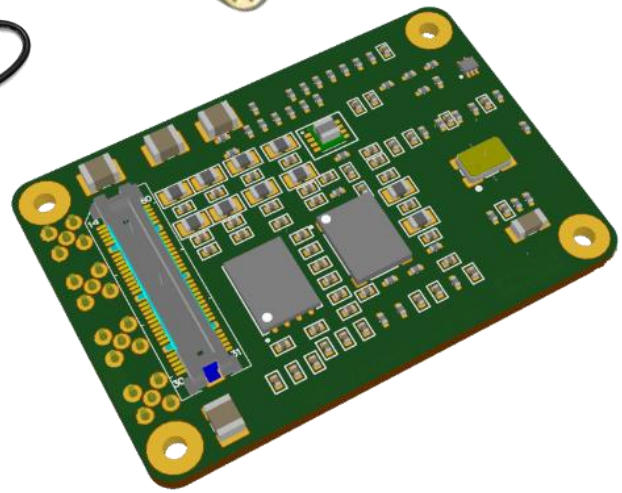


*Input frequency extended range PLL*

# GR716 evaluation board

## GR716-MINI – GR716 Software evaluation board

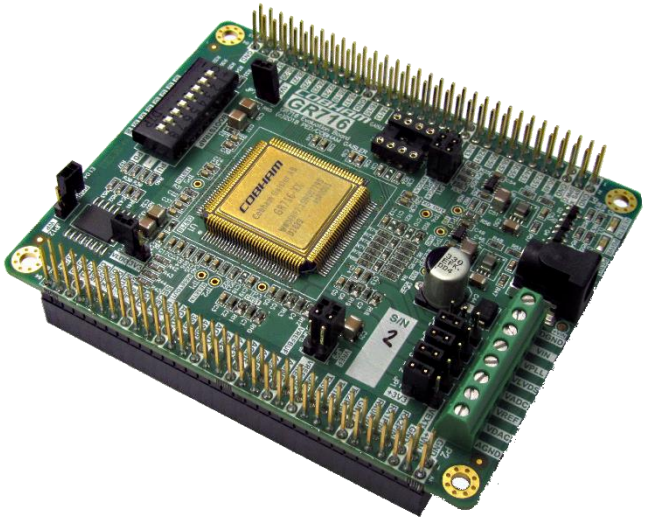
- Baseline design for evaluation board:
  - GR716 microcontroller
  - SPI Flash PROM (32 MiB)
  - SRAM (2 MiB)
  - FTDI USB interface
    - GRMON3 debug I/F via Debug UART
    - 2x UART interfaces, 1x I2C interface
    - control of reset, configuration pins etc.
    - power supply
  - 4x MMCX (micro-miniature coaxial):
    - 2x ADC, 2x DAC
  - miniature 80 pin mezzanine connector:
    - addition ADC, DAC, LVDS, GPIO, etc.
  - Oscillator
  - LED for power indication etc.
  - 50mm x 35mm (37.5% of a credit card)
- Shipped with:
  - free GRMON3 GUI (limited) download
  - free compilers, OS, tools downloads
  - USB cable (debug and power)

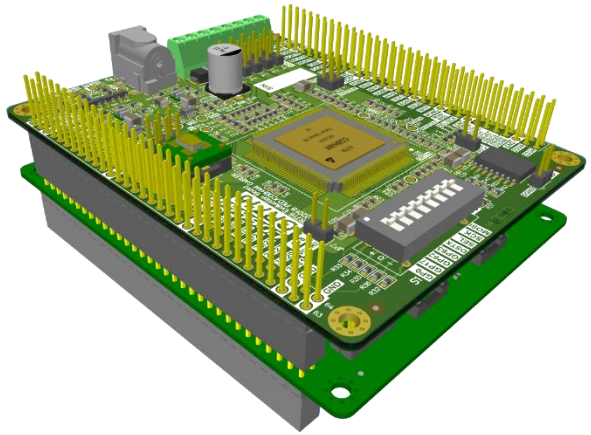
# GR716 development board

## GR716-BOARD – GR716 Hardware engineering board

- Baseline design for development board:
  - GR716 microcontroller
  - SPI Flash PROM (32 MiB)
  - PCI104 style stackable headers (2 x 64 pin) for interfaces
    - measurement points on all GPIO/interface signals for monitoring/debug
    - interface to user defined modules (memory, digital I/F, analog I/F)
    - interface to cPCI mother board in 6U rack or box format
  - Debug UART /IF
  - LVDS in/out (3+3 pairs) for 1x SpW or x SPI for Space
  - GPIO (64 pins)
    - digital I/O
    - external memory I/F
    - 6x UART
    - Mil-Std-1553B, PacketWire, CAN, I2C, 3x SPI, 16x PWM out
    - 8x analog in, 4x analog out, external ADC/ADC interface
    - 1x SpaceWire, 1x TDP
  - Socketed oscillator (5–25MHz)
  - DIP-switch for bootstrap options
  - Powered from external supply (range 5V to 12V)
  - Single supply operation or individual supplies
  - 80mm x 100mm format



*GR716 Standalone Board*

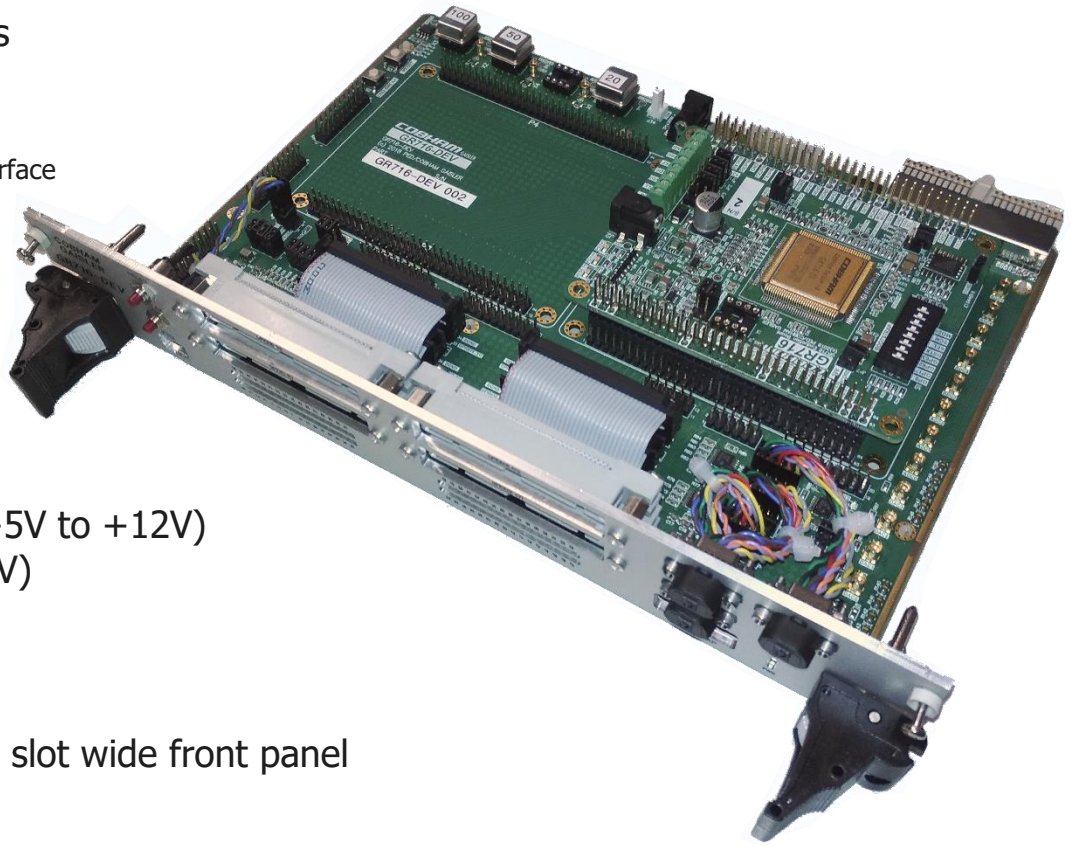


*Stack multiple boards via PC104 connector*

# GR716 development board

## GR-CPCI-GR716-DEV – GR716 interface development board

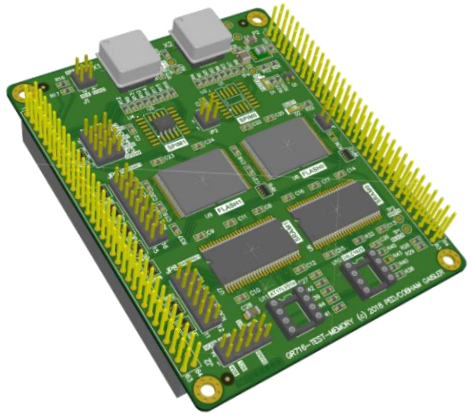
- Baseline design for interface application board:
  - GR716-BOARD engineering board in dedicated slot
    - Multiple slots for possibility to attach multiple GR716 engineering boards
  - Expansion slot for memory or user defined functions (e.g. SRAM, ADC/DAC)
  - Socketed oscillators for system, SpaceWire, Mil-Std-1553B and PWM clocks
  - Configuration of front panel functions
  - Front panel interfaces
    - MDM9S for fixed SpW (LVDS) interface
    - MDM9S for configurable SpW/SPI4S (LVDS) interface
    - GPIO (64 pins on standard 0.1" connectors)
    - LED indicators (64) for GPIO pins
    - DIP switch for bootstrap options
    - Reset and DSU Break push-button switches
    - LEDs for power and reset status
    - FTDI USB interface
      - GRMON3 debug I/F via Debug UART
      - 2x UART interfaces, 1x I2C interface
  - Power from external supply (range +5V to +12V) or via cPCI backplane connector (+5V)
  - Expansion through accessory boards
    - 6x UARTs using GR-CPCI-6U-UART
    - CAN, Mil-Std-1553B, SPI using GR-CPCI-GR740
  - 233mm x 160mm, 6U cPCI format, 2 slot wide front panel



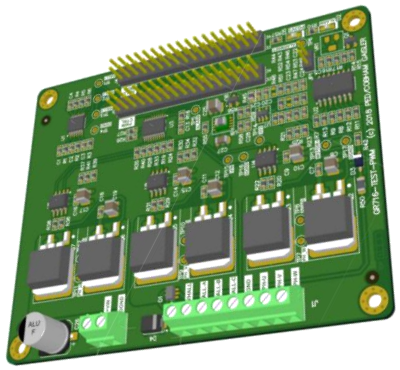
# GR716 development board

## GR716-BOARD – Extension-, Test- and Configuration- boards

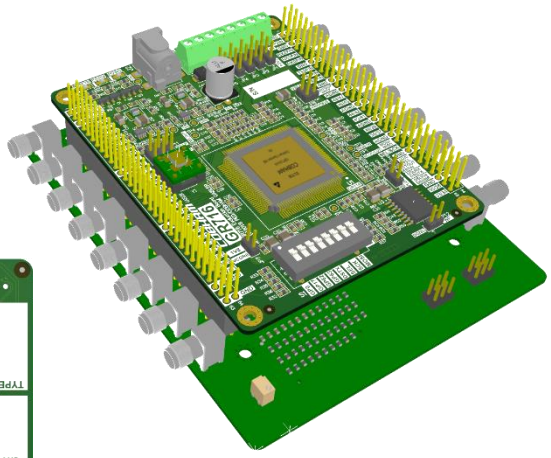
- GR716 Memory Board:
  - Memory extension board
    - Support dual memory redundancy protection
  - PCI104 style stackable headers (2 x 64 pin)
  - 80mm x 100mm format
- GR716 Configuration Board
  - Configuration board
- GR716 Analog Test Board
  - Interface board for analog interfaces
  - PCI104 style stackable headers (2 x 64 pin)
  - 80mm x 100mm format
- GR716 BLDC Test board
  - 3-phase inverter with PWM interface for interfacing BLDC/Stepper Motor



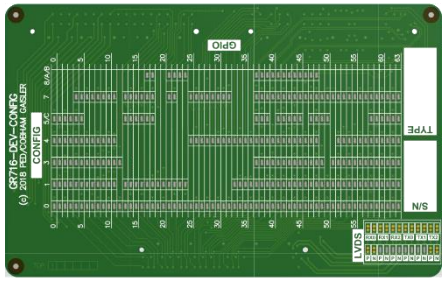
*Memory Board*



*BLDC Test Board*



*Analog Test Board*

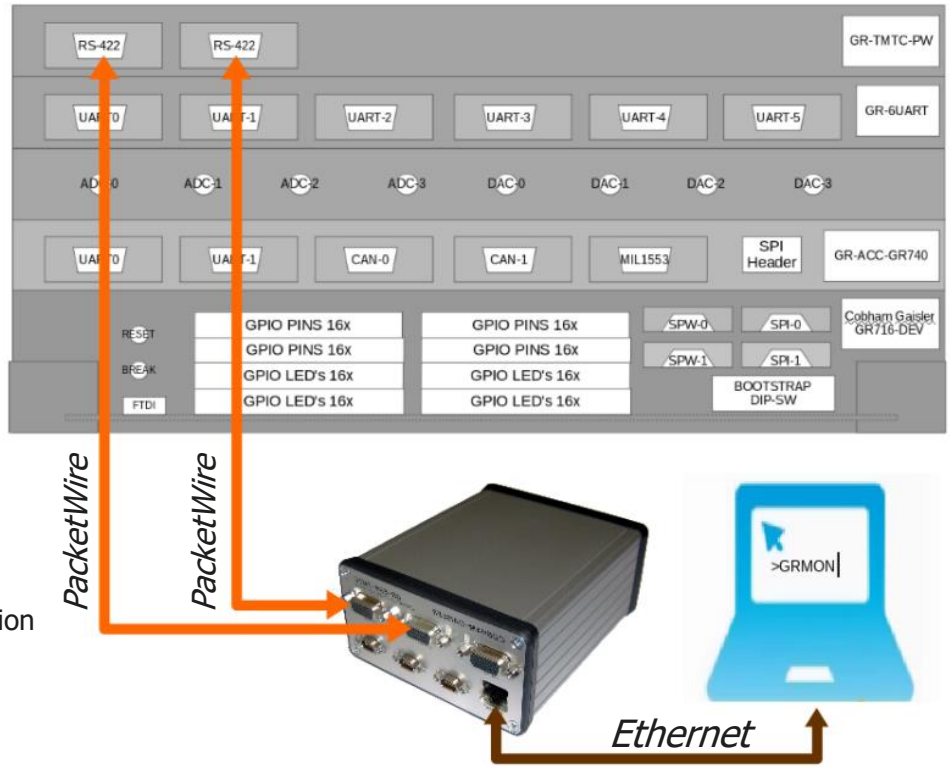


*Configuration Board*

# GR716 development board

## Build your application

- Build your application via available interface boards
- Compatible boards possible to direct connect and use from Cobham Gaisler:
  - GR-ACC-6U-6UART
    - Extend number of UARTs in the system
  - GR-ACC-GR740
    - Dual CAN 2.0 transceiver, Dual MIL-1553B interface and SPI interface
  - GR-CPCI-CAN
    - Dual CAN 2.0 transceiver
  - GR-TMTC-PW (6U)
    - RX/TX PacketWire interface
  - SPI4S Test Board
    - Reference board for SPI for Space demonstration
  - Analog Front end
    - Easy connection of external ADC and DAC



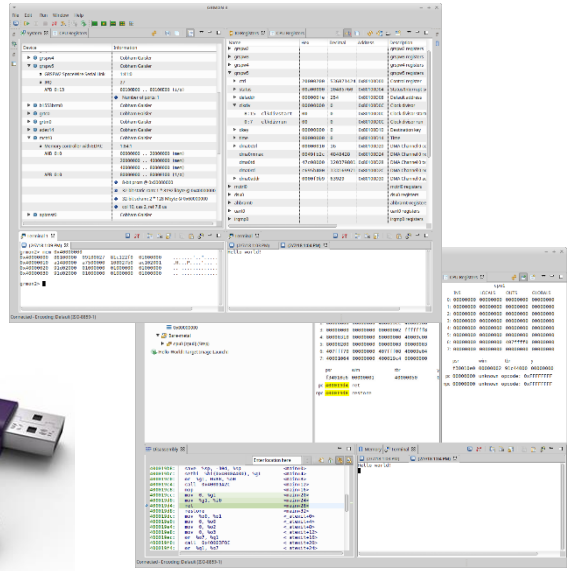

- Use Configuration Board to avoid driver contamination
  - Possible to fit mezzanine board on the development board to avoid erroneous configuration of the IOs

# GR716 Development Platform

## GR716 software development environment

- BCC2 Development Environment
  - GCC 7.2.0 or CLANG 8.0.0
    - Performance increase with '*link time optimization*'
    - CLANG 8.0.0 to be released in 2018
  - GR716 BSP Support build in

- GRMON3 Debugger
  - Graphical User Interface (GUI) based on Eclipse TCF (Target Communication Framework) platform (used by Wind River and Xilinx)
  - GRMON displays HW/SW state in GUI without GDB in-between
  - ***Low cost limited GR716 versions***



- TSIM3 Software Simulator
  - GR716 BETA release in 2019 Q1

# GR716 Development Platform

## BCC2 for GR716

- Bare metal toolchain for LEON processors
  - C/C++ cross compilers, both GCC and LLVM/Clang
  - C/C++ standard libraries
  - Open source with permissive licenses
- Support for GR716
  - Basic support for the GR716 architecture
    - Memory map, interrupts, capabilities
    - Linker scripts
    - ROM resident images
  - Support for GR716 features
    - REX
    - Single Vector Traps
    - Can generate chip specific instructions
  - Device drivers for GR716 I/O cores
  - Flat mode, staying in one register window
    - Can reduce jitter
    - Can be used with register window partitioning
  - Optional C runtime with even smaller footprint: -qnano

# GR716 Development Platform

## BCC2 for GR716 - Adjusting to different profiles

| Property | Performance | Footprint | IRQ Response time |
|---|---|---|---|
| Soft mul/div | - | - | + |
| Soft float | - | - | + |
| Flat mode | * | - | + |
| Single Vector Trapping | - | + | - |
| Smaller runtime: -qnano | | + | ~ |
| More register windows | + | ~ | ~ |
| IRQ jitter reduction | - | ~ | - |
| REX | | + | |
| Optimize for size | - | + | ~ |

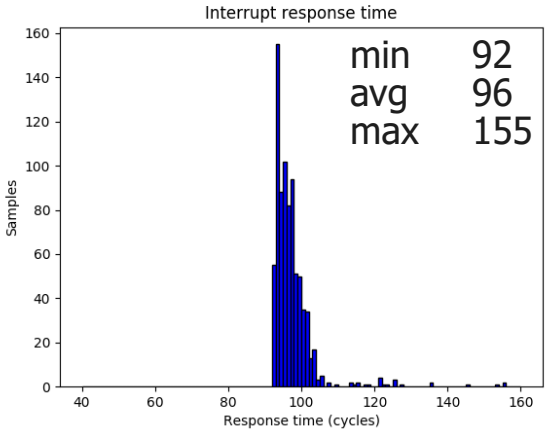
Effects in general for the given metric:

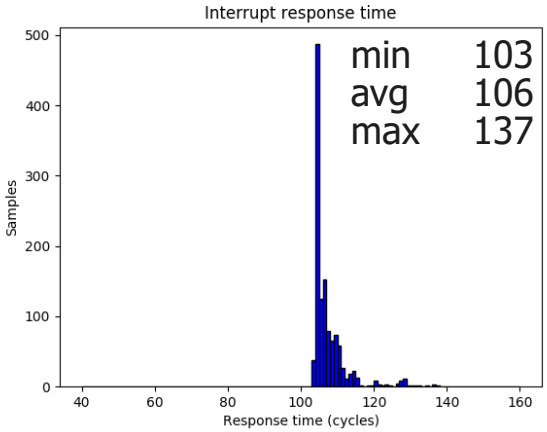
| | | | |
|---|---|---|---|
| + | better | * | Varies |
| - | worse | | |
| ~ | marginal | | |

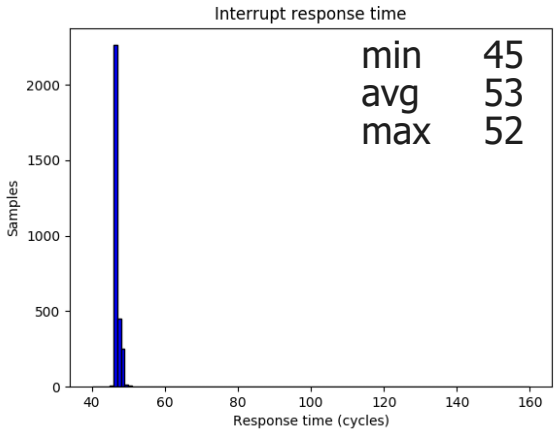
# GR716 Development Platform

## BCC2 for GR716 - Adjusting to different profiles - Whetstone

| Performance mode | Footprint mode | Response time mode |
|---|---|---|
| 8 s execution time | 12 s execution time | 250 s execution time |
| 131 KiB footprint | 77 KiB footprint | 155 KiB footprint |




- This is taking most parameters <u>to the extreme end</u>
  - No REX here in footprint mode
- Effects are application specific
- BCC2 Options can be mixed and matched to suit the application
- Footprints is excluding needed stack space

** Whetstone Profile Performance: GR716 run-time profiles Application note is available upon request via support@gaisler.com*

# GR716 Development Platform

## TSIM for GR716 development

- Already used in daily internal testing
  - All boot possibilities
  - Load and run from local memory or external SRAM
  - Many of the new GR716 features in place
- TSIM-GR716 BETA release in 2019 Q1
  - In between TSIM2 and TSIM3
    - GR716 does not need all new features of TSIM3
  - User model API available
    - Not in final TSIM3 form


```
$ /tsim-leon3 -gr716 ./coremark.elf
tsim> run

TSIM/LEON3 SPARC simulator, version tsim3-dev-ad71c1e55f1cee67 (internal version)

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For latest updates, go to http://www.gaisler.com/
Comments or bug-reports to support@gaisler.com

Number of CPUs: 1
register windows: 31
system frequency: 50.000 MHz
using 64-bit time
Allocated 128 KiB LOCAL ICACHE RAM memory at 0x31000000
Allocated 64 KiB LOCAL DCACHE RAM memory at 0x30000000
allocated 4096 KiB SRAM memory, in 1 bank
allocated 2048 KiB ROM memory
allocated 16384 KiB SPIM ROM memory
allocated 16384 KiB SPIM ROM memory
section: .text, addr: 0x31000000, size 78032 bytes
section: .rodata, addr: 0x30000000, size 3088 bytes
section: .data, addr: 0x30000c10, size 1584 bytes
read 475 symbols
tsim> run
  starting at 0x31000000
2K performance run parameters for coremark.
CoreMark Size    : 666
Total ticks      : 18529354
Total time (secs): 18.529354
Iterations/Sec   : 107.936844
Iterations       : 2000
Compiler version : GCC7.2.0
Compiler flags   : -O2 -qnano -qsvt -qbsp=gr716 -mcpu=leon3
Memory location  : Static
seedcrc          : 0xe9f5
[0]crclist       : 0xe714
[0]crcmatrix     : 0x1fd7
[0]crcstate      : 0x8e3a
[0]crcfinal      : 0x4983
Correct operation validated. See readme.txt for run and reporting rules.
CoreMark 1.0 : 107.936844 / GCC7.2.0 -O3 -qnano -qsvt -flto -qbsp=gr716 -mcpu=leon3  / S

 Program exited normally.

tsim>
```

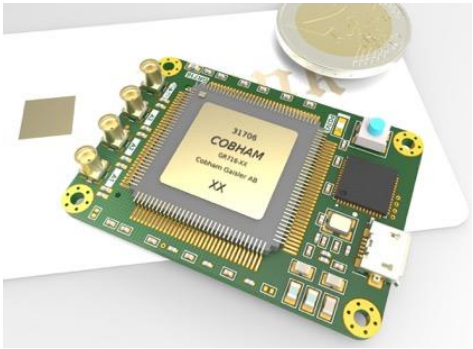
# GR716 updated schedule

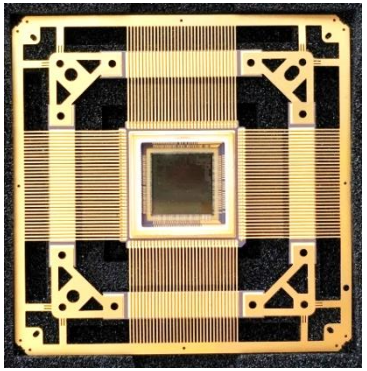
As of 12 December 2018

| GR716 | Status | Milestone | Comments |
|---|---|---|---|
| Advanced Data Sheet & User's Manual | *done* | *Q2 2017* | *Available* |
| PDR | *done* | *Q2 2017* | *review passed in June* |
| CDR | *done* | *Q2 2018* | *review passed in May* |
| Prototype level tape-out | *done* | *Q2 2018* | *taped-out in May* |
| Prototype level assembly | done | Q3 2018 | completed in September |
| Prototype level functional test | done | Q4 2018 | completed in December |
| Prototype level performance test | | Q1 2019 | Ongoing |
| Prototype level part delivery | | Q1 2019 | Ongoing |
| Evaluation board delivery | | Q1 2019 | Ongoing |

- GR716 microcontroller is funded by ESA up to prototype design and validation, output from ESA activity will be prototype parts and evaluation boards.
- Additional funding available from ESA for the evaluation with respect to analogue performance and radiation.
- Qualification decision pending successful evaluation.

- Price list to be established and orders for prototypes to be accepted in Q1 2019.



# GR716 Highlights

## Highlights

- Successfully developed and integrated several new digital and RadHard analogue IP cores in first tape-out
- Sucessfully taped-out and demonstrated working prototypes
- Sucessfully manufactured system development kit
- Improved LEON-SPARC tool-chain and debugger released
- Improved the LEON3FT code density and real-time characteristics
  - LEONREX
  - Fast context switching
- Improved work flow:
  - ESD strategy for mixed signal ASIC
  - Voltage drop strategy
  - Low power strategy
  - SET strategy
  - Digital on top integration and verification

# GR716 Highlights

## Preliminary performance results

- All ADC and DAC channels are working
  - ADC linearity less than 1 LSB
  - DAC linearity less than 5 LSB *
- BandGap voltage reference is measured to 1.003V and external voltage reference to 2.40V.
- Single voltage supply and separate voltage supply has been validated
- Possible to trim the internal core voltage from software in range 1.780V to 1.925V.
- Crystal Oscillator, PLL and frequency generation logic has been validated
  - Sleep and low-power mode
- Possibility to trim and set BrownOut detection levels has been validated
- Power on reset functionality has been validated
- Glitch free GPIOs during power-up or power-down **

** Limitation in test setup. (1 LSB = 1 uA)*

*** Test system not able to detect any glitches lower than 1uA.*

# GR716 Conclusion and Outlook



- Mixed signal microcontroller prototypes has been succesfully manufactured

- Microcontroller characteristics implemented
  - High level of integrated RadHard analogue functions
  - High level of integrated digital functions and communications interface
  - High level of configurability
  - Scalable  performance
  - Software debugger and toolchain with driver and device support

- Microcontroller suitable for variety of platforms and equipment

THANK YOU FOR LISTENING!

**Contact support@gaisler.com for more information**