Compact Reconfigurable Avionics – Reconfigurable Data Handling Core

CORA-RDHC

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2019 CAN IN SPACE WORKSHOP

Presentation overview

- Introduction to CORA
- Overview of the CORA-RDHC activity
- System design and COTS BB
- RDHC design
- RDHC hardware
- VHDL design
- Software
- Summary

00
Introduction to CORA

Introduction to CORA

Objectives

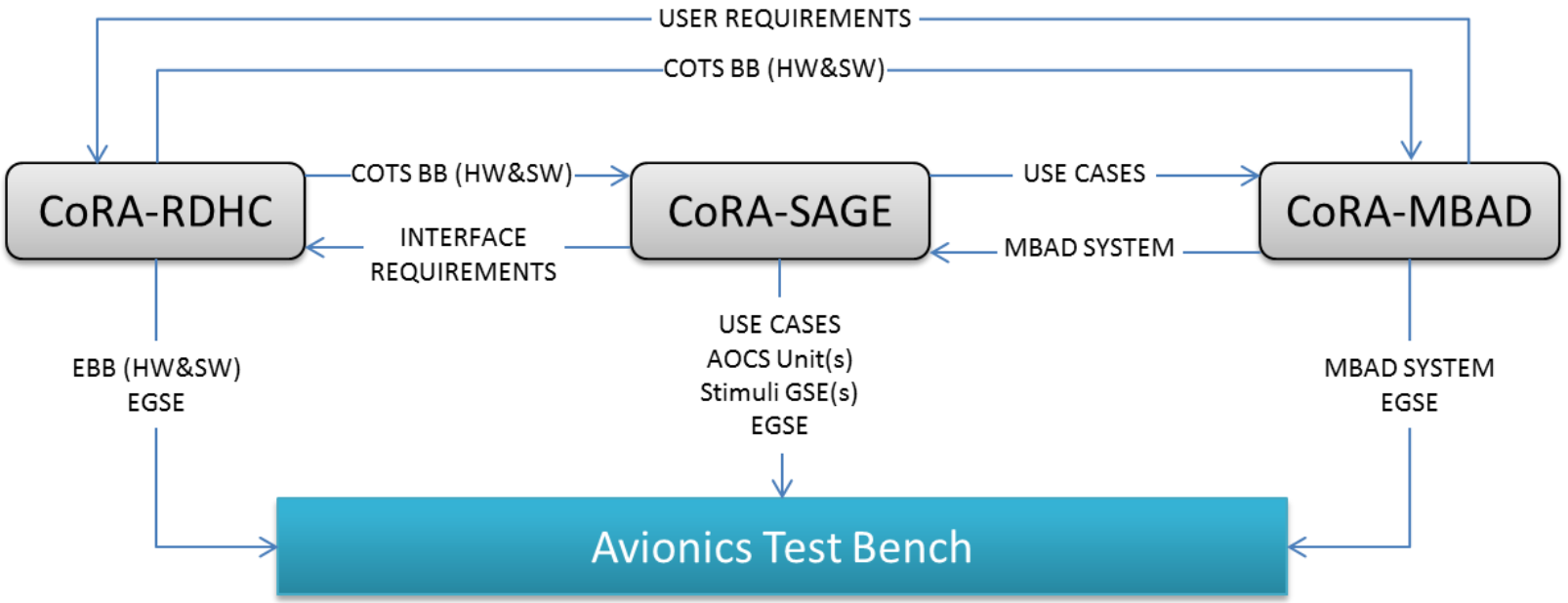
- To experiment the co-engineering process between three activities to prototype a compact reconfigurable avionics:
  - Supporting exploratory designs during early development phases
  - Allowing in-flight reconfigurations for the adaptation to different mission phases and modes
  - Offloading the processor thanks to on-board hardware support

Introduction to CORA

Organization

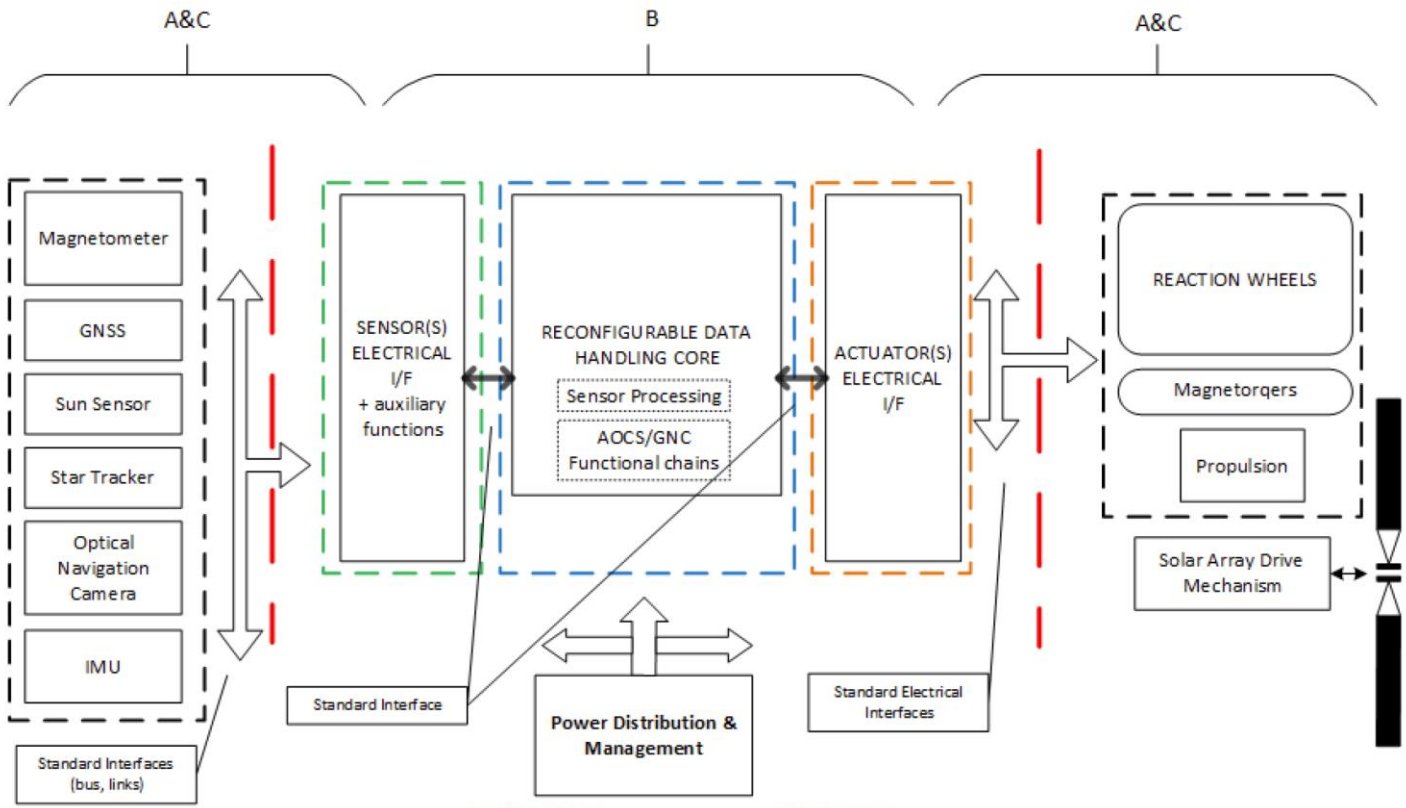
Three coordinated TRP activities with dependencies between them:

- Reconfigurable Data Handling Core (CoRA-RDHC)
- Model Based Avionics Design (CoRA-MBAD)
- Smart AOCS&GNC elements (CoRA-SAGE)



Introduction to CORA

Scope and distribution



Candidate sensors:

- FaintStar-based Star Tracker
- MEMS-based IMU
- Sun Sensor on a chip
  Navigation on a chip

Applications:

- LEO Earth Observation
- LEO Telecom
- Exploration
- In-orbit servicing

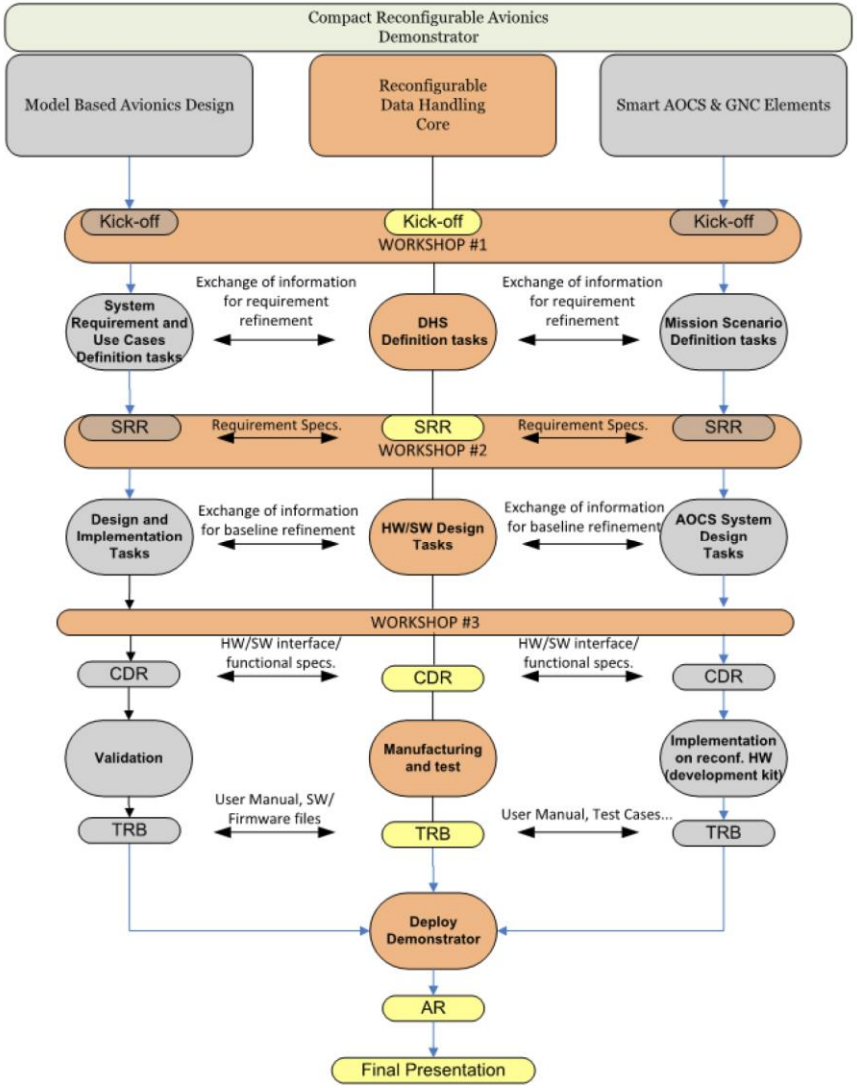
Concepts:

- SAVOIR-SAFI
- Spacewire AOCS prototyping
- Time and Space partitioning

A: scope of the SMART AOCS & GNC ELEMENTS ACTIVITY
B: scope of the RECONFIGURABLE DATA HANDLING CORE
C: scope of the MODEL BASED AVIONICS DEVELOPMENT

Introduction to CORA

Cross activity information flow

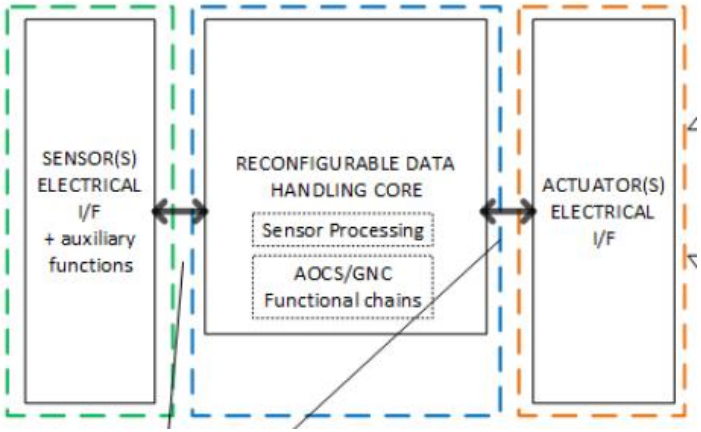


Overview of the CORA-RDHC activity

Objectives

Summary

- Development of an Elegant Bread Board
  - A compact reconfigurable datahandling core module
  - High performance microprocessor and high capacity reconfigurable FPGAs
  - Clear path to space qualification
  - Accompanied by I/O interface modules
- Delivery of a SW development platform
  - Bread Board based on COTS
  - Identify, procure and make available to the parallel activities by PDR
- Development of Board Support Package
  - FPGA communication and reconfiguration
  - Communication interfaces towards external sensors and actuators
- Development of Boot SW
- Installation of the compact reconfigurable avionics testbed at the ESTEC Avionics laboratory



Organization

- ESA
  - Technical Officer: Jørgen Ilstad, TEC-EDD –> EOP-PPE
- Cobham Gaisler AB, Sweden (prime)
  - Responsible for the development of hardware, VHDL design, boot software and drivers
- Thales Alenia Space France
  - Responsible for middleware software design
- Thales Alenia Space España S.A., Spain
  - Responsible for FPGA reconfiguration code
- Airbus Defence & Space, France
  - Contribution to the systems analysis and trade-off, requirements and system architecture
- External service providers
  - Responsible for breadboard development

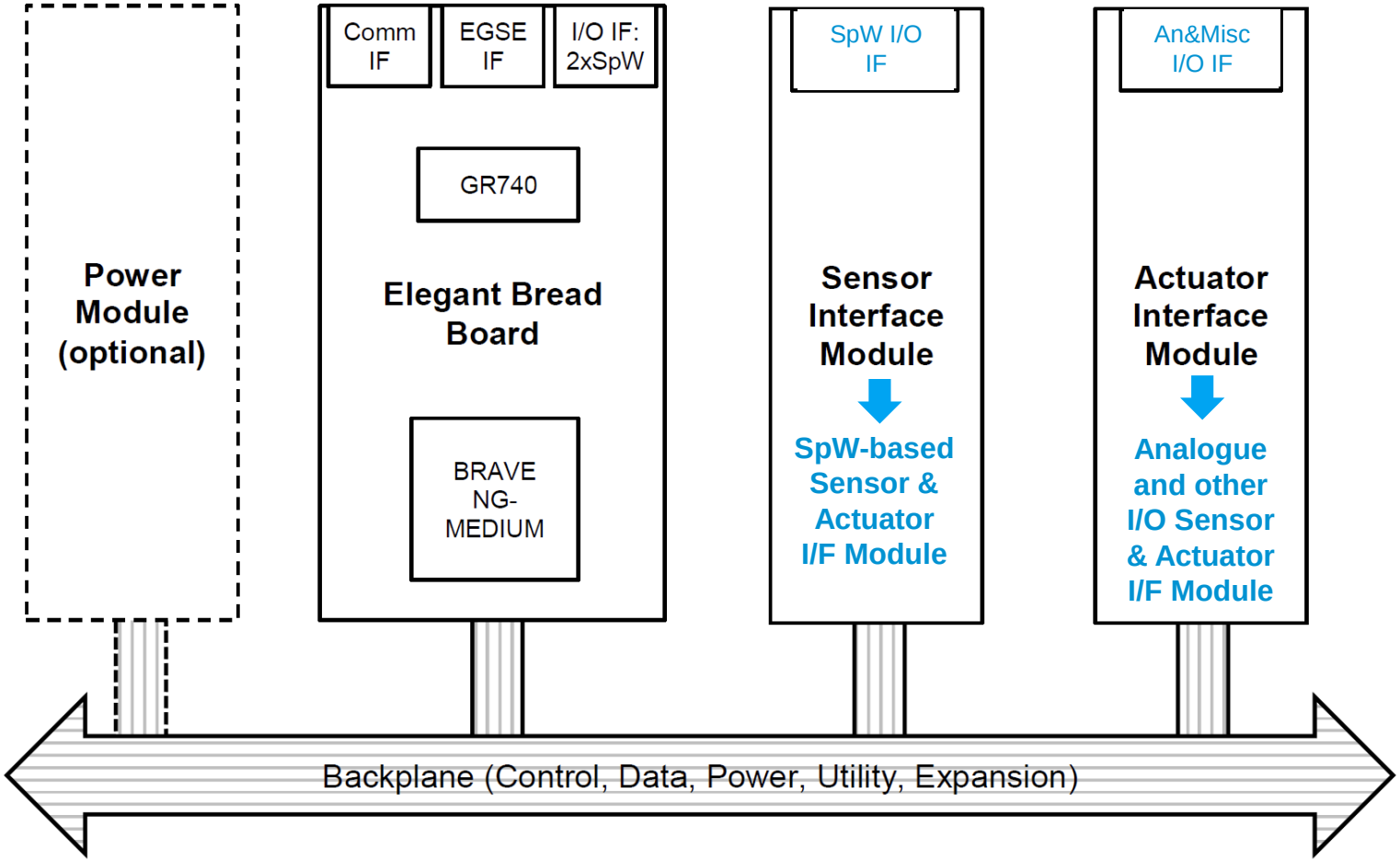
02
System design and COTS BB

Prerequisites

- GR740 Quad-Core LEON4 SPARC V8 Processor
  - Controller and high-performance processing
- FPGA BRAVE NG-Medium
  - European, existing, SpW-reconfigurable
- Common form factor
  - EBB and I/O modules
- I/O interfaces to be consolidated with the CORA-SAGE activity
- SW platform to be consolidated with the CORA-MBAD activity

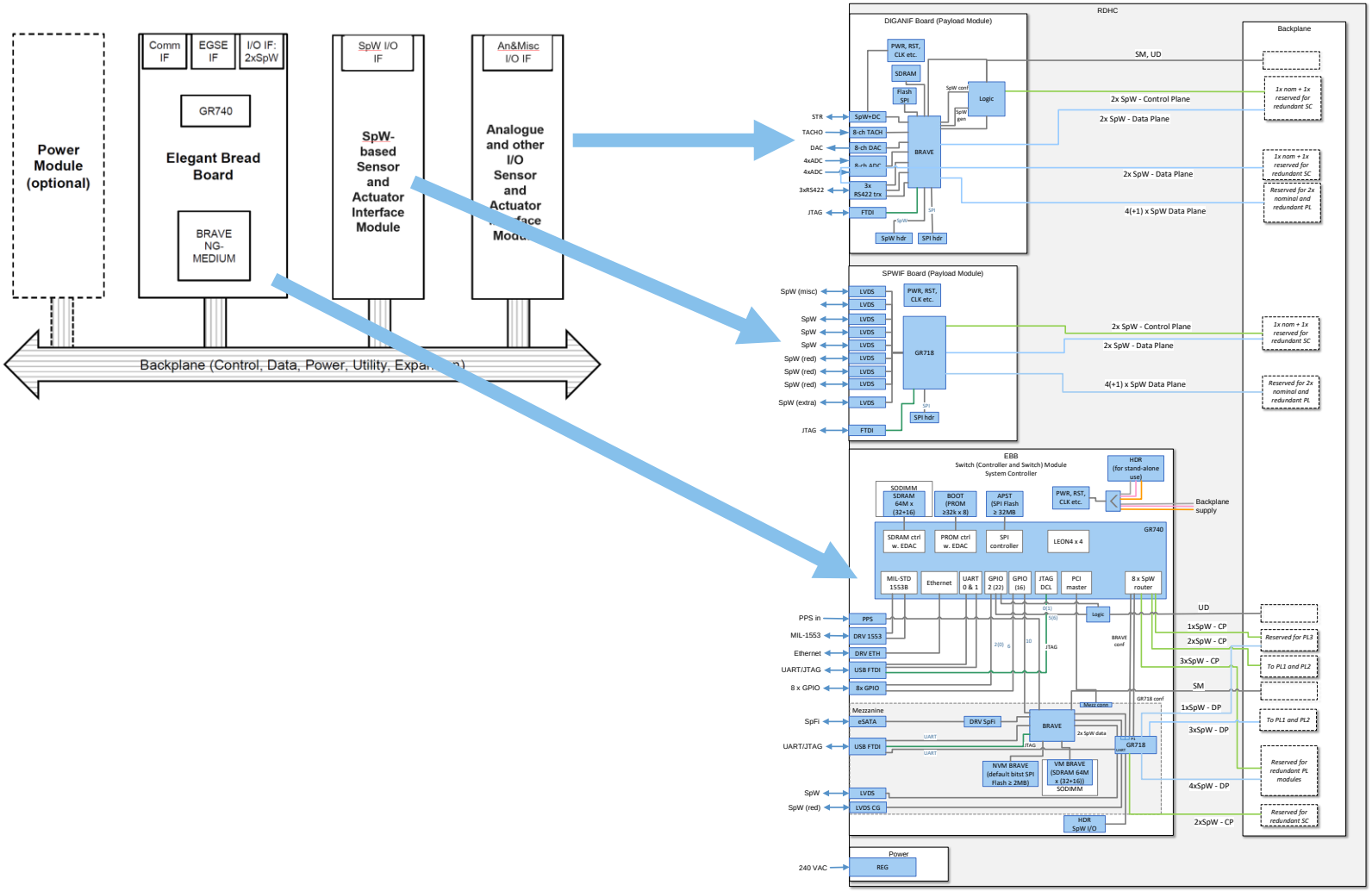
Concept

After CORA interface consolidation



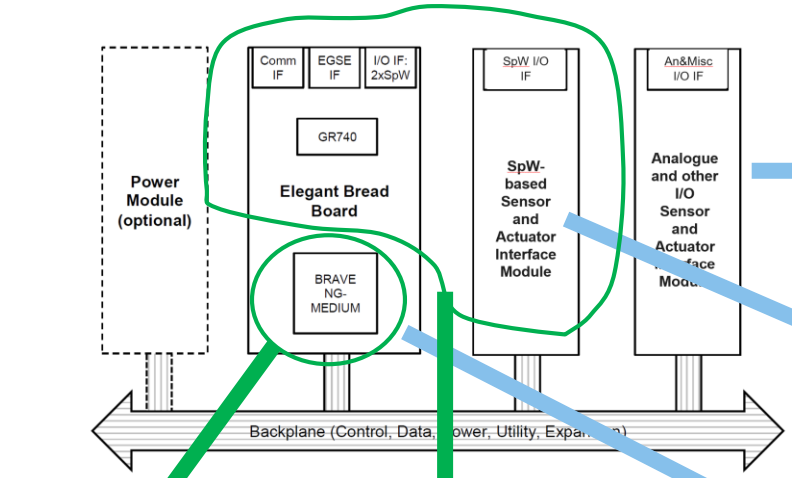
System design

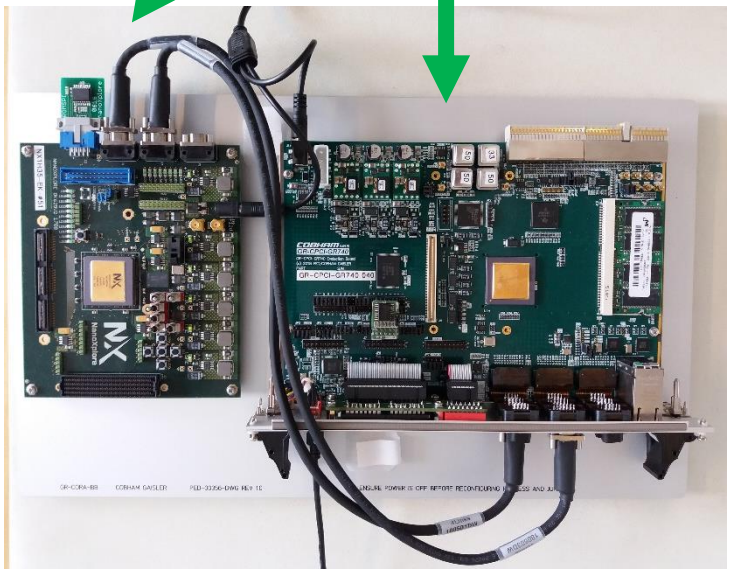
For COTS BB and final RDHC

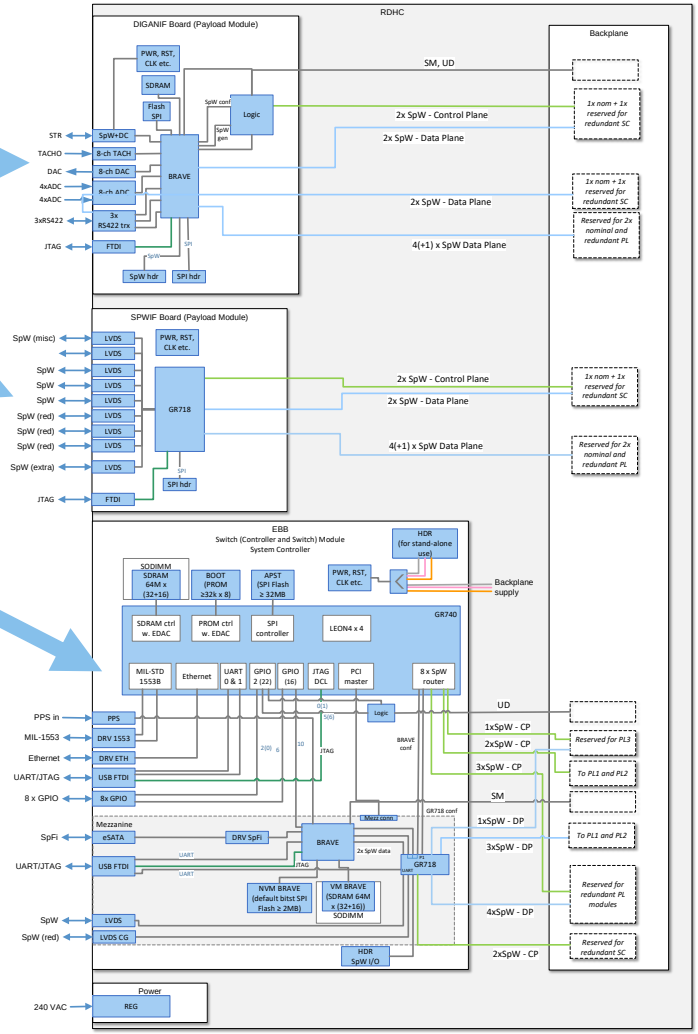


System design

For COTS BB – GR-CPCI-GR740 and NX1H35S-EK

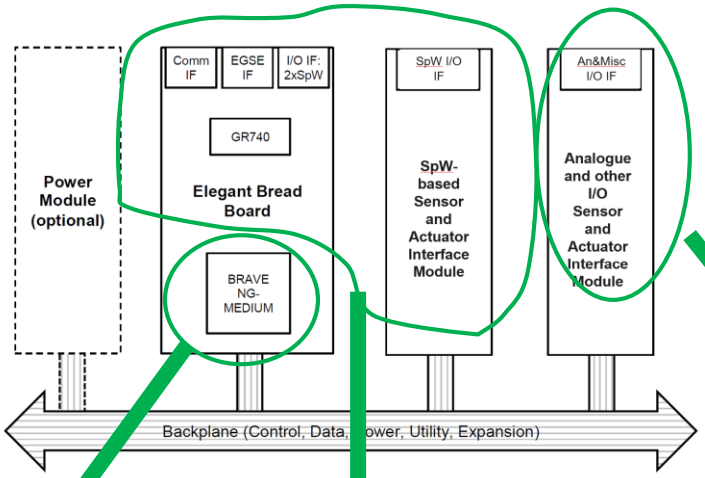




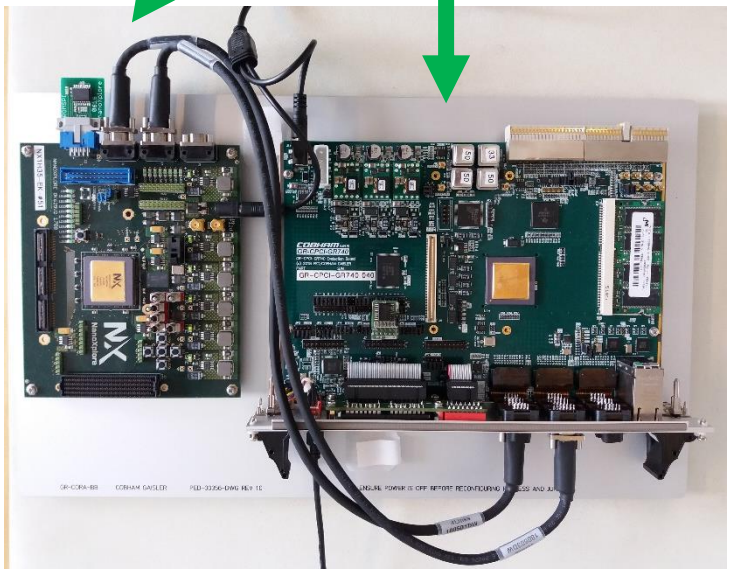


System design

For COTS BB – with DIGANIF Light



- Enables testing of Analogue and other I/O Interfaces for SAGE
- Developed prior to final RDHC
- Mezzanine for BRAVE Evaluation Kit

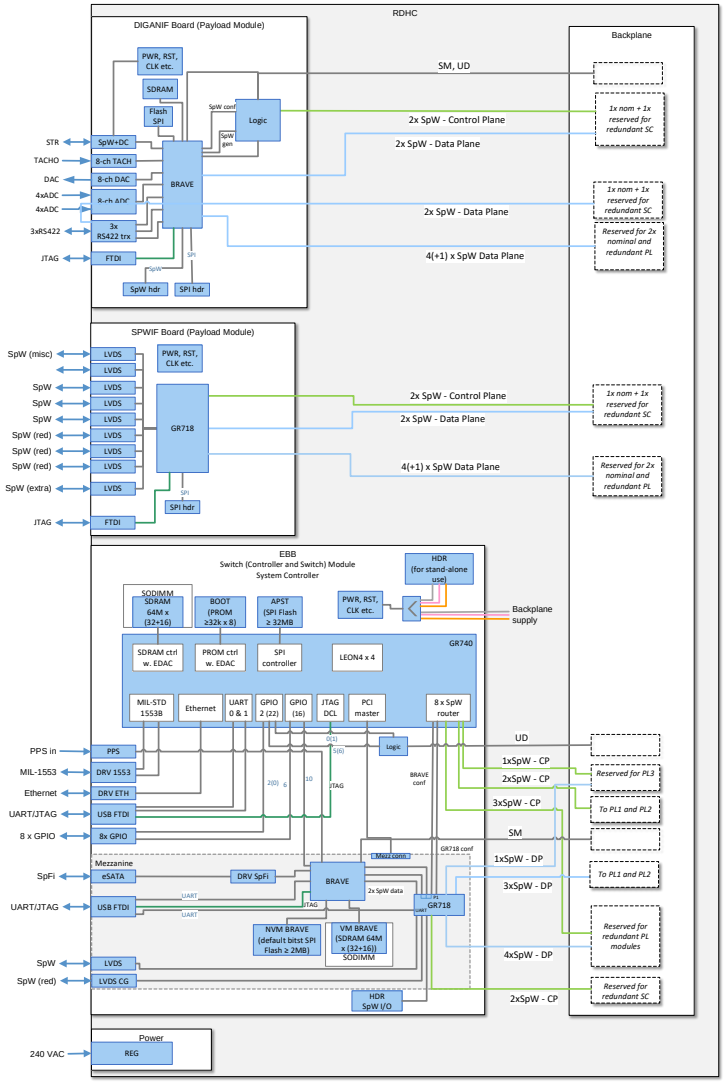


03
RDHC design

RDHC design

Major design iterations

- Form factor
  - OpenVPX, VITA 65 (3U, 6U)
  - SpaceVPX, VITA 78.0 (3U, 6U)
  - SpaceVPXLite, VITA 78.1 (3U)
  - Others
- I/O interfaces
  - Specifications
  - Adaptations to SAGE activity
- Redundancy concepts
  - Backplane profile
  - Board designs
- Reconfiguration options
  - On-board and between boards
- Design support for future
  - Flight parts
  - Backplane profiles



RDHC design

Major design decisions

- Form factor
  - VPX 6U selected
    - Front-panel interfaces dimensions
      - Driven by large connectors used in space applications
      - Lots of I/O distributed externally to the unit, is generally required for most applications
    - The need for power condition circuitry for many power supply rails coupled with lack of small footprint space qualified components
    - Additional PCB real-estate to achieve fault tolerant designs
    - Thermal design constraints drive module size to be become large
    - Thus 3U module size is inadequate to meet the above mentioned design drivers

RDHC design

Form factor

- OpenVPX 6U selected
  - COTS backplanes availability
- Backplane profile 11.2.5
  - Centralized Data Plane
  - Similar SpaceVPX Backplane Profiles
- EBB
  - For Switch Slots
- I/O Modules
  - For Payload Slots

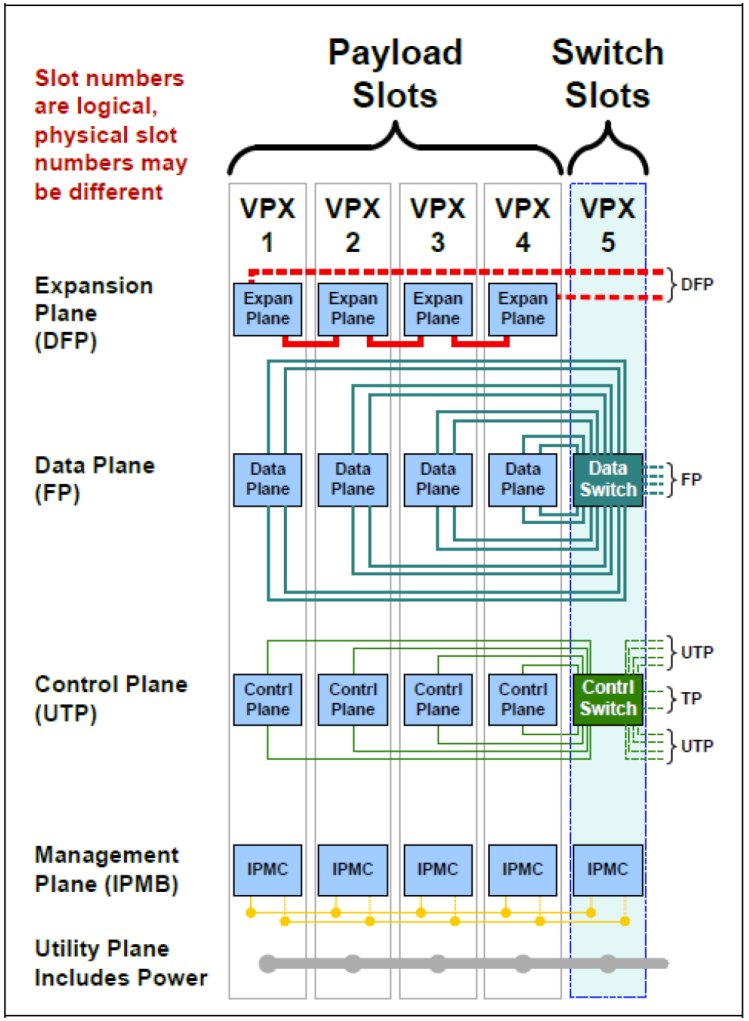


Figure 11.2.5-1 Topology of BKP6-CEN05-11.2.5-n

RDHC design

Form factor – forward compatibility

- SpaceVPX Backplane Profile 11.2.5
- EBB
  - Controller & Switch Slot
  - Factory-configuration needed
- I/O Modules
  - Payload Slots
  - Factory-configuration needed
- Designed to support redundant pairs
- No testing in the CORA activity
- Non-compliance: SpW used in Data Plane
  - Mainly driven by the lack of support for high speed serial links in the selected FPGA technology (BRAVE NG-Medium)
- Upgrade of the EBB FMC mezzanine will allow full compliance to the VITA dataplane in using high speed serial links e.g. SpaceFibre.

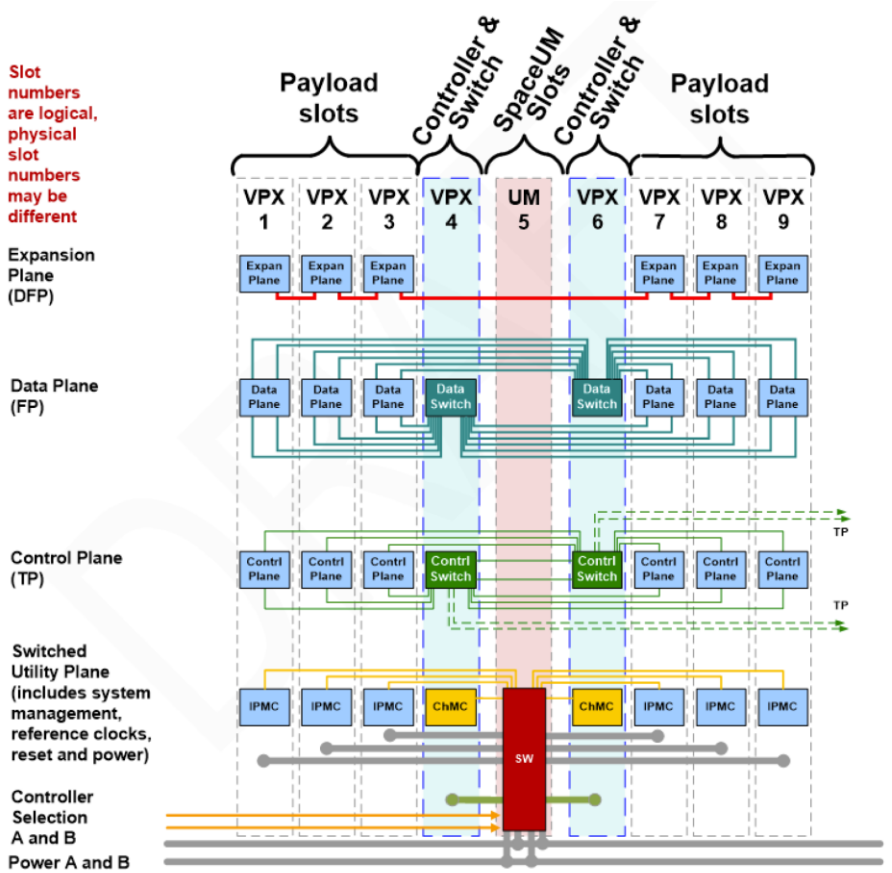
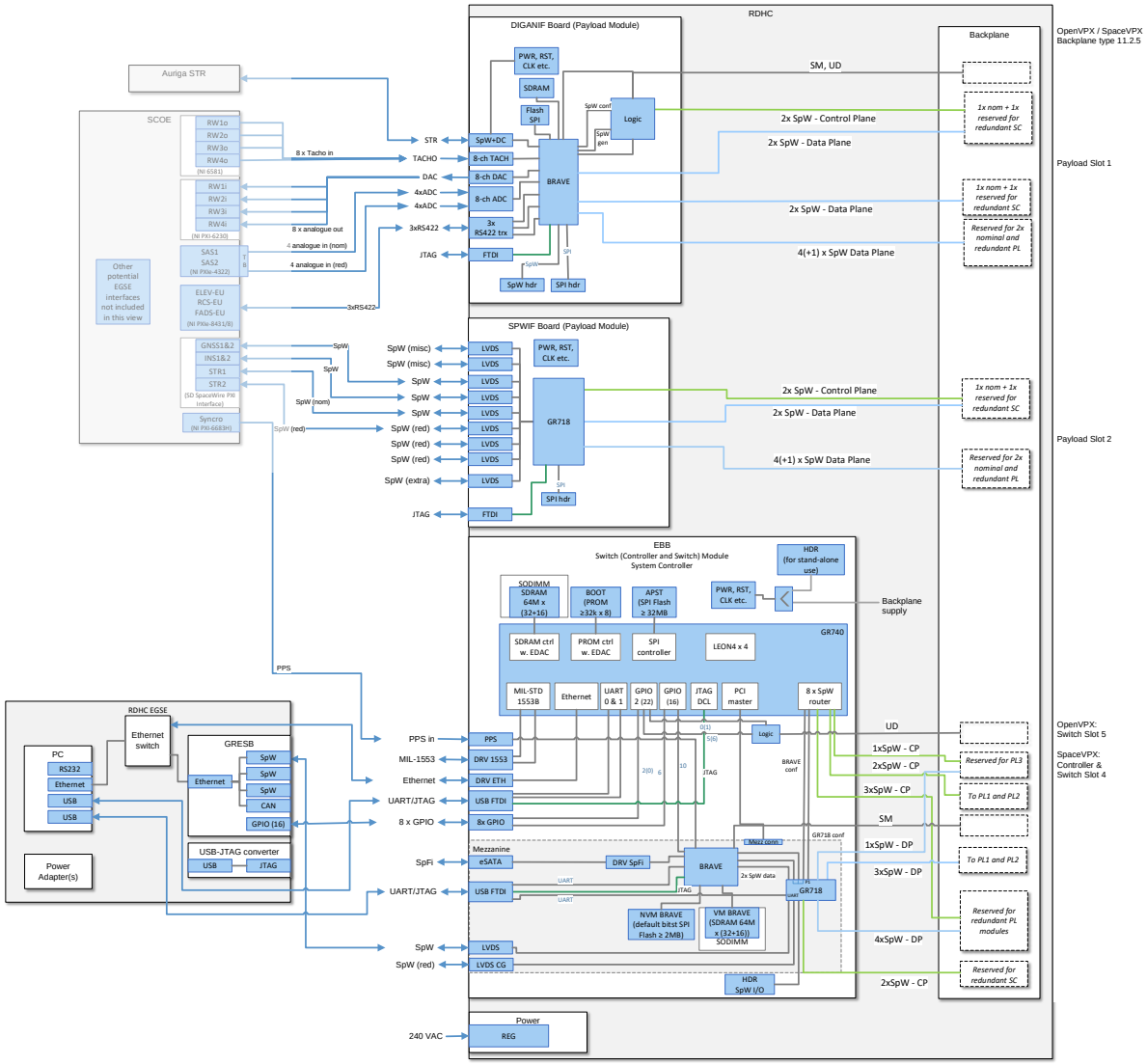


Figure 11-4: Topology of BKP-CEN10-11.2.5-n

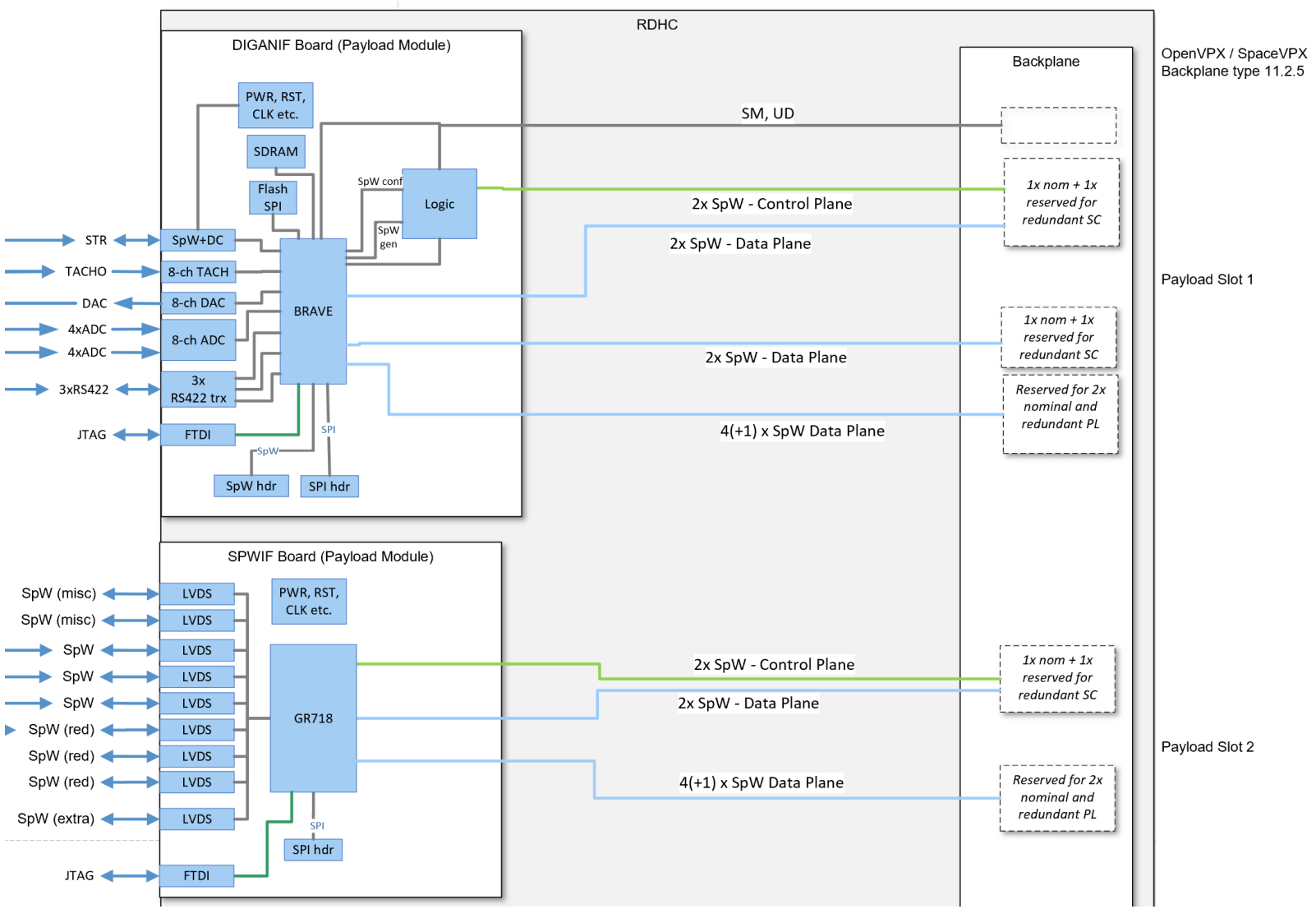
RDHC design

Complete CORA system



RDHC design

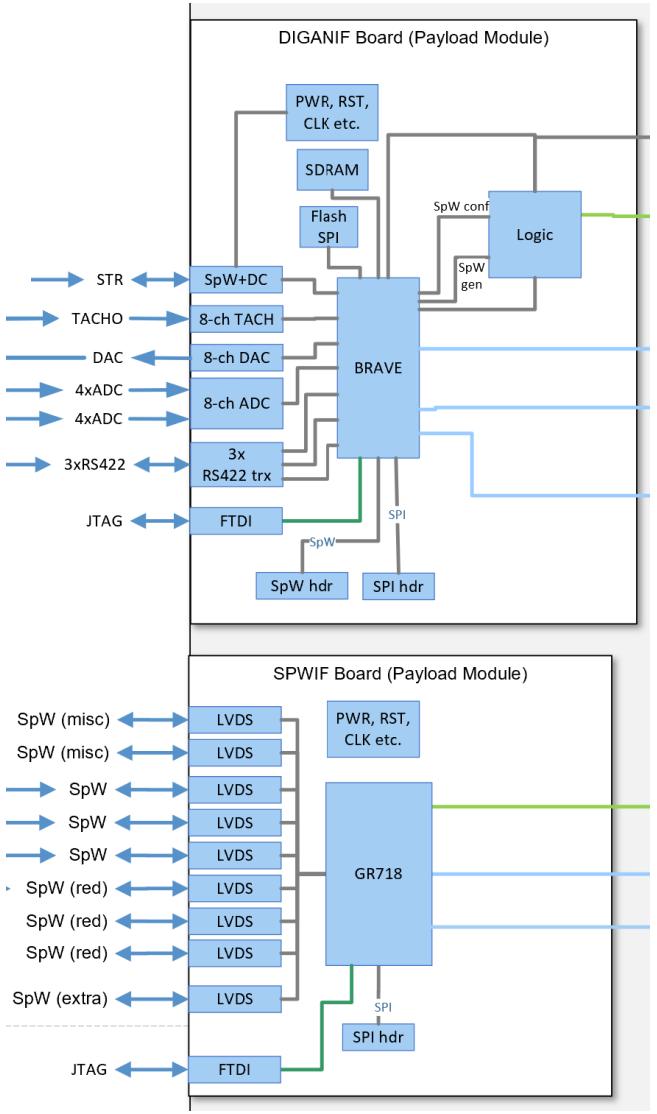
I/O Modules



RDHC design

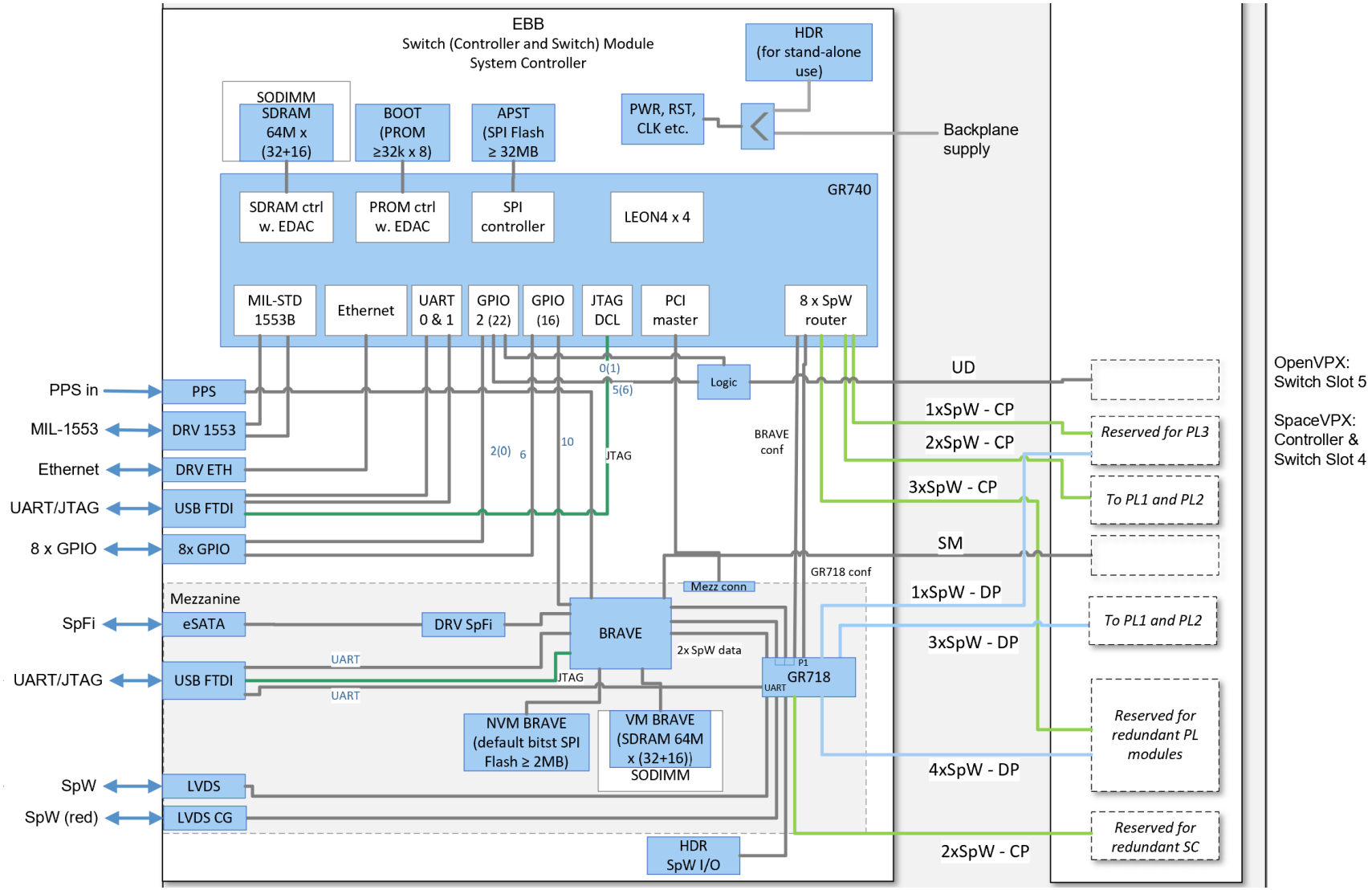
I/O Modules

- Mainly for CORA use
- Interfaces adapted to CORA-SAGE activitiy
- Supporting SpW-based redundancy concepts
- Stand-alone or backplane operation
- Limitations: no HSSL in Data Plane, no formal SpaceVPX compliance
- DIGANIF board
  - BRAVE NG-Medium
  - PCB design for SpW reconfiguration
  - SPI bitstream in CORA
- SPWIF board
  - GR718B
  - Mainly a SpW router board
  - Supporting the three redundant pairs of SpW instrument



RDHC design

EBB



RDHC design

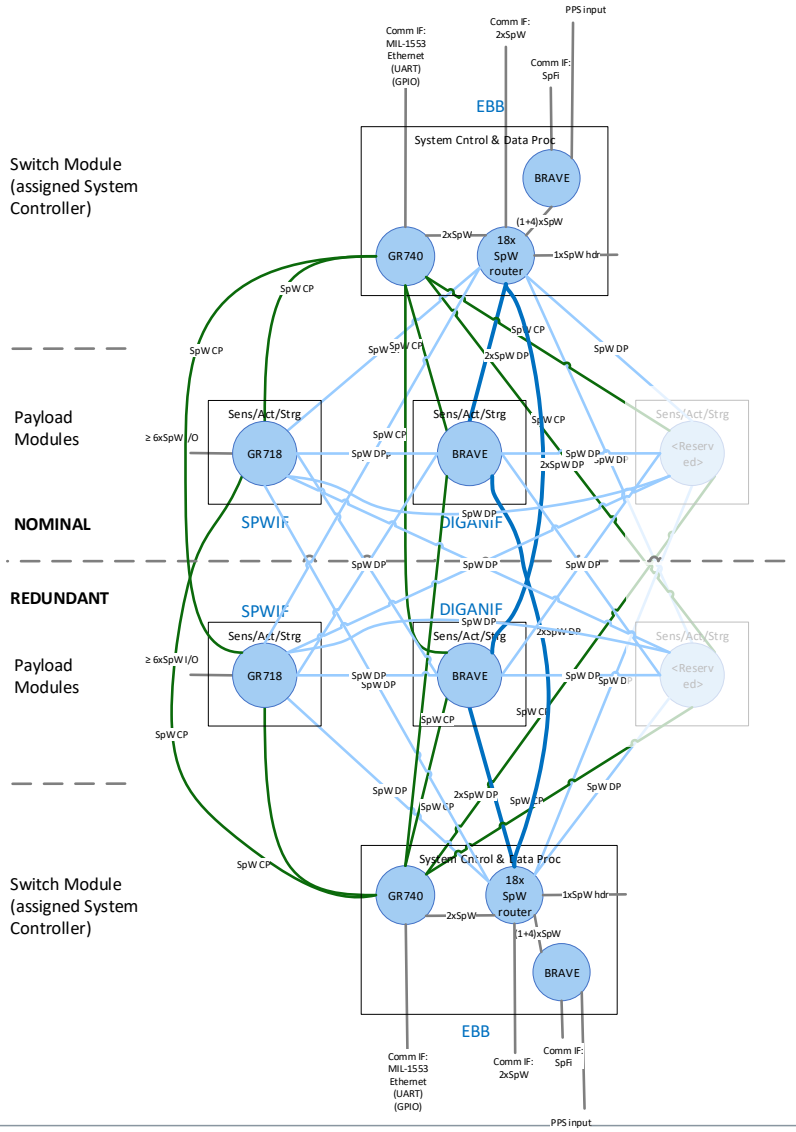
EBB

- Interfaces adapted to CORA-SAGE activity
- Supporting redundancy concepts
- Stand-alone or backplane operation
- GR740 on Main Board
- BRAVE NG-MEDIUM and GR718B on Mezzanine
  - For use in CORA
  - SpW-based reconfiguration of FPGA
  - SpFi interface routed in hardware
- Support for future Mezzanine boards
  - PCI from GR740
  - High-performance FPGA
  - SpFi routing to Data Plane
  - SpaceVPX-supported protocols

RDHC design

Module-redundant architecture

- Not used in CORA
- Path-to-flight concept
- PCB design prepared
- Currently SpW-based dataplane
- EBB supporting SpFi on Data Plane needs updated Mezzanine

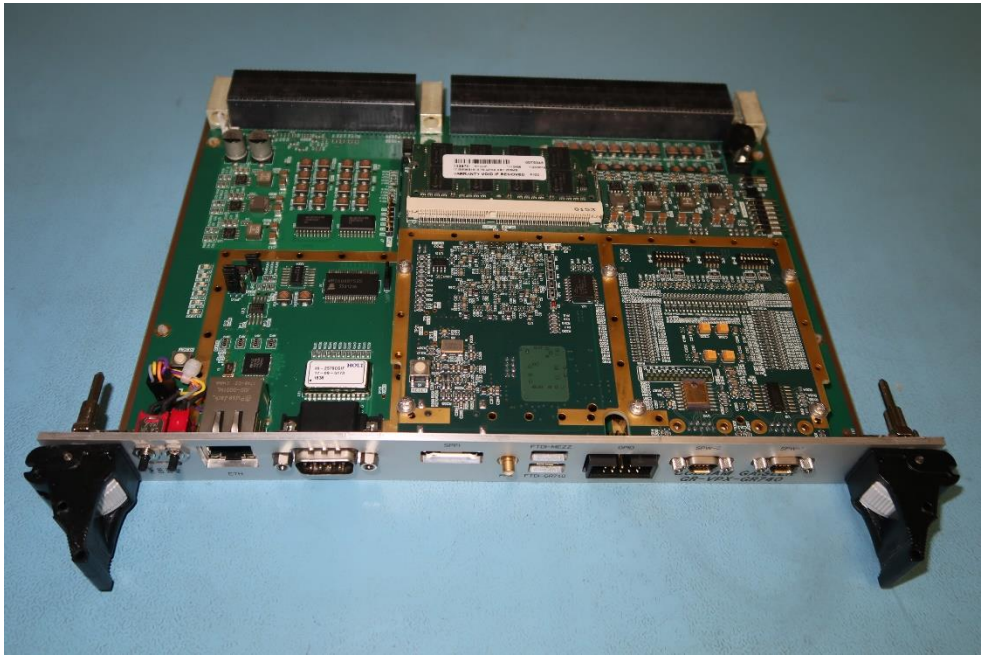


04
RDHC hardware

RDHC hardware

EBB – Main Board

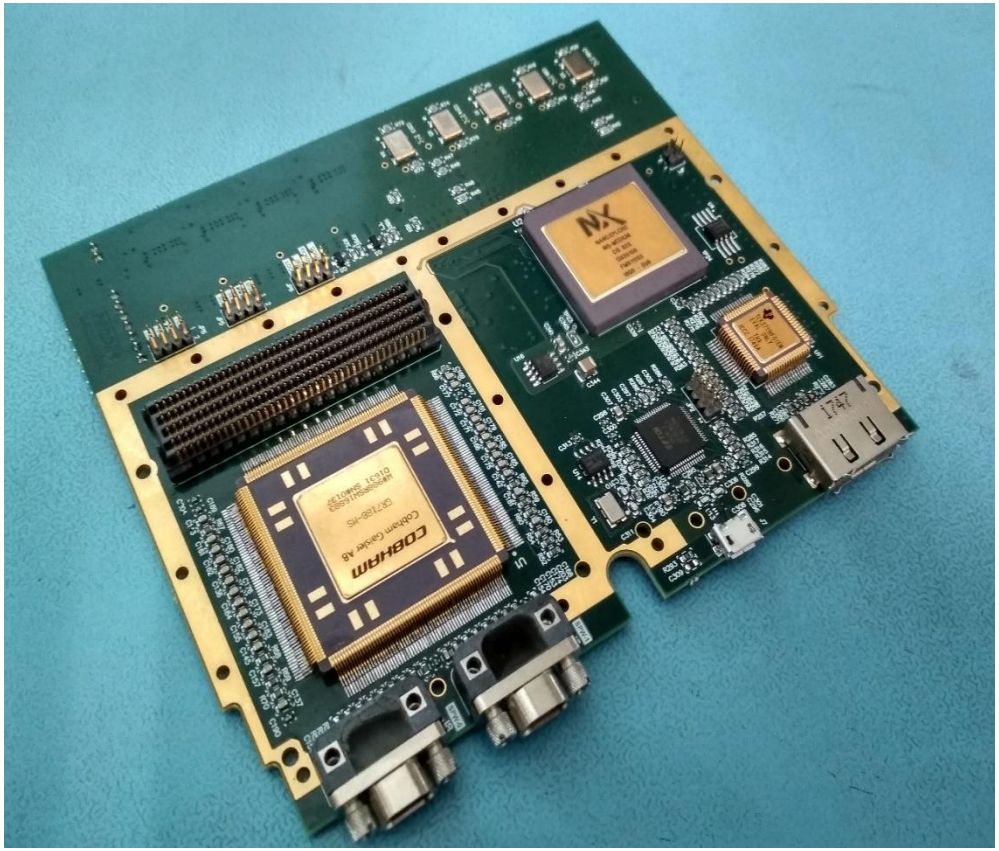
- Main Board
  - GR-VPX-GR740
  - GR740, SDRAM, SPI Flash
  - In test phase
  - Illustrated with Mezzanine Board



RDHC hardware

EBB - Mezzanine

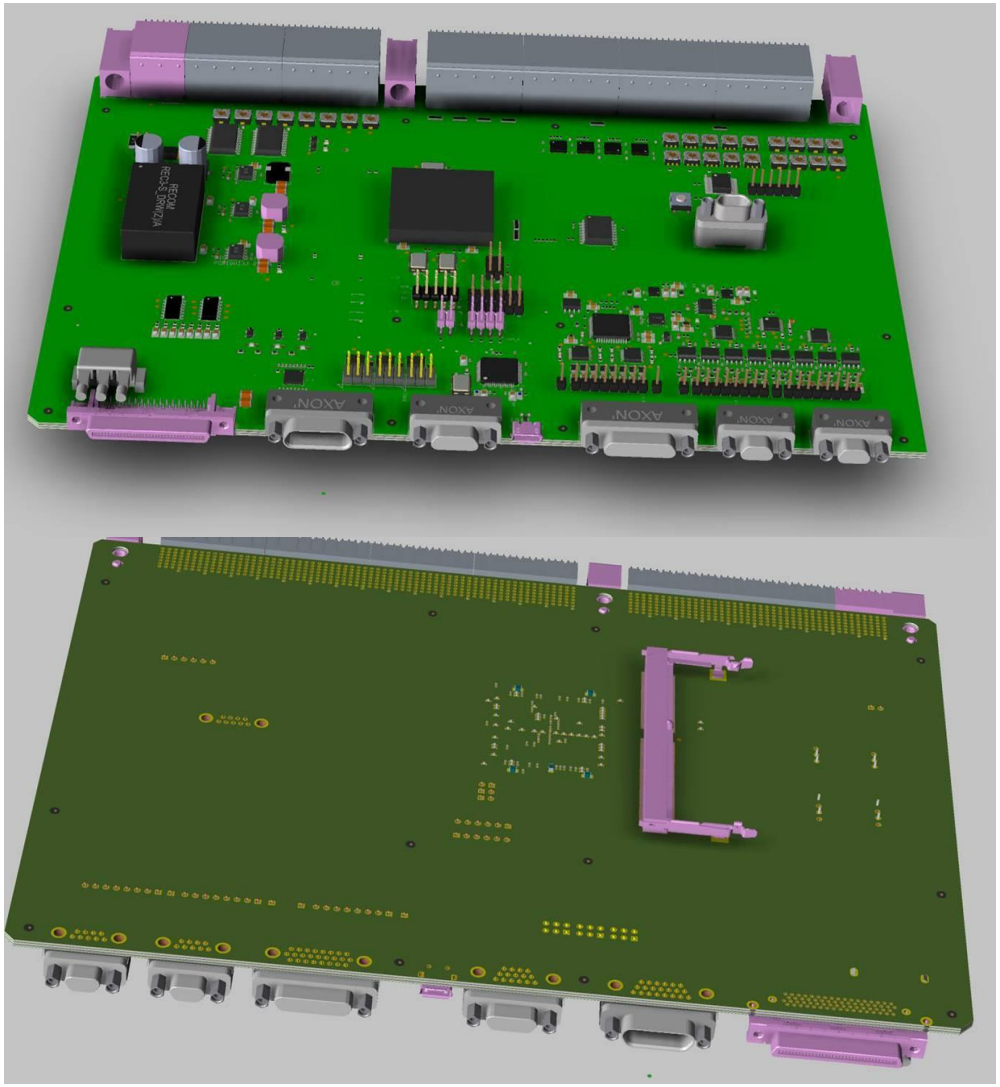
- GR-VPX-BM-MEZZ
- BRAVE NG-Medium, GR718, GR54LVDS049, SDRAM, SPI Flash
- Main parts of initial testing completed
- Successful FPGA programming using JTAG
- Successful communication with the design using UART/GRMON debug interface.



RDHC hardware

DIGANIF board

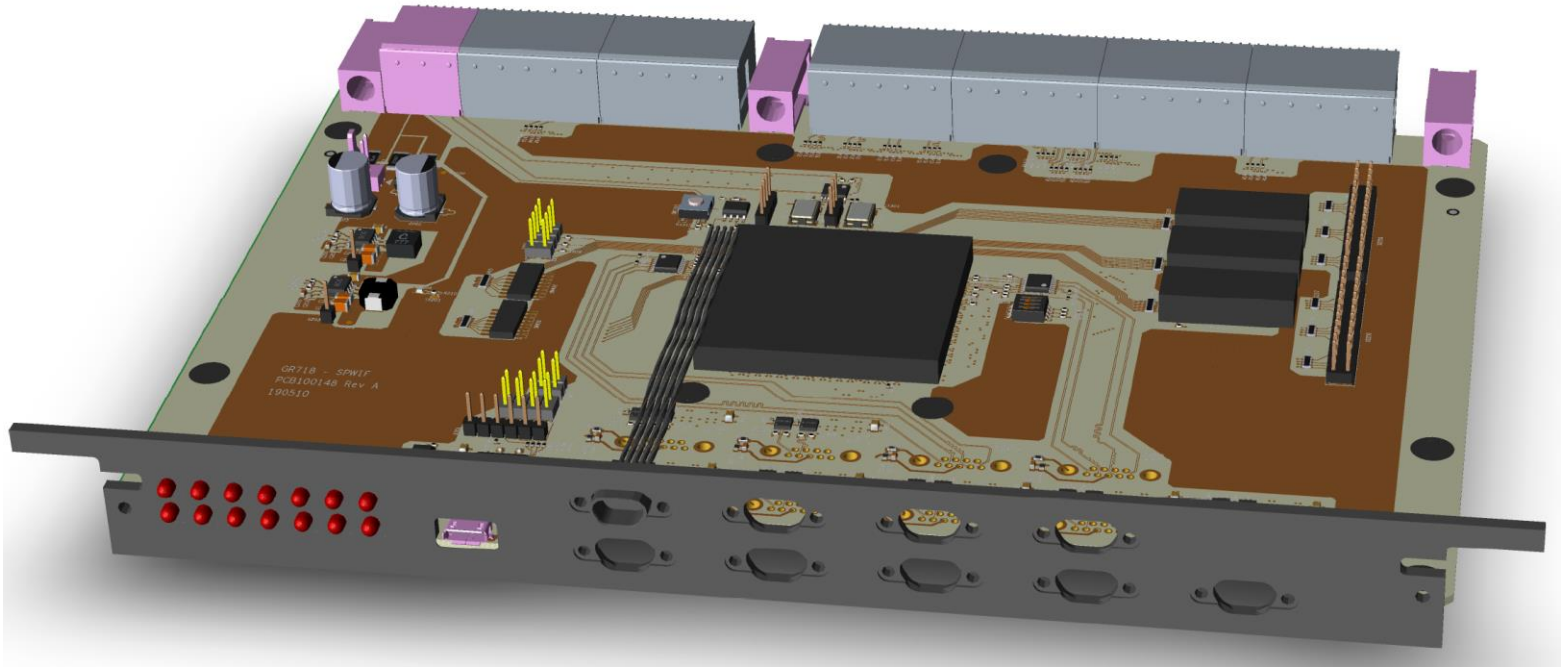
- BRAVE NG-Medium, digital and analogue interfaces
- In assembly phase
- PCB and components available
- VHDL completed



RDHC hardware

SPWIF board

- GR718B
- In PCB manufacturing phase
- All components available

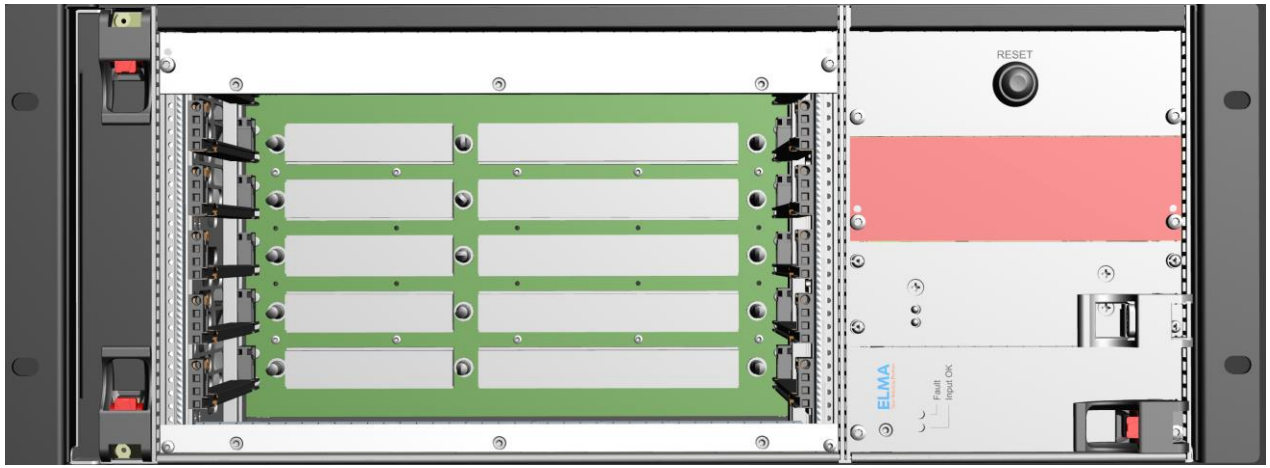


3D illustration only, colors not representative

RDHC hardware

Chassis and cabling

- Chassis
  - ELMA 6U, 5 slots
  - In assembly phase



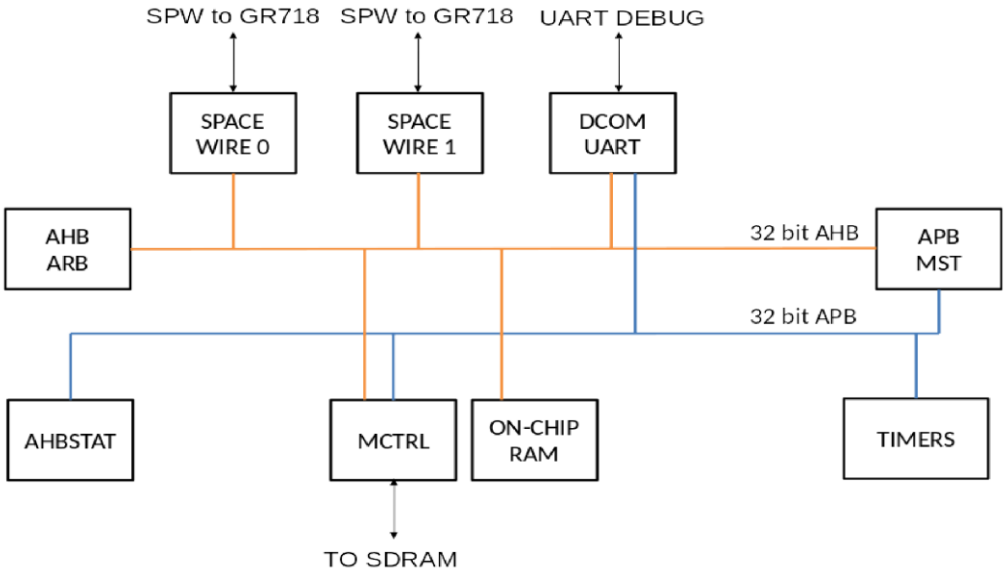
Other hardware:

- I/O cabling
  - Custom-designed
  - RDHC to SCOE (SAGE) interface
  - Partly delivered

05
VHDL Design

VHDL

EBB – BRAVE on Mezzanine

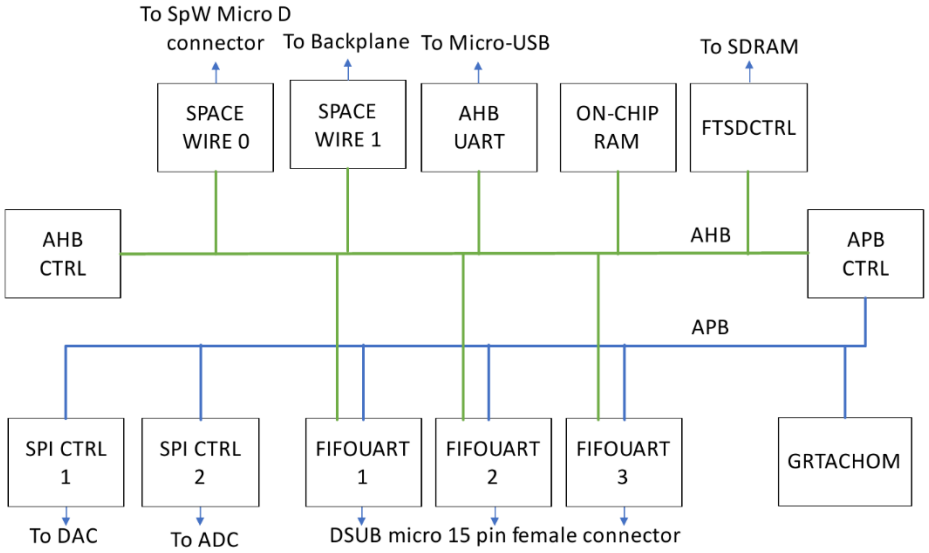


The IP cores in the design are:

- **SpaceNet – RMAP IP Core** (v 1.00) [RD2].
- **AHBARB : AHB arbiter and decoder**
- **APBMST** : AHB/APB bridge
- **AHBRAM** : On-chip RAM with AHB slave interface
- **TIMERS** : Two general pupose timers and one watchdog
- **DCOM**: UART for debug support unit
- **MCTRL** : External memory controller
- **AHBSTAT**: AHB status register. Latches the address and bus parameters when an error is signaled on the AHB bus
- **UART** with APB interfaceSystem block diagram

VHDL

I/O Board – BRAVE on DIGANIF



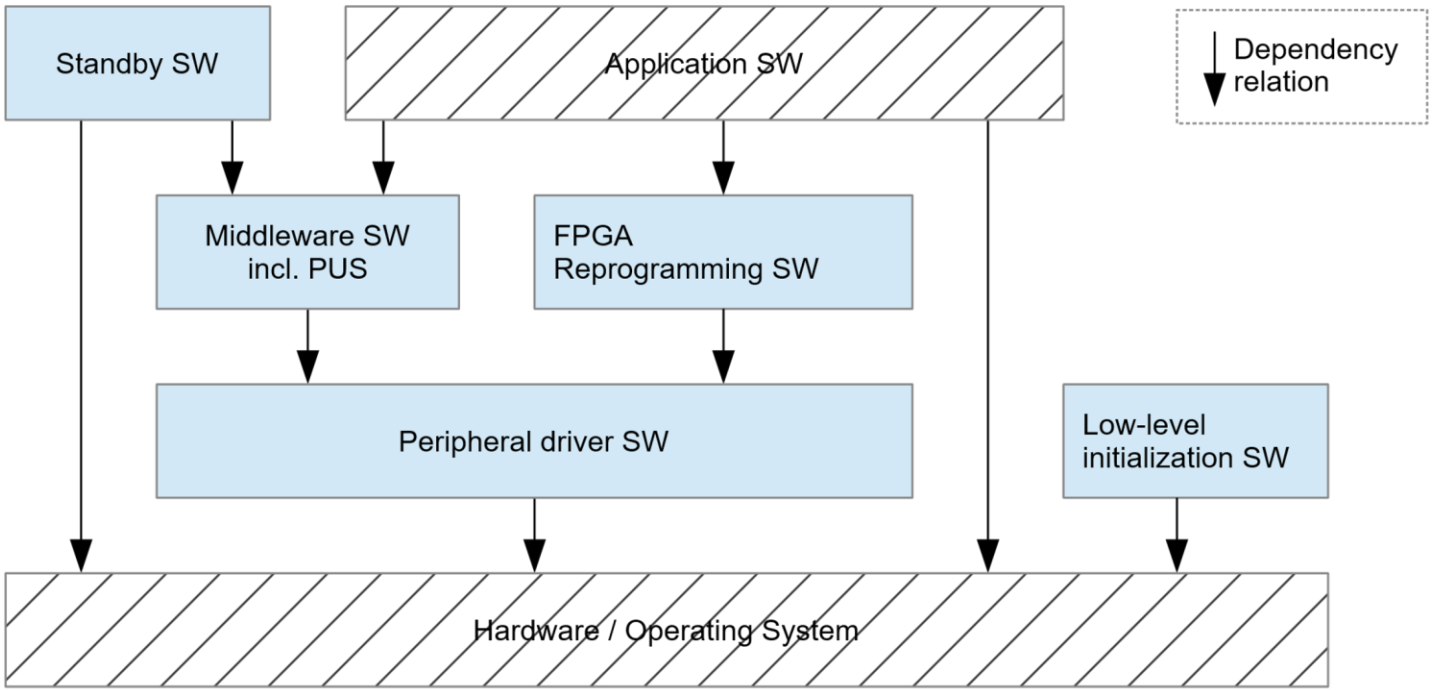
The following modules are included in the design:

- A SpaceWire codec with AHB host Interface and RMAP target
- Three UARTs with FIFO and separate baud rate generators
- Two SPI controllers, configured as SPI master, with one slave select signal and FIFO depth equal to 8.
- One AHB UART, usable as a debug Link
- An on-chip RAM, with 32 KB size
- A GRTACHOM IP, to acquire (measure) the RW Discrete Digital Tacho inputs

06
Software

Software

Overview

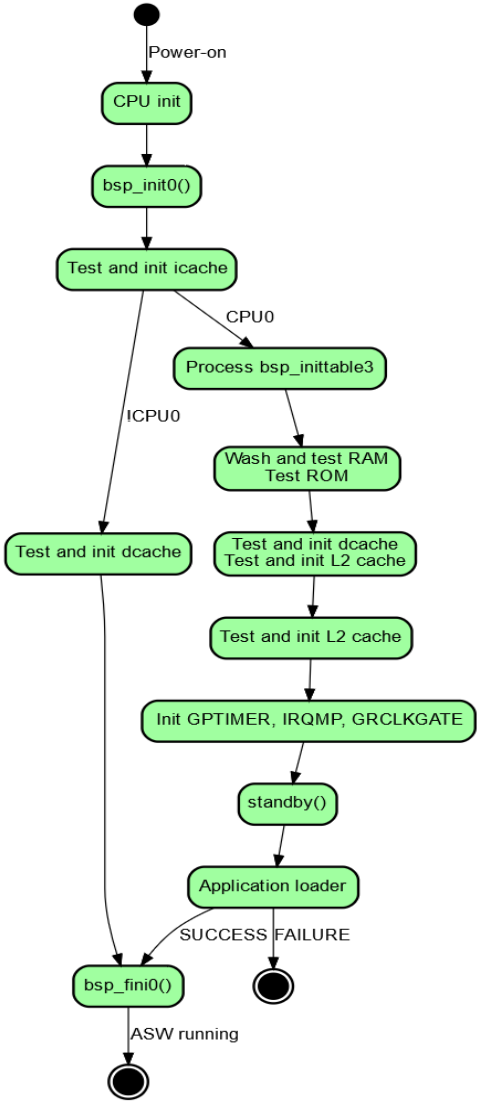


The RDHC software is delivered with the system which allows SAGE/MBAD to implement their use cases.

Software

Low-level initialization (boot)

- GR740/RDHC Boot SW
- Compliant with ESA initialization requirements
- Peripheral initialization
- Self-tests
- Application loader
  - Application stored in SPI flash
- Support for SMP boot
  - RTEMS
  - Linux, VxWorks
- To be available as a product outside CORA



Software

Peripheral drivers

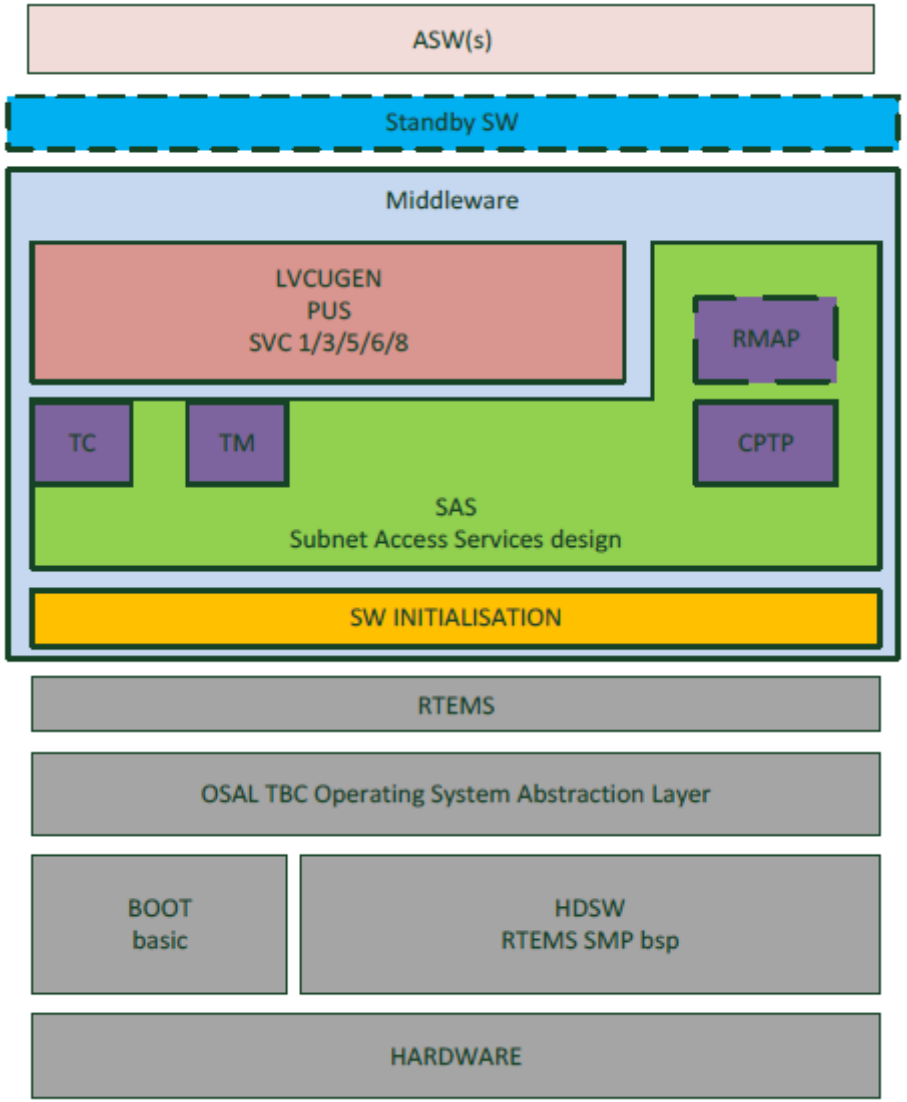
- RDHC Drivers (SW and API doc.)
  - SPI controller
  - SPI flash
  - GPIO
  - Timer
  - Clock gating unit
- The execution environment is RTEMS-5 SMP

- Also provided
  - RMAP transaction example
  - Flash access example

Software

Middleware and Standby

- Provides an application layer with an abstraction suitable for RDHC operation
- Such as configuration of the SpaceWire router, GPIO and SPI flash management
- Implementation of all level 2 OSI layers of interface of the study
- Implementation of level 3 OSI layers for various space standards protocols (TM/TC CCSDS PUS, RMAP, CPTP) and Ethernet UDP/IP for debug purposes.



The middleware provides PUS services over SpaceWire:

- Service 1: TC ack and completion
- Service 3: Housekeeping TM report management
- Service 5: Event report management
- Service 6: Memory management for accessing non-volatile memories.
- Service 8: Function management for custom commands.

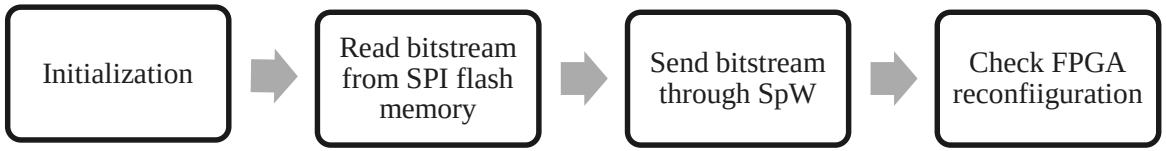
Service 6 and 8 allows for

- Upload a file to the on-board FPGA bit-stream memory.
- Initiating FPGA reconfiguration using the FPGA reconfiguration engine.

Software

FPGA reconfiguration

- The FPGA reconfiguration SW provides an interface to reconfigure the FPGA on the EBB.
- The bitstream to configure the FPGA is selected through a run time parameter.
- Monitor dedicated FPGA status signals so that the GR740 software can take appropriate actions on FPGA events.



07
Summary

Major results and challenges and way forward

Summary

Major results

- COTS BB platform delivered
  - Supporting MBAD and SAGE activities
- RDHC hardware developed
  - Processing Module (EBB) with GR740 and BRAVE NG-Medium – testing on-going
  - Sensor and Actuator I/F modules – in assembly phase
  - Chassis and I/O cabling - in assembly phase
- VHDL code delivered
  - For BRAVE NG-Medium on the Processing Module and I/O Module
- Software developed
  - Boot software and basic drivers delivered
  - Middleware software partly delivered
  - FPGA reconfiguration software partly delivered

Summary

Major challenges

- Three parallel CORA activities
  - Requirements and interfaces defined during the activities
  - External dependency
  - Focus of eliminating blocking points
  - Consolidation at workshops
- In addition, another dimension of requirements
  - Consolidation with ESA
  - Path to flight
    - Redundancy concepts
    - Form factor
  - Platform for reconfiguration concepts
- Planning and resources for review
  - Internal, partners and ESA
  - Driving schedule

Summary

Way forward

- In the CORA-RDHC activity
  - Finalize hardware manufacturing and initial testing
  - Finalize software development
  - Deliver selected parts to CORA consortium
  - Prepare and perform ESTEC Avionic Lab testing with CORA partners
  - Complete all deliverables
- Potentially, after CORA
  - Develop mezzanine for EBB with SpFi?
  - Descope EBB module for 3U form factor?
  - SpaceVPX-variant of the EBB?

COBHAM

Thanks for listening!