HOW TO IMPROVE QUALITY IN THE CAN PHYSICAL LAYER

CAN in space workshop

Gothenburg June 13, 2019

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www.kvaser.com

Main factors that defines the quality of the physical layer

1. The CAN-bus layout
2. The quality in the cable and connectors
3. The bit-configuration in all connected CAN-controllers
4. The oscillator tolerance for the CAN-logic
5. The quality of the CAN-drivers

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The CAN-bus layout

- Secure a continues impedance through the length of the CAN-bus
  - Use the same cable impedance in all sections
  - Match the termination to the cable impedance
  - Connectors must match the impedance in the cable

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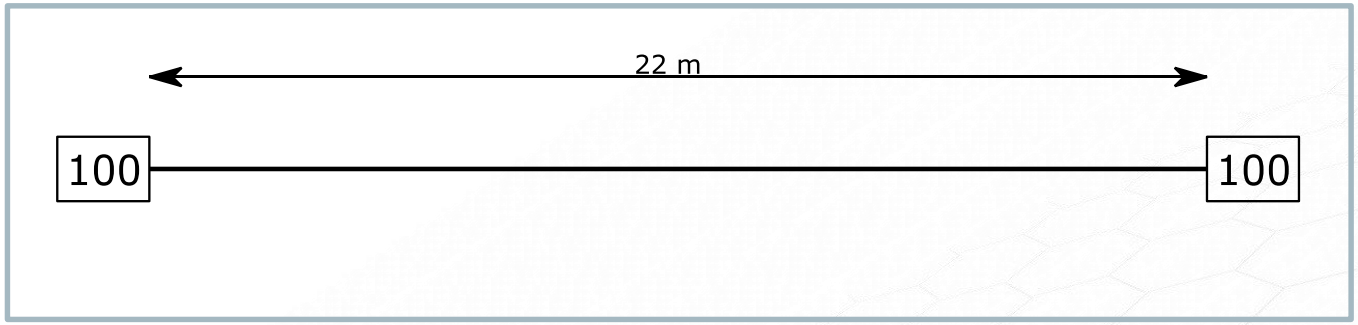
Optimal communication link



- Point to point
- The same cable over the hole cable length
- Impedance matching in both ends at both sender and receiver
- Unlimited bit-rate, but skin effect above 400 Mbit/s

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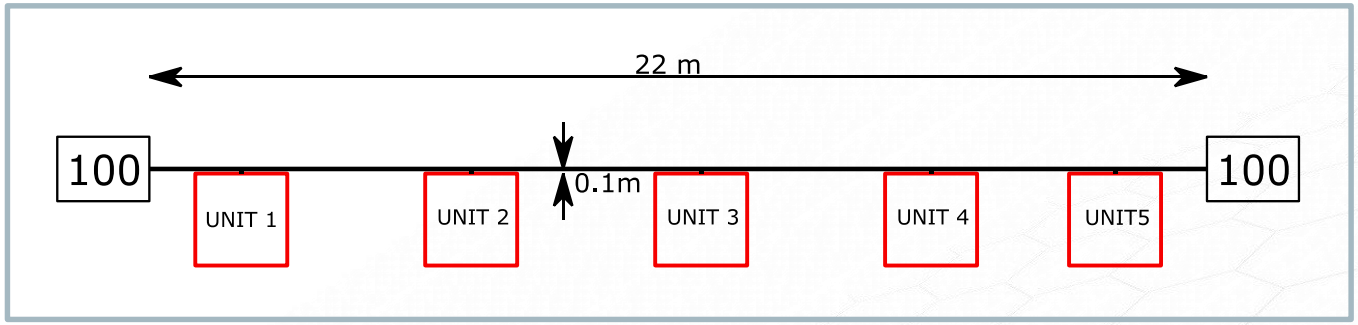
Optimal CAN-bus 0.1 m drop lines



- The impedance miss match is only 10 centimeter (2*0.5 nanosecond)
- Which is invisible for a slew-rates less than 5 nanosecond
- Which should be enough for a bit-length of 25 nanosecond
- Which corresponds to **40 Mbit/s**

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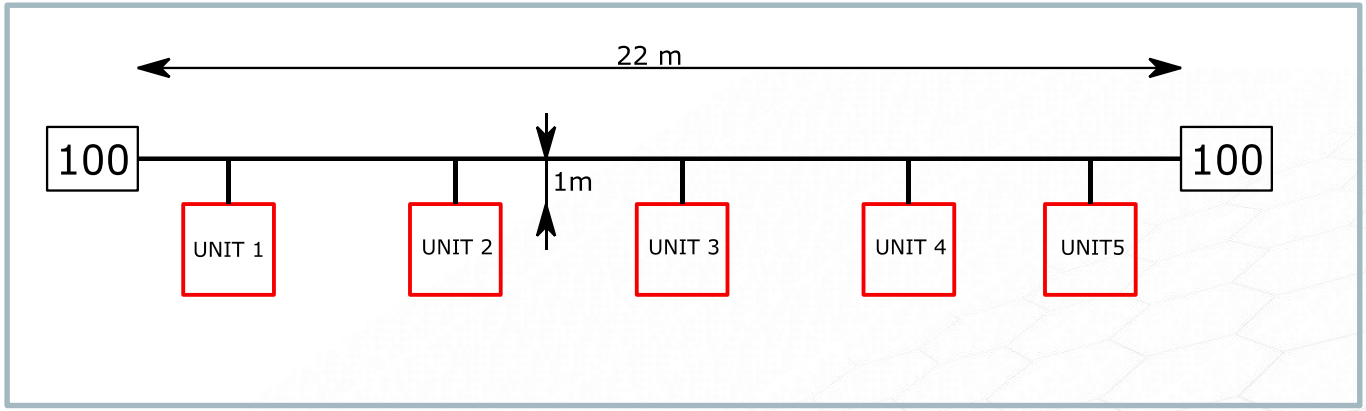
Good CAN-bus 1 m drop lines



- The impedance miss match is only 1 meter (2*5 nanosecond)
- Which is invisible for a slew-rates less than 50 nanosecond
- Which should be enough for a bit-length of 250 nanosecond
- Which corresponds to **4 Mbit/s**

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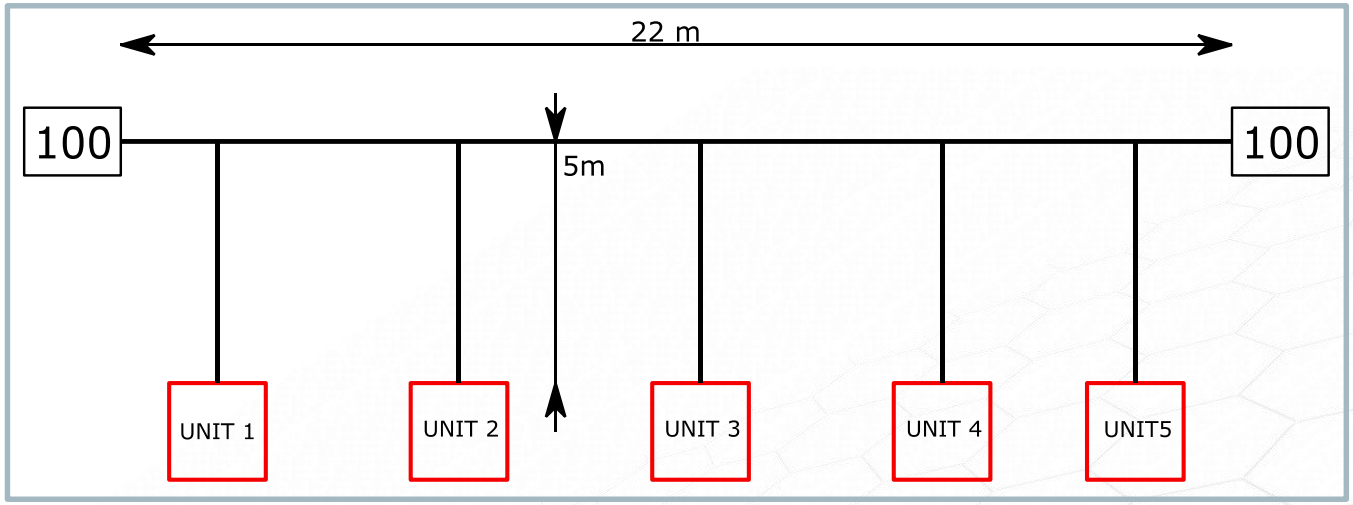
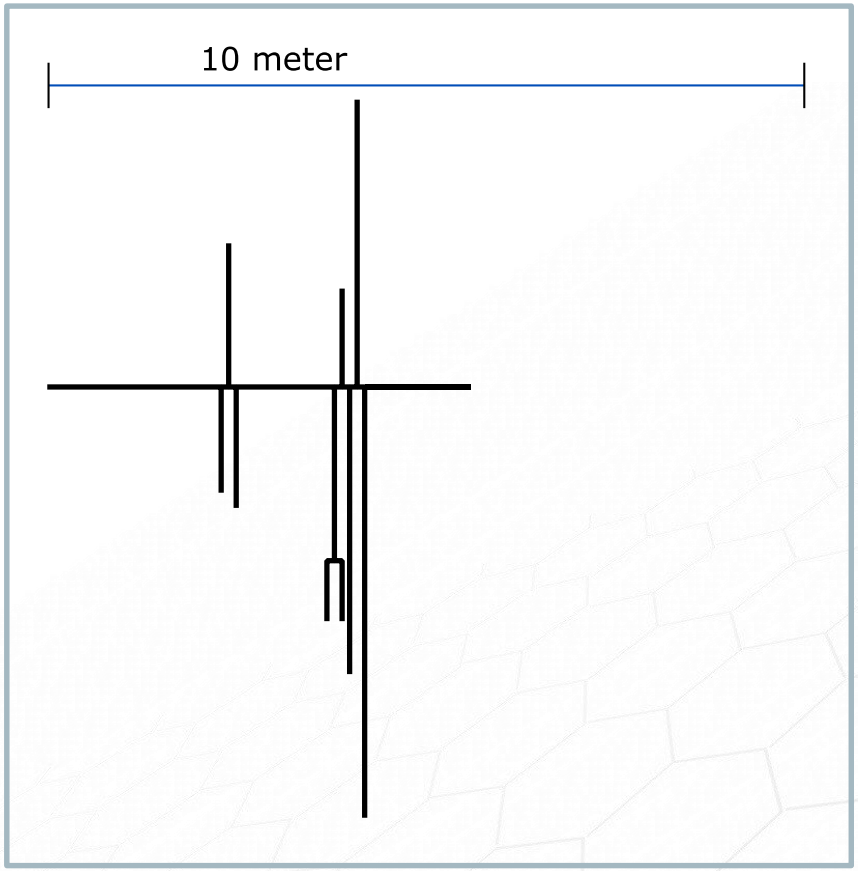
Bad CAN-bus 5 m drop lines



The impedance miss match is 5 meter (2*25 nanosecond)
Which is invisible for a slew-rates less than 250 nanosecond
Which should be enough for a bit-length of 1250 nanosecond
Which corresponds to **800 kbit/s**

A typical Automotive installation.



- The impedance miss match is 5 meter, but it is not evenly distributed.
- Which reduce slew-rate to 400 ns.
- Which demand a bit-length of 2000 nanosecond
- Which corresponds to **500 kbit/s**

Problem adds up

- Small distortion in connections adds up with each unit installed
- Distortion become worse if units are not evenly spread over the cable length
- EMC-filter, capacitors and inductors in the ECU, could increase the problem

Slew-rate

- If a higher slew-rate is used it will result in oscillation at the bit-edge.

The CAN-bit configuration considerations

- The CAN-bus delays
  - Cable delay 5 nanoseconds/meter
  - Propagation delay in CAN-driver, 20 to 400 ns
  - Propagation delay in galvanic isolation 10 to 100 ns
- Oscillator tolerance in each CAN unit.
  - Typical +/- 100 ppm for crystal oscillators
  - CAN support up to +/- 15000 ppm

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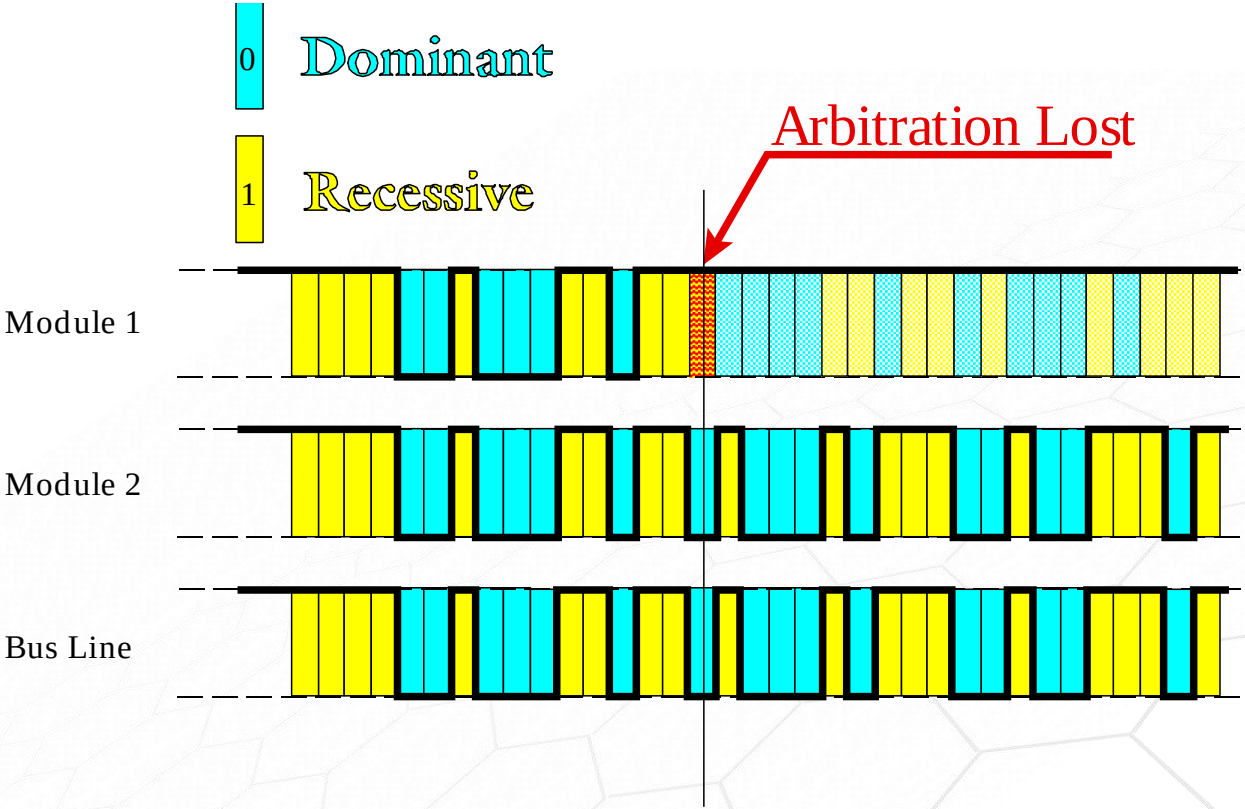
Bit-wise Arbitration



Bit-wise Arbitration

The green node starts transmisson of a recessive bit on the idle bus.

Bit-wise Arbitration

The wave from the green node has not yet reached the red node. To this the bus is still free and the red node starts transmitting a dominant bit.

Bit-wise Arbitration

Now the green node can see that there is a dominant bit on the bus and that it has lost arbitration.
Thus a transmitter has to wait until the wave has reached the most distant node and **back** (plus internal delays) before judging the bus-line level

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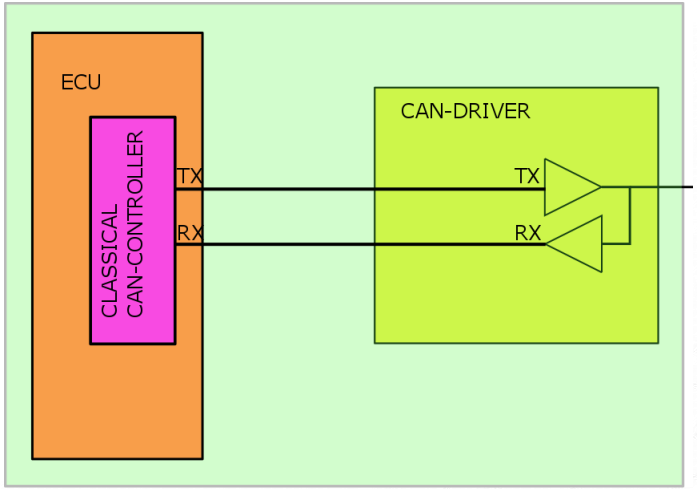
Added to the Cable delay there is also delays in the ECU



- CAN-driver delay 20 to 200 ns from TX to CAN-bus
- CAN-driver delay 20 to 200 ns from CAN-bus to RX.
- Delays in galvanic isolation between CAN-controller and CAN-driver, 10 to 40 ns.

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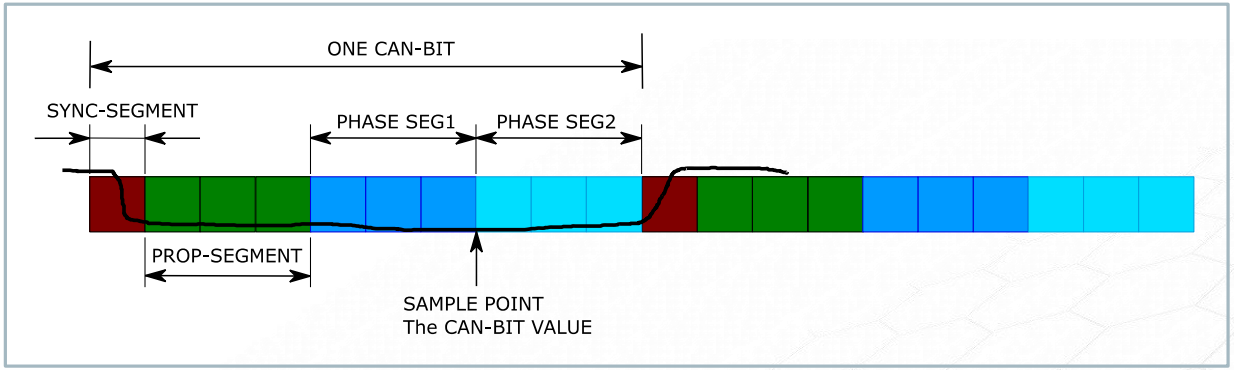
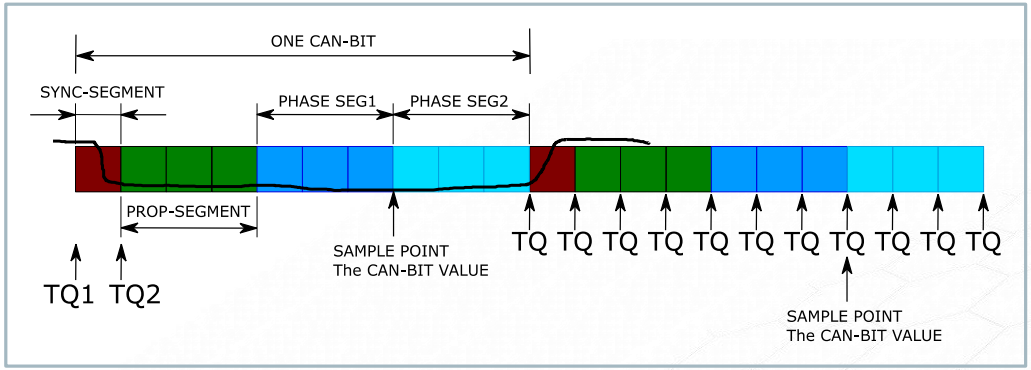
The different segments in a CAN-bit



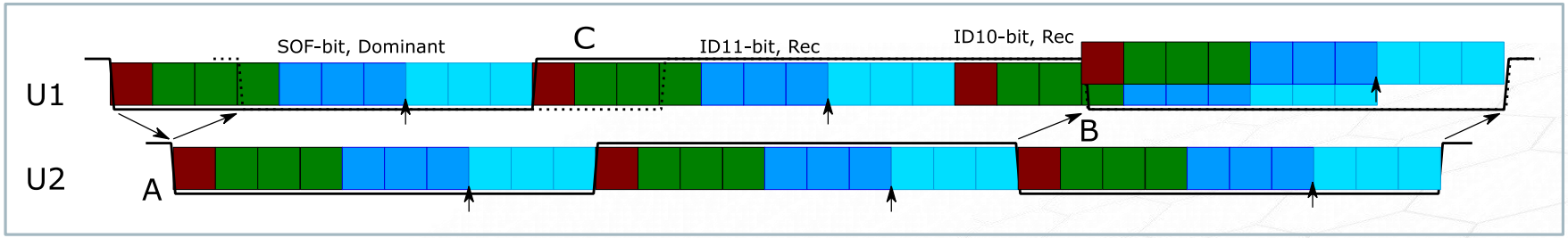
- The Bit-edge should be located in the Sync-Segment
- Propagation segment follows after the sync-segment. This part must be large enough to handle all phase shift caused by delays
- The two Phase Segments should be large enough to cover all phase shift caused by the clock offset in-between different units.

The different segments in a CAN-bit



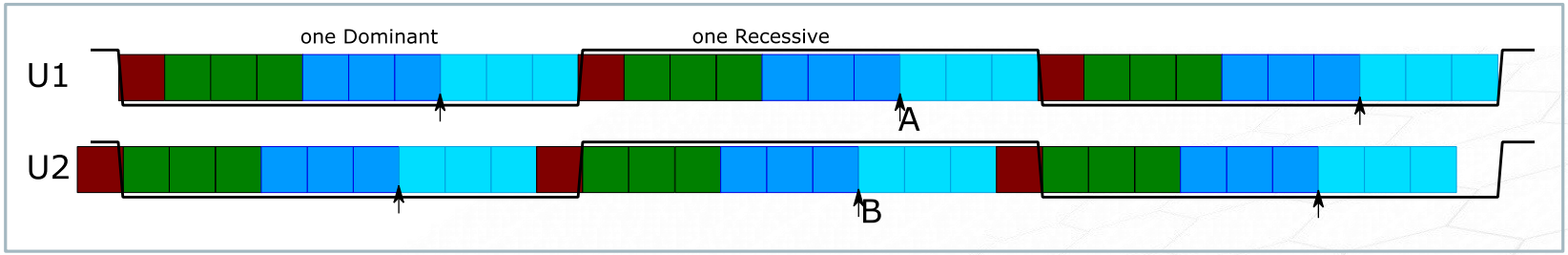
- The bit is sampled in every TQ Time Quanta.
- In TQ1 is the level sampled Recessive.
- In TQ2 is the level sampled Dominant. This must be an bit edge and the TQ between TQ1 and TQ2 is the SS Sync-Segment.
- Only Recessive to Dominant edges are used to relocate SS.

Phase shift during arbitration



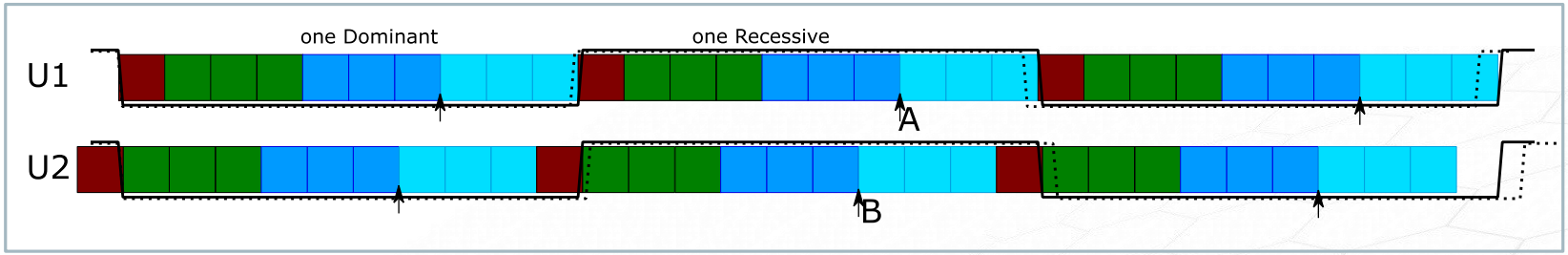
- Unit U1 is starting the CAN-frame on an Idle CAN-bus
- This SOF edge is delay 1.5 TQ before it reach U2 and during this time this unit is allowed to start a new CAN-frame as late as A.
- U1 is losing the arbitration at B, and this edge is delay 2x 1.5 TQ, and will be compensated by the SJW at B.
- The three TQ at C will dominant due to the Dominant signal from U2.

Phase shift due to TQ resolution



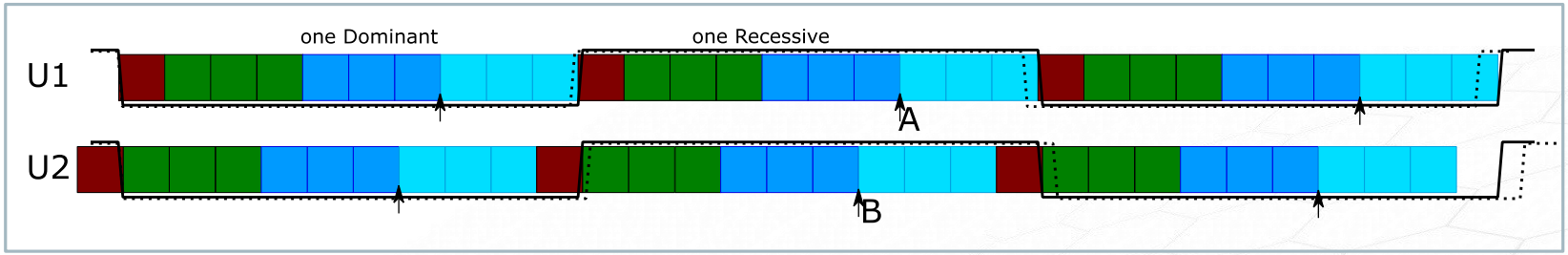
- Unit U1 and U2 is located at the same location and receive the edge at the same time.
- This will result in different units are sampling the the bit different in time A and B.

Phase shift due to clock offset



- The maximum allowed clock offset in CAN is +/-1.5% which +/-15000 ppm
- The clock offset between two unit can be maximum 30000 ppm
- The dotted line at U1 indicate a signal from a unit with 3% faster clock.
- The dotted line at U2 indicate a signal from a unit with 3% slower clock.
- The phase offset is relative small over one bit.
- The phase shift will increase linear over the number of CAN-bits.

Phase shift due to clock offset



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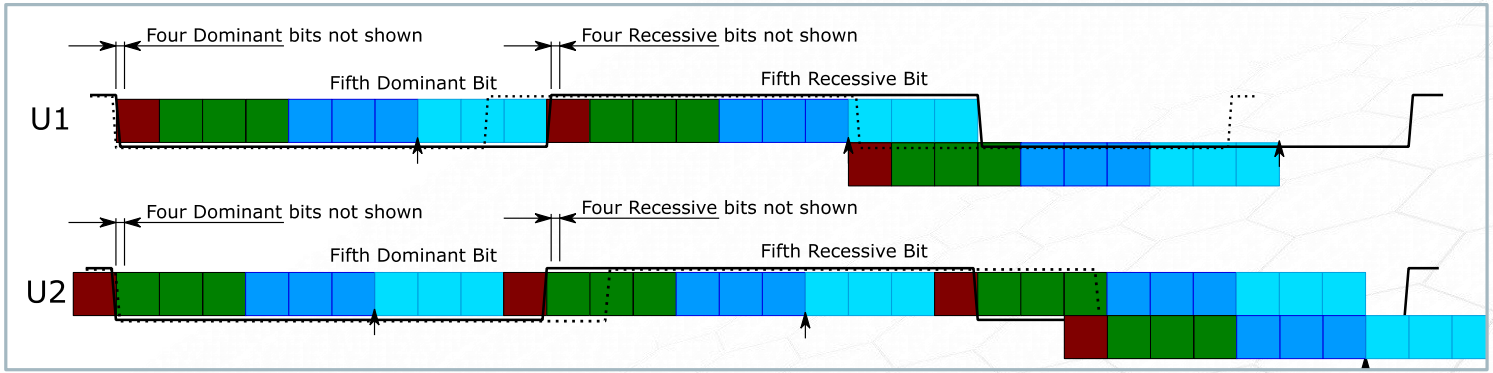
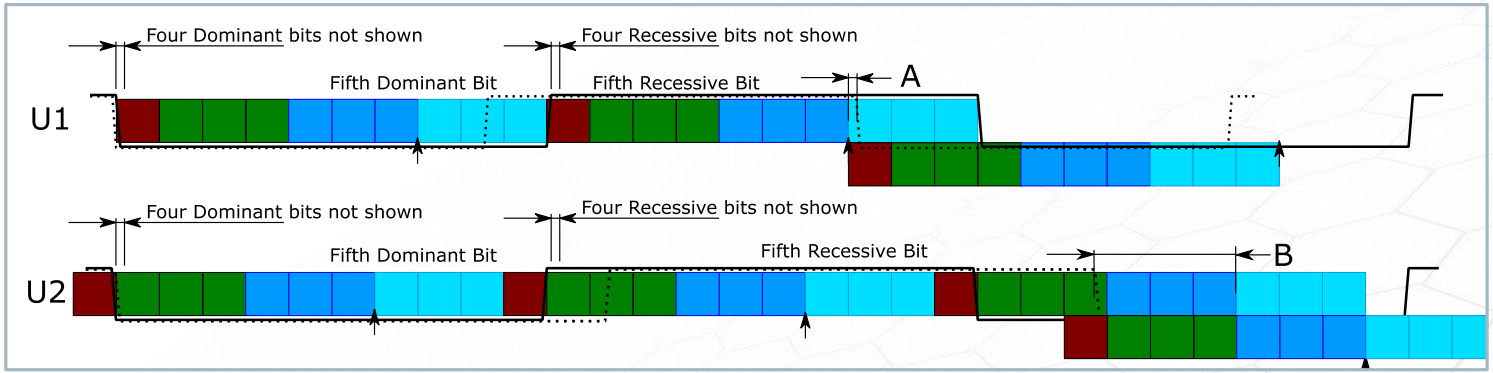
Phase shift due to clock offset over maximum 10 CAN-bits



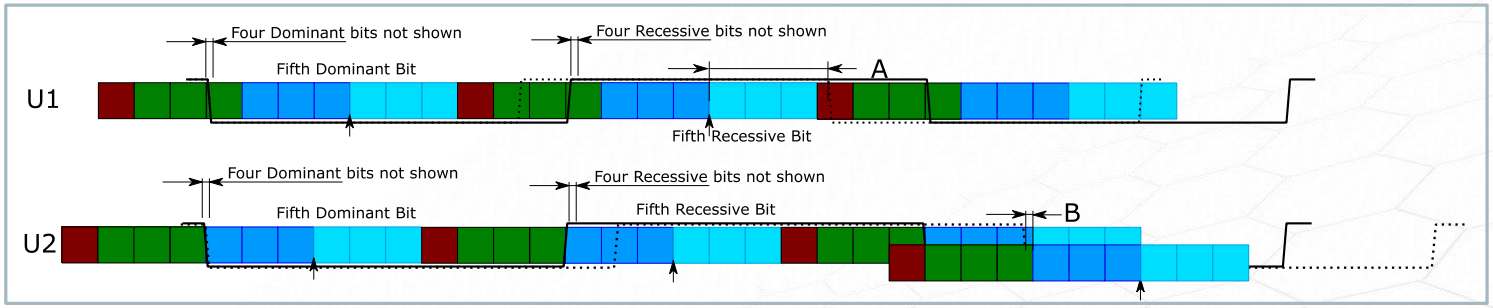
- Five Recessive plus Five Dominant bits is the longest sequence between two Recessive to Dominant edges.
- The maximum phase shift over 10 bits is 30%
- The SJW must be 3 TQ in this case to correct the phase shift.

Phase shift due to clock offset over maximum 10 CAN-bits



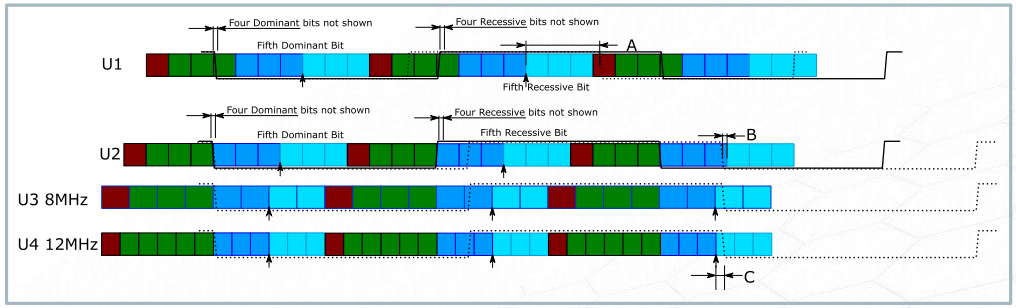
- The phase margin for shorter bits at A is very small and minor phase noise could cause wrong bit value sample
- The edge in shorter bits will be somewhere in Phase Segment 2
- The phase margin for longer bits at B is large
- The edge for longer bits will be somewhere in the Propagation Segment.

Phase shift due to clock offset and Arbitration over 10 CAN-bits



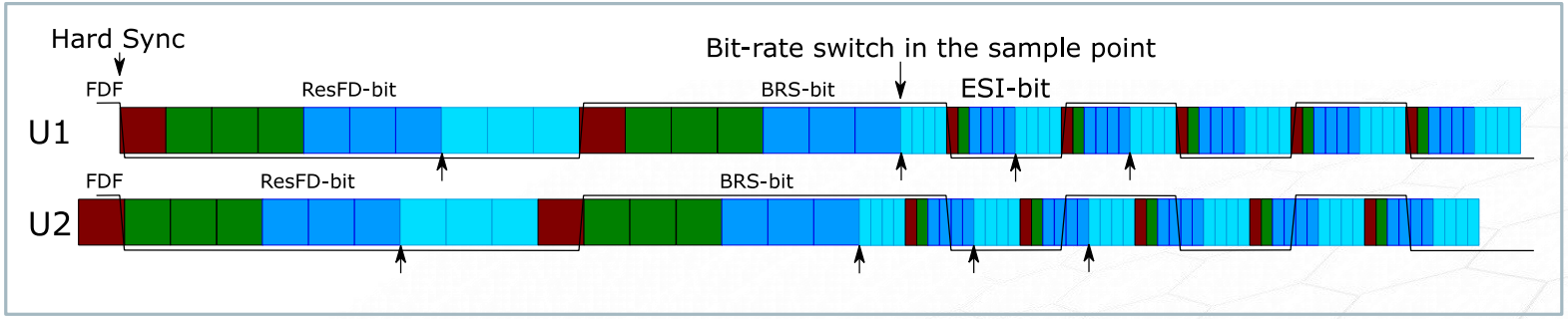
- The phase margin for shorter bits at A is large
- The edge for shorter bits will be somewhere in the Propagation Segment
- The phase margin for longer bits at B is very small and minor phase noise could cause wrong bit value sample
- The edge in longer bits will be somewhere in Phase Segment 1
- Note that the phase adjustment at B is limited to SJW=3TQ

Phase shift due to clock offset and Arbitration over 10 CAN-bits



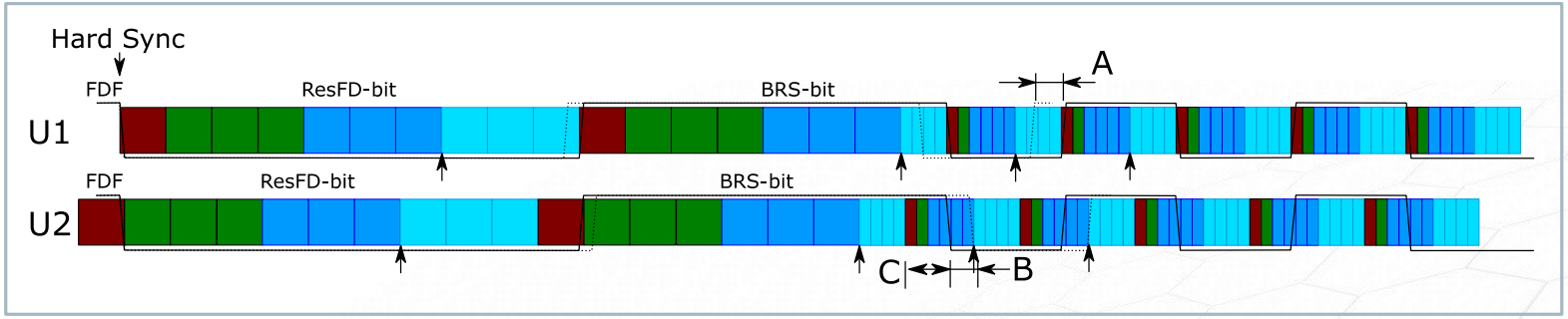
- U1 and U2 is using 10 MHz clock, U3 8 MHz and U4 12 MHz.
- The sampling is done C to early with wrong bit-value.
- With U3 and U4 maximum clock offset is 2.5%
- It is possible to increase the number of TQ in phase segment 1 and 2 for U3 and U4 but this will reduce the Propagation segment.

Phase shift in the BRS-bit for CAN FD



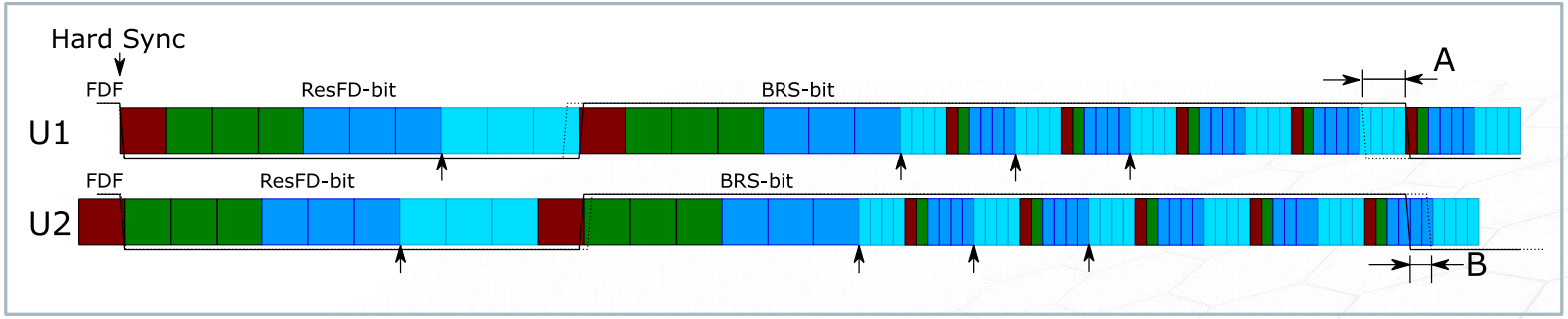
- In this exampel is the data-rate 4x the arbitration bit-rate
- The bit-rate switch is done at the sample point in the BRS-bit
- CANFD units will do a Hard Synchronization at the end of the FDF-bit
- The ESI-bit is normally Dominant
- The ESI-bit is Recessive only if the sender is Error-Passive

Phase shift in the BRS-bit for CAN FD



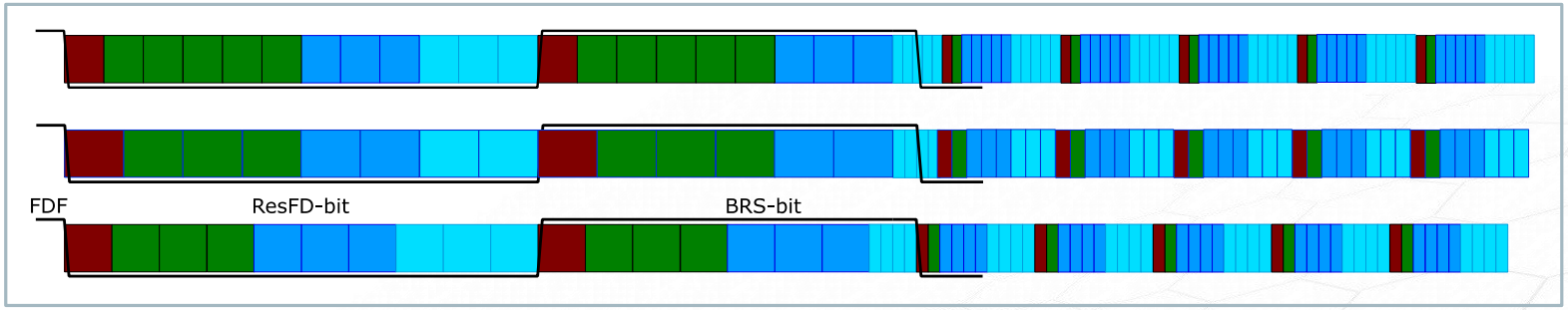
- U1 is in perfect synchronization with the transmitter
- In U1, a 3% faster sender clock will cause a phase offset A=2.5dTQ
- U2 has the edge late in the Sync-Segment causing a phase offset C=4dTQ long.
- In U2, a 3% slower sender clock will cause a phase offset B=2.5dTQ
- The two phase offset in U2 will reach the sample point in the first data-bit

Phase shift in the BRS-bit for CAN FD



- The worst case will occur when sender is Error-Passive, ESI-bit Recessive
- Then there could BRS-bit plus four more data-bits an before synchronization edge
- U1 is in perfect synchronization and could handle 3% clock offset.
- U1 with a 3% faster sender clock will cause a phase offset A=4dTQ.
- U2 has the edge late in the Sync-Segment and can only handle 1.5% offset.
- U2 with a 1.5% slower sender clock will cause a phase offset B=2TQd, which is added to the Phase offset caused by the late FDF-edge.

Phase shift due to SAMPLE POINT



- An offset in the arbitration sample point will cause phase offset in data-bits at the BRS
- This will be worse due to phase offset in the Sync-Segment in the ResFD-bit.
- Solution;
  - Use clocks that makes it possible to get common sample point
  - Use as small TQ as possible to reduce the Sync-Segment offset.
  - Use as small TQ to make it possible to get a common sample point.

The CAN-driver

- The propagation delay must be short in system with:
  - Long cables
  - High bit-rates
- High slew-rate is necessary for high bit-rates;
  - But demand optimized CAN-bus layout to prevent ringing and EM emission

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Basic CAN-bit rules

- **Propagation Segment** must be large enough to cover all propagation delays
- **SJW** must be large enough to match the clock offset
- Unnecessary large SJW could cause over compensation due to phase noise
- **Phase Segment 1 and 2** must be large enough to fit the SJW
- Many TQ in the CAN-bit, will improve the quality

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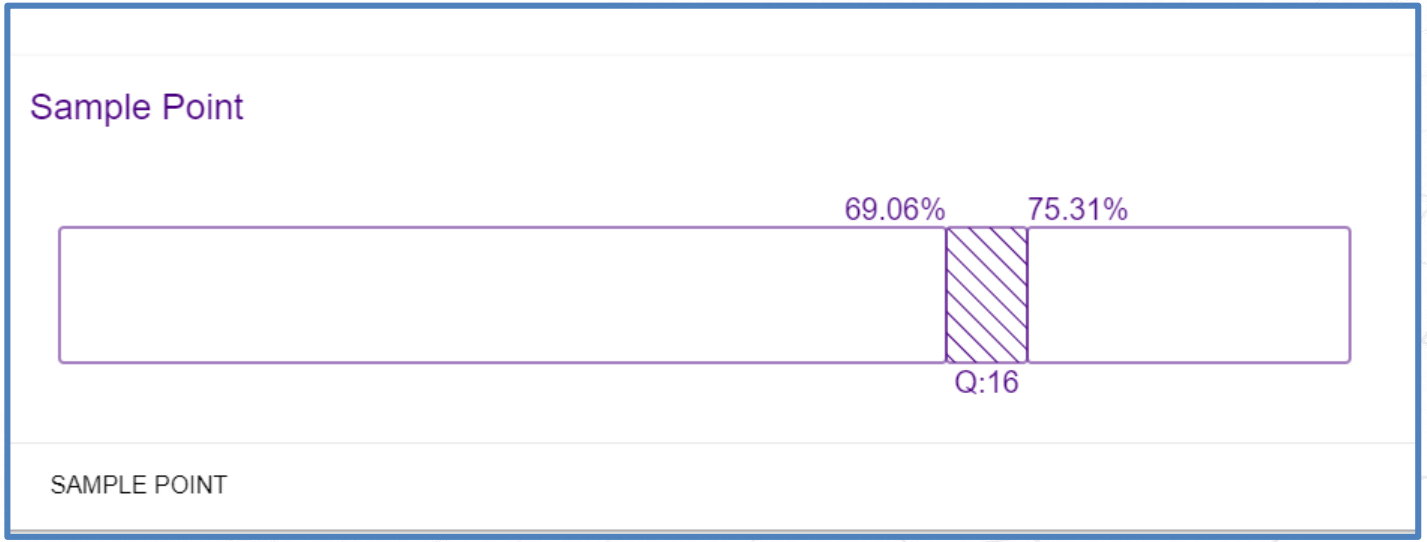
Kvaser CAN-bit checking tool Provide:

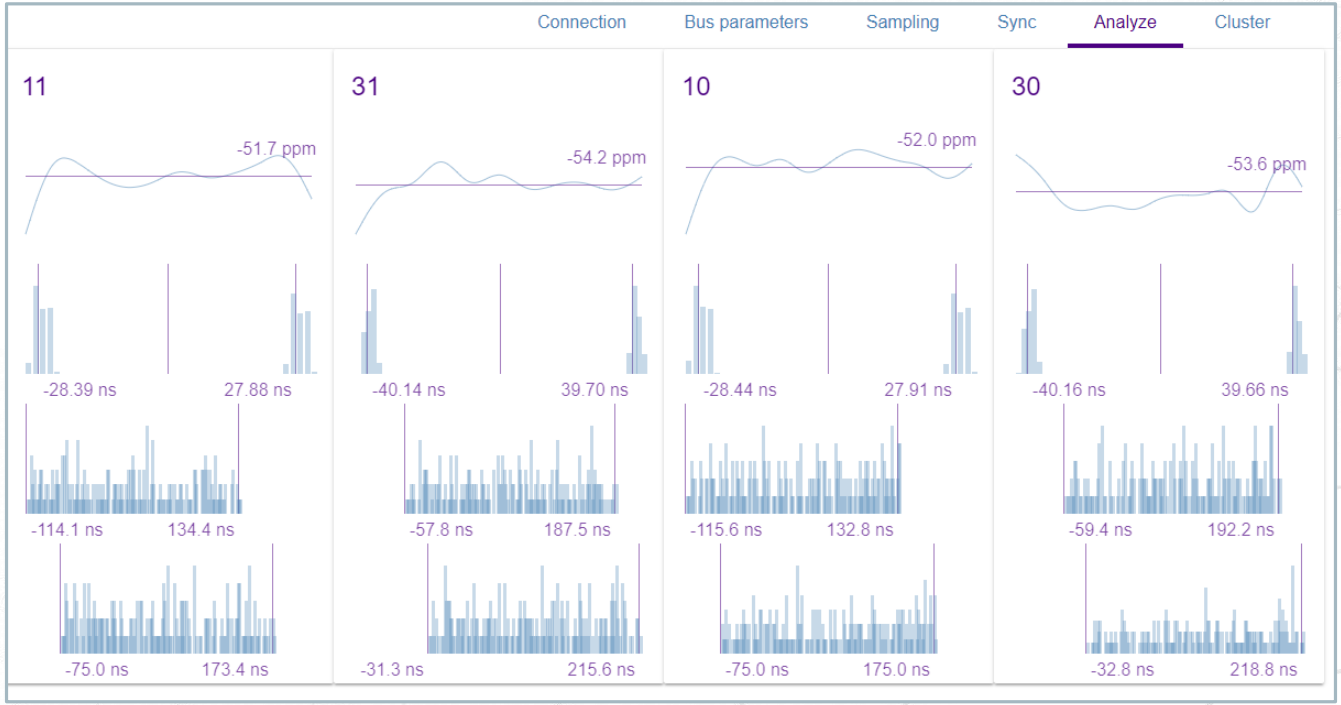
- Sample point location.
- Time Quanta Length
  - Number of TQ in the CAN-bit
- CAN-clock offset.

Kvaser CAN-bit checking tool
Bitrate checker:

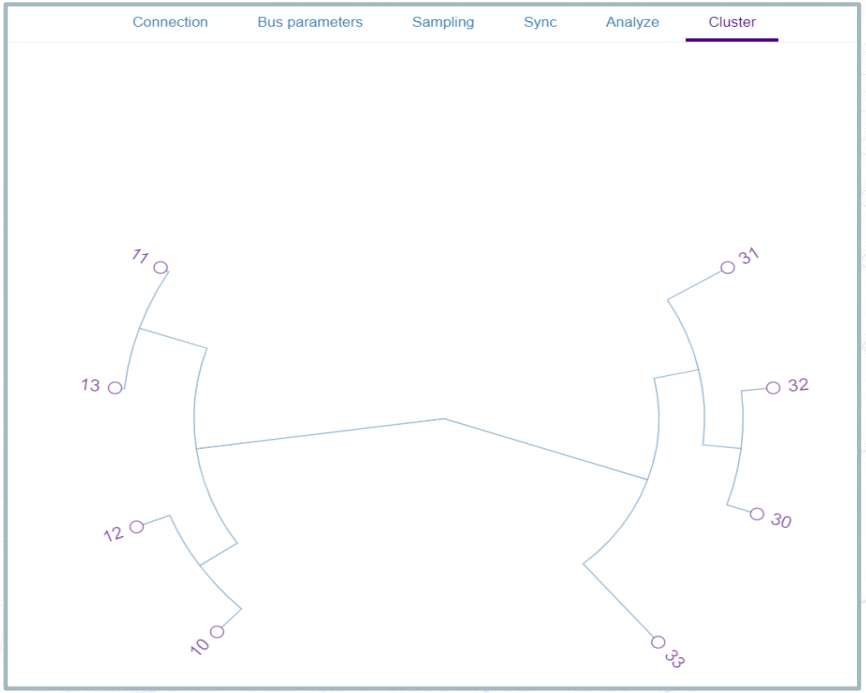
Kvaser CAN-bit checking tool Sample point and TQ-length:



Kvaser CAN-bit checking tool clock offset and Dom/Rec relation:



Kvaser CAN-bit checking tool CAN-ID cluster:



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Thank You!

QUESTIONS?