CAN XL THE NEXT GENERATION OF CAN

CAN in space workshop Gothenburg June 13, 2019

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CAN XL draft information

- This CAN XL information is preliminary.
 - Next meeting is in late September 2019
 - This meeting will be open for opinion to the solution as presented here.
 - The necessary CRC length is under investigation



CAN XL Provide:

- More data in each CAN-frame.
 - 1 to 2048 Byte.
- Increased bit-rate during the data section.
- Better protection for faults
- Better prepared for future generations of CAN



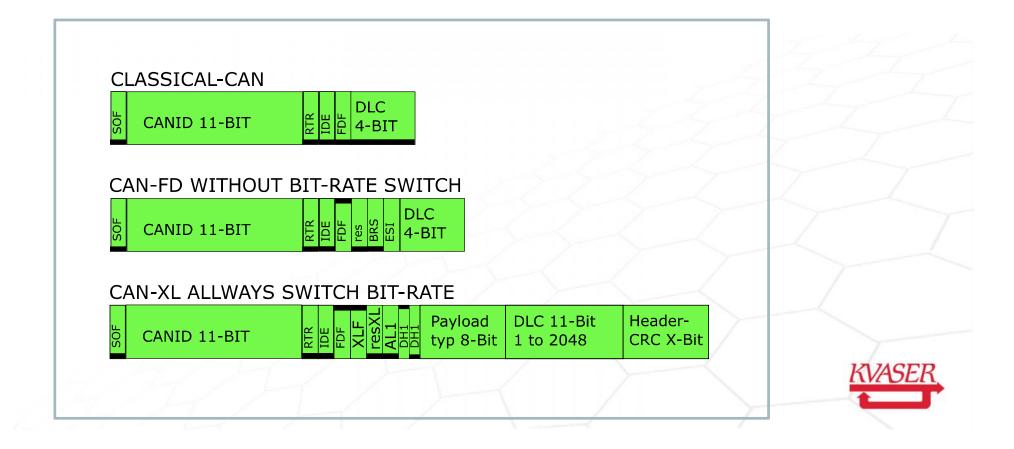
CAN compared to CAN FD

	DLC 4-BIT DATA BYTE 1		DATA BYTE 4 DATA	A BYTE 5 DATA BYTE 6	DATA BYTE 7 DATA	A BYTE 8 CRC15-(15+S) BI	TS BY EOF 7-BITS BEEN	
N-FD WITHOUT BIT-RATE	SWITCH							
CANID 11-BIT 플립	DLC 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	YTE 1 DATA BYTE 2 DATA E	YTE 3 DATA BYTE 4	DATA BYTE 5 DATA BY	TE 6 DATA BYTE 7	DATA BYTE 8 CRC17-27	BITS INCLUDING STUFF-BITS AND SCNT	요 성상 성상 EOF 7-BITS 된 문
AN-FD WITH BIT-RATE SWI	DLC	2 DATA BYTE 3 DATA BYTE 4 DATA BYTE 5 DATA BYTE 6	DATA BYTE 7 DATA BYTE 8 CRC17-27 I	BITS INCLUDING STUFF-BITS AND SCIVE	EOF 7-BITS			
N-FD WITH BIT-RATE SWI	N.	JAGANES JARANES JARANES JARANES ALCONVERSIALAINESTARESKALSIN		1	22			

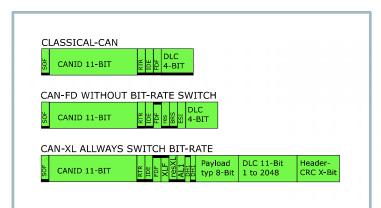
- First frame is Classical CAN frame with 8 Byte of data.
- Second frame is CAN FD without bit-rate switch is longer due to more overhead.
- Third frame is CAN FD with data section at double bit-rate.
- Fourth frame is CAN FD with data section at quadruple bit-rate.



CAN, CAN FD, CAN XL Header part



CAN Header bits



- SOF and 11 bit CANID is common for all generations of CAN.
- Black line in top indicate Recessive and in bottom indicate Dominant bit
- RTR remote request is not supported in CAN-FD and CAN-XL, always Dominant
- IDE identifier extension (29-bit CANID) is not supported in CANXL, always Dominant



CAN FD header bits

CLASSICAL-CAN	
ក្ល CANID 11-BIT	
CAN-FD WITHOUT	BIT-RATE SWITCH
ក្តុំ CANID 11-BIT	
CAN-XL ALLWAYS	SWITCH BIT-RATE

- FDF is in Classical CAN reserved and always Dominant.
- An Recessive FDF-bit indicate FD, XL or future protocols.
- The following res-bit is always Dominant in FD.
- In the XL-format is this the same bit the XLF-bit indicated by Recessive
- A Recessive BRS-bit (Bit Rate Switch), will cause a increased bit-rate.
- The ESI-bit is normally Dominant but will become Recessive when Error Passive

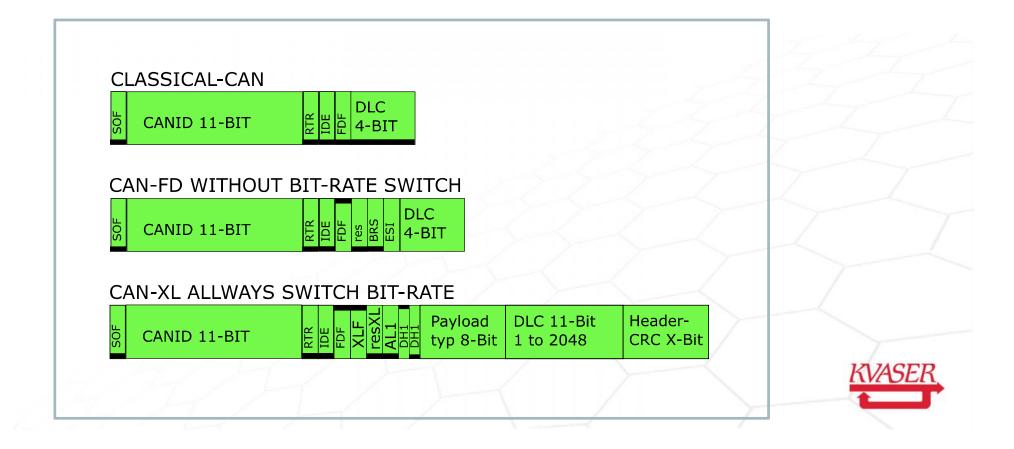


CAN DLC coding

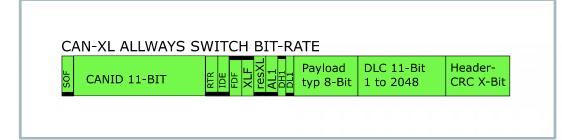
DLC	CAN	CAN FD	CAN XL	Ţ.
0-8	0-8	0-8	1-9	
9	8	12	10	
10	8	16	11	
11	8	20	12	
12	8	24	13	
13	8	32	14	
14	8	48	15	
15	8	64	16	
16 -2047			17 2048	



CAN, CAN FD, CAN XL Header part



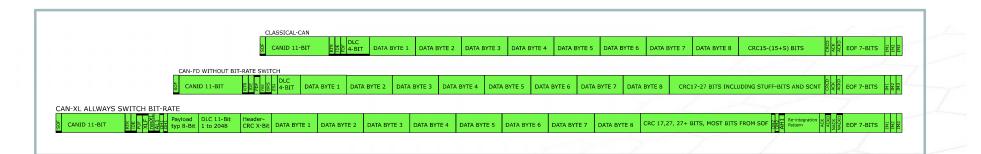
CAN XL header bits



- resXL is Recessive which could be used Dominant for future extension
- AL1, DH1 and DL1 is the new bit-rate switch sequence.
- The XL BRS is complex signaling between CAN-controller an CAN-driver
- Payload 8-bit, is a predefined multiplexer for different data packages
- DLC is a 11-bit integer, where number of data bytes is this integer plus 1
- Header-CRC is to secure correct DLC, which define where data CRC start



CAN frame trailing bits



- CAN FD increased the number of overhead bits compared to Classical CAN
- CAN XL will add even more overhead bits compared to CAN FD
- Those additional bits are located in the header and in the frame ending.
- Most of the overhead in the ending is the CRC that must increase to keep the protection over more bytes



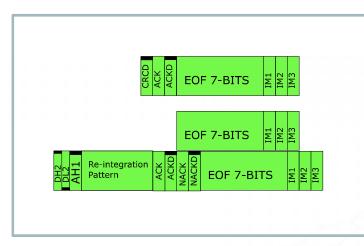
CAN trailing bits

	CRC15-(15+S) BITS	
CRC17-27 BITS INCL	UDING STUFF-BITS AND SCM	
CRC 17,27, 27+ BITS, MOST BITS		

- The only different between Classical CAN and CAN FD is the CRC length
- The longer header in CAN XL will probably demand longer CRC for same data length
- CAN XL includes extra bits for bit-rate switch, acknowledgement and forward compatibility



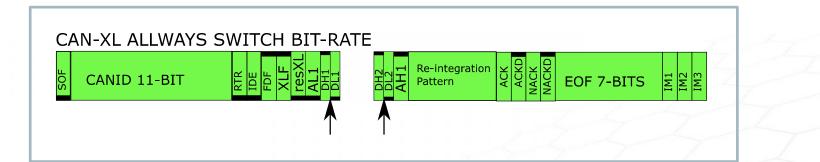
CAN XL trailing bits



- CAN XL CRC is followed with the bit-rate switch pattern and not a CRCdelimiter
- To secure resynchronization to the end of future formats is a reintegration pattern include.
- Added to the old ACK bit it is in CAN XL possible to place an NACK.

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The Bit-rate switch



- The bit-rate increase at the edge between DH1 and DL1
- The bit-rate decrease at the edge between DH2 and DL2
- The AL1 bit includes a special pattern that will switch the CAN-driver into high bit-rate mode.
- The AH bit includes a special pattern that will switch the CAN-driver **away** from high bit-rate mode.



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CAN FD and XL IP:

- Kvaser will provide CAN-XL IP when defined
- Kvaser has a CAN-FD IP.
- The CAN FD IP is sold By Synective Labs.
- The CAN FD IP is used by:
 - Microchip, in the PIC and stand alone CAN-controllers
 - Support for Xilinx, Intel, MicroSemi, Lattice FPGA.



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Thank You! QUESTIONS?