CCSDS Lossless Compresstion IP-CoreSpace applications

The use of multispectral and hyperspectral sensors on unmanned vehicles such as drones or satellites is spreading nowadays. The information acquired by this kind of sensors has multiple applications in the fields of surveillance, recognition and navigation, among others. Nevertheless, these sensors generate vast amounts of data, which need to be processed, stored and transmitted. The data transmission bandwidths are currently stable and, compared with the size of multispectral and hyperspectral images may constitute a bottleneck when transmitting the information to a ground station. On the other hand, the limited hardware resources available on board the systems operating the aforementioned applications restrict their computational power as well as their storage capabilities. These problems may be aggravated in the near future with the progressive increase in the resolution of these sensors. Therefore, applying on board compression techniques becomes mandatory for those missions which include multispectral or hyperspectral sensors.

With this goal, the Consultative Committee for Space Data Systems (CCSDS) has developed several lossless data compression standards specifically designed for space applications. These standards provide efficient compression together with a reduced complexity, which fits well with the limited computational resources available in space systems. Among these standards, the CCSDS-121 constitutes a universal compressor, while the CCSDS-123 specifically targets multispectral and hyperspectral images. Both compression standards make use of predictive pre-processing stages, well suited for low complexity implementations.

Currently, the European Space Agency (ESA) provides a portfolio of IP cores intended for future space missions. This IP core portfolio has recently included two IP cores, which consist in hardware implementations of the CCSDS 121 and 123 compression standards respectively, which are known together as SHyLoC. These IP cores are provided as technology independent, configurable and synthesizable VHDL designs and they are capable of working separately as well as jointly. However, the SHyLoC IP cores are not fully compliant with the CCSDS lossless compression standards. On the one hand, the CCSDS-121 IP does not implement the pre-processing stage defined in the CCSDS-121 standard. On the other hand, the external communications of the CCSDS-123 IP require an improvement in order to increase its throughput.

This work presents the modifications proposed over the SHyLoC IP cores in order to implement additional features of the CCSDS lossless compression standards, while at the same time achieving higher performance in terms of compression efficiency and throughput. These result in a new version of the SHyLoC IP cores, known as SHyLoC-e. On the one hand, the main feature of the ShyLoC-e 121 IP is the inclusion of the unit-delay predictor defined in the standard, which additionally requires inserting reference samples in the compressed data. On the other hand, the throughput of the ShyLoC 123 IP is improved in the Band-Interleaved (BI) architectures by optimizing the communications between the IP and the external memory where the intermediate residuals are stored, optimizing the use of the AHB bus. In addition, modifications in order to implement the custom weight initialization defined in the CCSDS-123 standard are proposed. This project has been supported by ESA as an extension of the TRP-AO8032 contract.