COMPACT RECONFIGURABLE AVIONICS – RECONFIGURABLE DATA HANDLING CORE

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ABSTRACT

Cobham Gaisler has developed a reconfigurable platform under European Space Agency (ESA) contract 4000121650/17/NL/LF. The main objective of the activity was to design and manufacture a reconfigurable platform hosting a high performance microprocessor and high capacity reconfigurable FPGA(s). The platform consists of three major modules providing the necessary processing power and the capability to interface with sensors and actuators. One of the modules has been developed as an Elegant Bread Board (EBB) consisting of the GR740 Quad-Core LEON4FT SPARC V8 processor along with the BRAVE NG-Medium FPGA which can be reconfigured using SpaceWire. The activity includes development of boot SW and also system SW for the EBB, supporting low level processor to companion FPGA communication as well as communication interfaces towards external sensors and actuators.

INTRODUCTION

The Compact Reconfigurable Avionics (CORA) is a set of three ESA activities having the technical focus for each activity respectively in Software (Model Based Avionics design – MBAD), Data Handling (Reconfigurable Data Handling Core – RDHC) and AOCS (Smart AOCS & GNC Elements – SAGE).

The Reconfigurable Data Handling Core (RDHC) is the execution platform for the CORA. Cobham Gaisler AB (Sweden) is the prime for the activity and responsible for the VHDL design and HW/SW deliverables. The work has been performed along with Airbus Defence & Space (France) contributing to the systems analysis and trade-off, requirements and system architecture, Thales Alenia Space (France) responsible for middleware software design and Thales Alenia Space España S.A. (Spain) responsible for FPGA reconfiguration code and HW/SW validation.

HARDWARE

The RDHC platform consists of the three major modules: the Elegant Bread Board (EBB), the DIGANIF (Digital and Analogue Interfaces) and the SPWIF (SpaceWire Interfaces) boards. The system hardware architecture is based on OpenVPX (ANSI/VITA 65) and the modules are designed with SpaceVPX (ANSI/VITA 78) compatibility in mind. Each of these modules occupy a single slot on the backplane and the modules' design are prepared for modular redundancy.

The complete RDHC System is illustrated in the block diagram below.

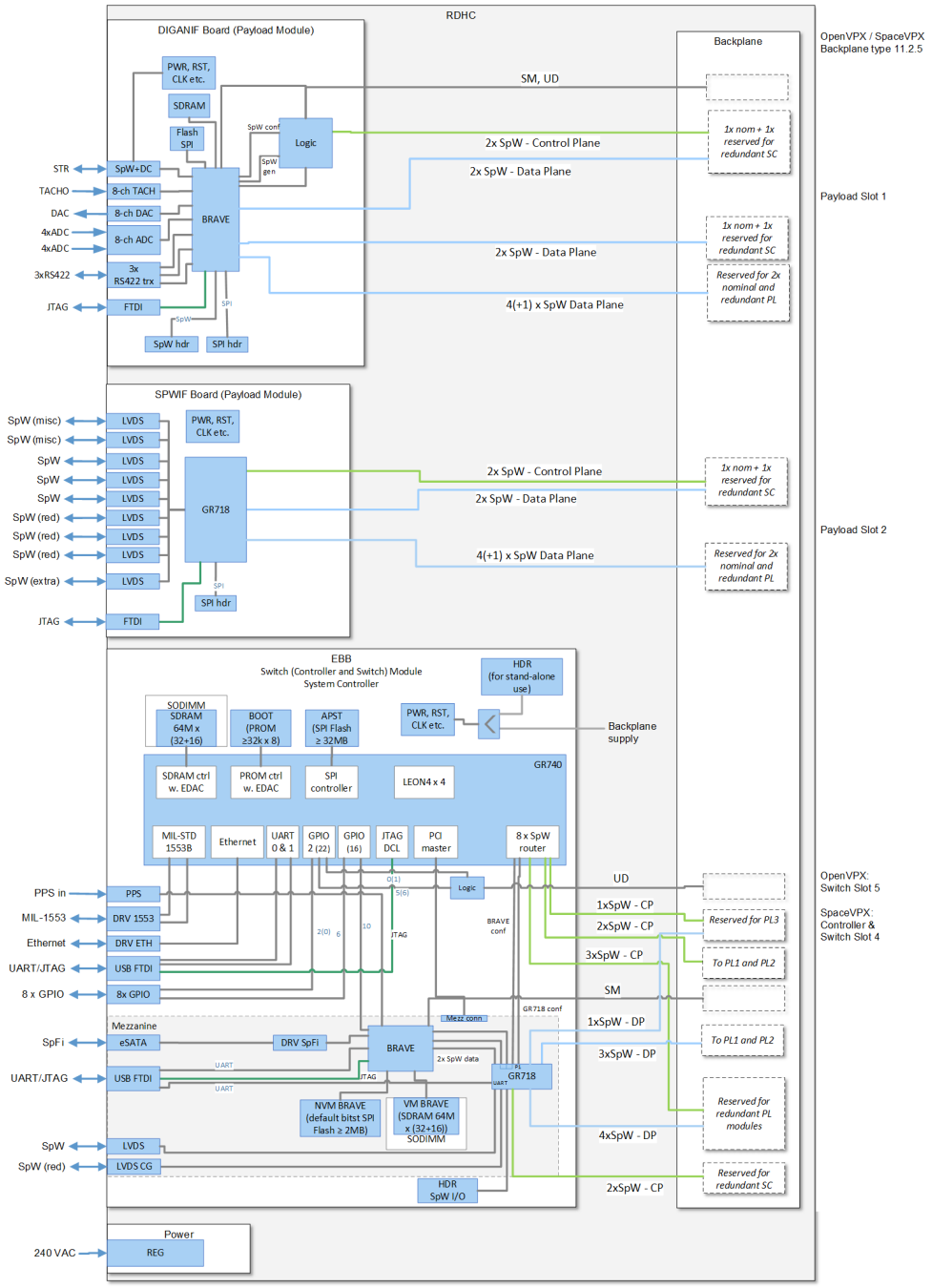

Fig. 1. CORA-RDHC Block Diagram

In the figure the top two boards (DIGANIF and SPWIF) represent payload modules in the OpenVPX terminology. The EBB is according to the OpenVPX terminology a switch module and will also act as system controller. The modules developed have been functionally verified and validated in an OpenVPX system. In order to reduce cost, complexity and lead-time of the RDHC the OpenVPX standard has been used, but with a fairly short path to a SpaceVPX platform.

SOFTWARE

The software packages developed as part of the activity are described below,

Boot software

The RDHC requirements include software compatibility with the ESA SAVOIR Flight Computer Initialisation Sequence Generic Specification. It is developed as two independent units.

The Initialisation sequence is responsible for taking the GR740 from a system reset state to the execution of application software. It configures GR740 peripherals, performs self-tests on memories. The results are written to a boot report which is available to the application. Application can be loaded from an SPI flash memory located on an external SPI bus.

FPGA reconfiguration

The BRAVE NG-Medium FPGAs available in both the modules (EBB and DIGANIF) are designed to be reconfigurable through SpaceWire, as defined in the bit streams stored at the SPI flash connected to GR740. In the activity SpaceWire reconfiguration has only been applied for the EBB. An FPGA reconfiguration software library is developed to implement the BRAVE SpaceWire configuration protocol. In addition to the configuration operation, it will also monitor dedicated FPGA status signals so that the GR740 software can take appropriate actions on FPGA events.

Middleware

The Middleware layer provides the application with an abstraction suitable for RDHC operation. This includes among other things configuration of the SpaceWire router, GPIO and SPI flash management. Middleware also provides a PUS terminal operating on SpaceWire. PUS services are provided for managing on-board memory and to perform system specific operations, such as reconfiguring the FPGA.

Execution environment

The intended operating system for application executing on the RDHC system GR740 is RTEMS-5.1 SMP [1]. RTEMS provides powerful peripheral drivers for the main communication interfaces. RDHC is SpaceWire centric and so the RTEMS SpaceWire driver, with its zero-copy DMA, is a very good match. An RMAP initiator is designed on top of the this driver. RTEMS SMP is currently being qualified for GR740 in a separate ESA activity.

SUMMARY

The activity consisted of four major work phases (system definition, design, manufacturing, test and installation). All phases except the final installation phase have been completed. Installation at ESTEC is currently on-going and is expected to be completed in December 2019.

REFERENCES

[1] RCC User's Manual. Internet: https://www.gaisler.com/anonftp/rcc/doc/rcc-1.3.pdf [November, 2018]