Compact Reconfigurable Avionics – Reconfigurable Data Handling Core CoRA-RDHC

TEC-ED & TEC-SW Final Presentation Days 3-4 December 2019

Presenter: Arne Samuelsson, Cobham Gaisler

Agenda

Overview of the CORA-RDHC activity
System design and COTS BB
RDHC design
RDHC hardware
VHDL design
Software
Experiences
Summary

COBHAM

Overview of the CORA-RDHC activity

System design and COTS BB

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RDHC hardware

VHDL design

Software

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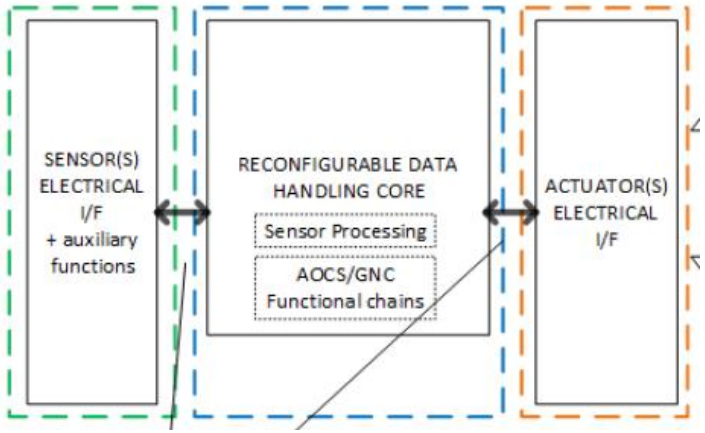
Objectives
Summary

- Development of an Elegant Bread Board
  - A compact reconfigurable datahandling core module
  - High performance microprocessor and high capacity reconfigurable FPGAs
  - Clear path to space qualification
  - Accompanied by I/O interface modules
- Delivery of a SW development platform
  - Bread Board based on COTS
  - Identify, procure and make available to the parallel activities by PDR
- Development of Board Support Package
  - FPGA communication and reconfiguration
  - Communication interfaces towards external sensors and actuators
- Development of Boot SW
- Installation of the compact reconfigurable avionics testbed at the ESTEC Avionics laborator



Organization

- ESA
  - Technical Officer: Jørgen Ilstad, TEC-EDD –> EOP-PPE
- Cobham Gaisler AB, Sweden (prime)
  - Responsible for the development of hardware, VHDL design, boot software and drivers
- Thales Alenia Space France
  - Responsible for middleware software design
- Thales Alenia Space España S.A., Spain
  - Responsible for FPGA reconfiguration code
- Airbus Defence & Space, France
  - Contribution to the systems analysis and trade-off, requirements and system architecture
- External service providers
  - Responsible for breadboard development

Overview of the CORA-RDHC activity
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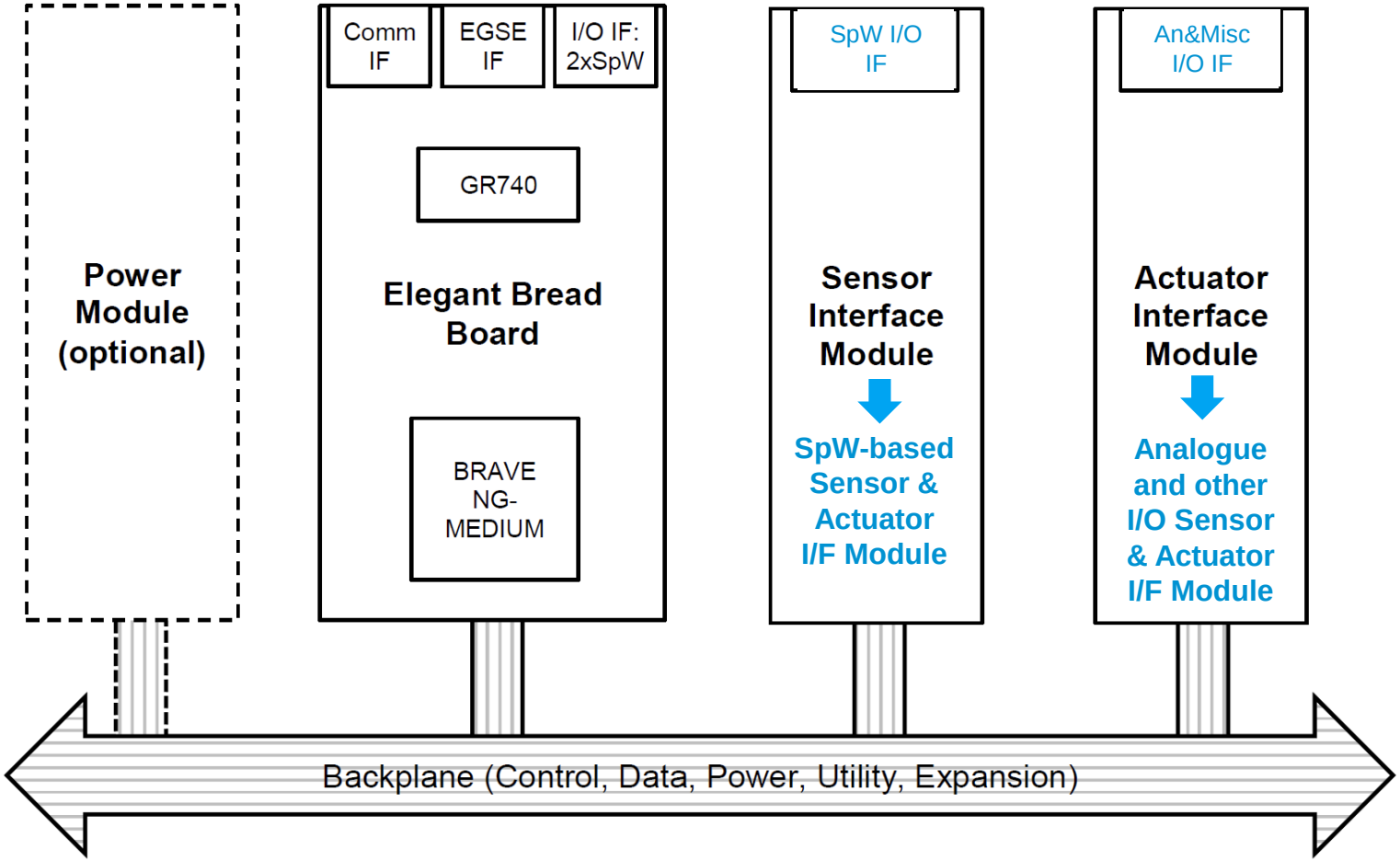
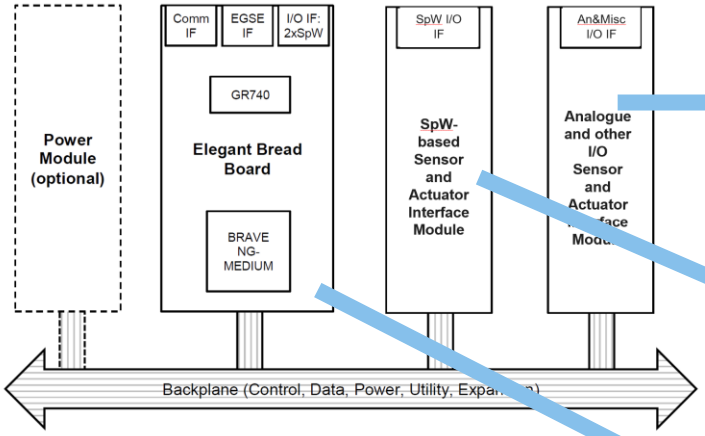
Prerequisites
Summary

- GR740 Quad-Core LEON4 SPARC V8 Processor
  - Controller and high-performance processing
- FPGA BRAVE NG-Medium
  - European, existing, SpW-reconfigurable
- Common form factor
  - EBB and I/O modules
- I/O interfaces to be consolidated with the CORA-SAGE activity
- SW platform to be consolidated with the CORA-MBAD activity

Concept
After CORA interface consolidation



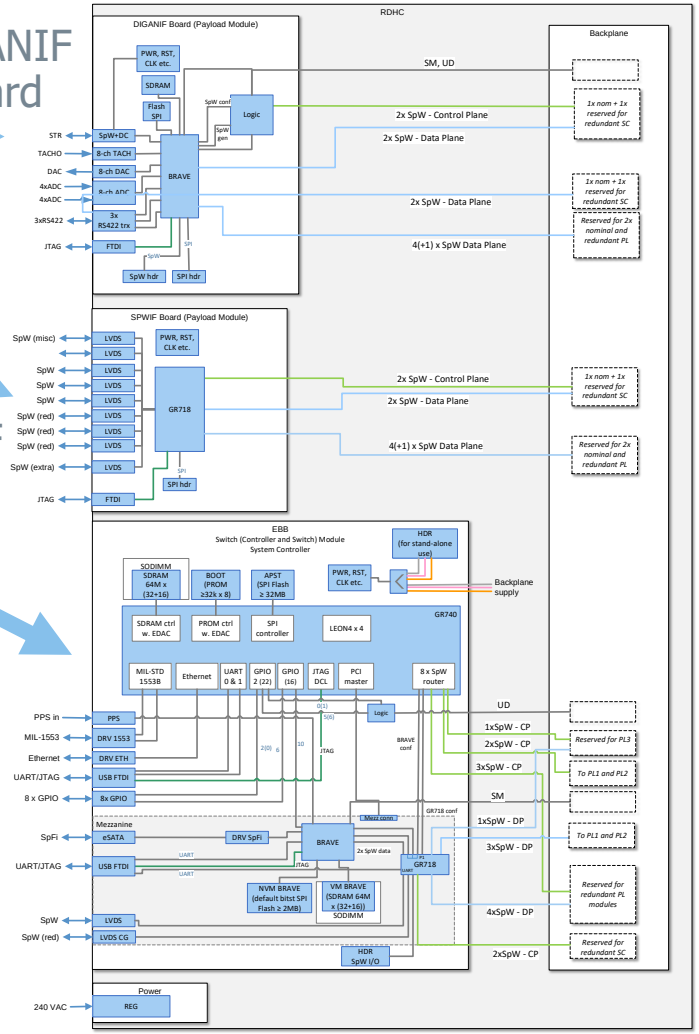
System design
For COTS BB and final RDHC



DIGANIF board

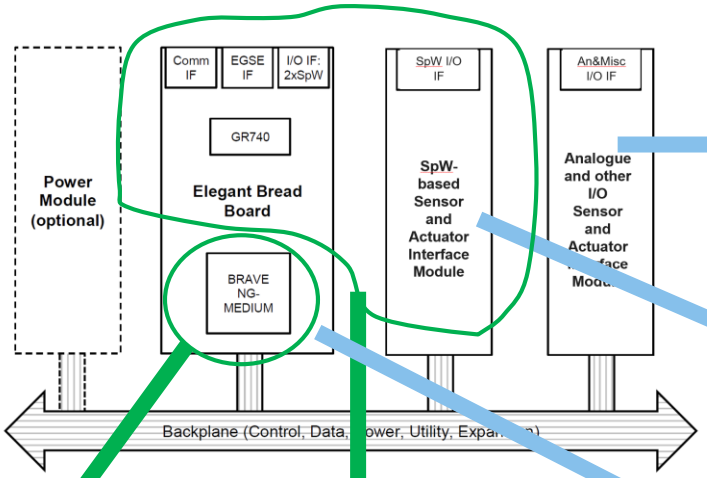
SPWIF board

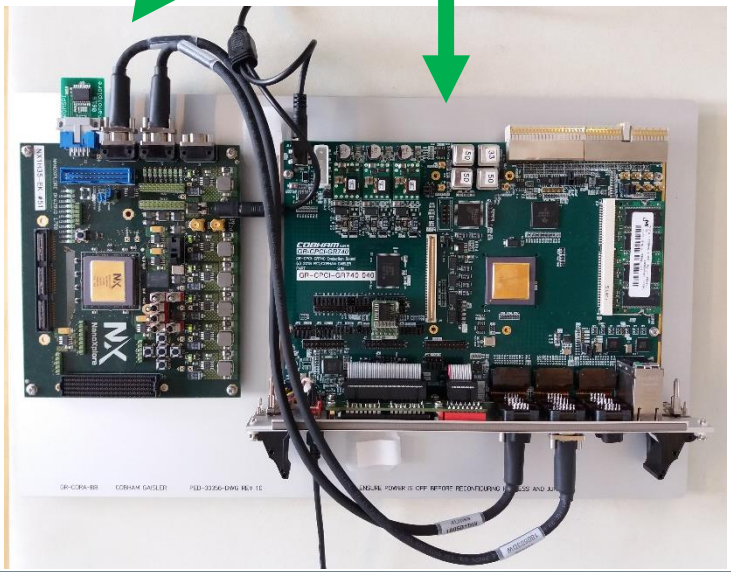
EBB (Elegant Bread Board)

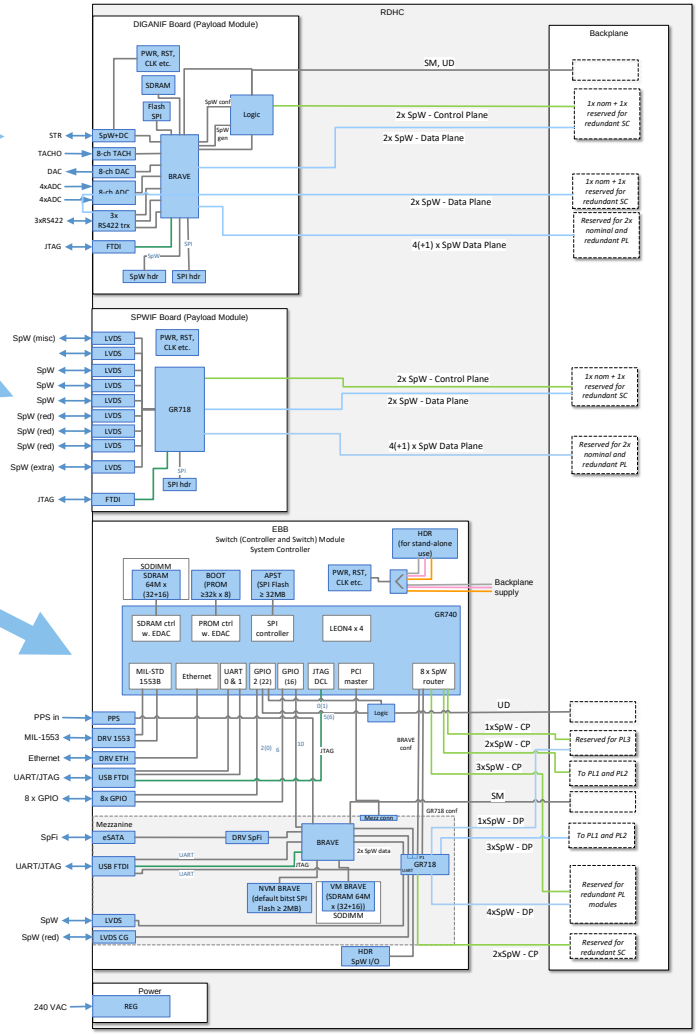


Detailed block diagram provided on slides to follow

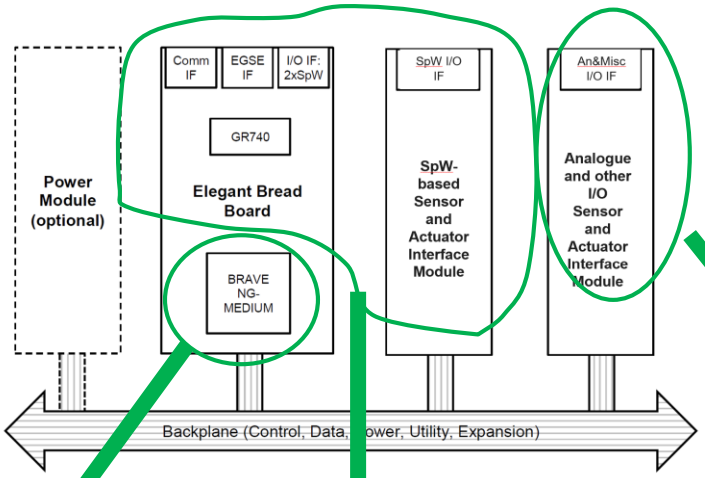
System design
For COTS BB – GR-CPCI-GR740 and NX1H35S-EK



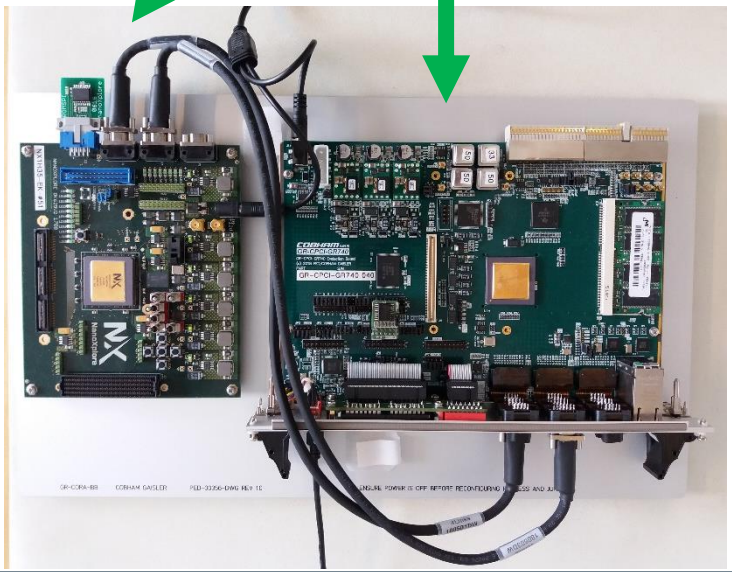




System design
For COTS BB – with DIGANIF Light



- Enables testing of Analogue and other I/O Interfaces for SAGE
- Developed prior to final RDHC
- Mezzanine for BRAVE Evaluation Kit



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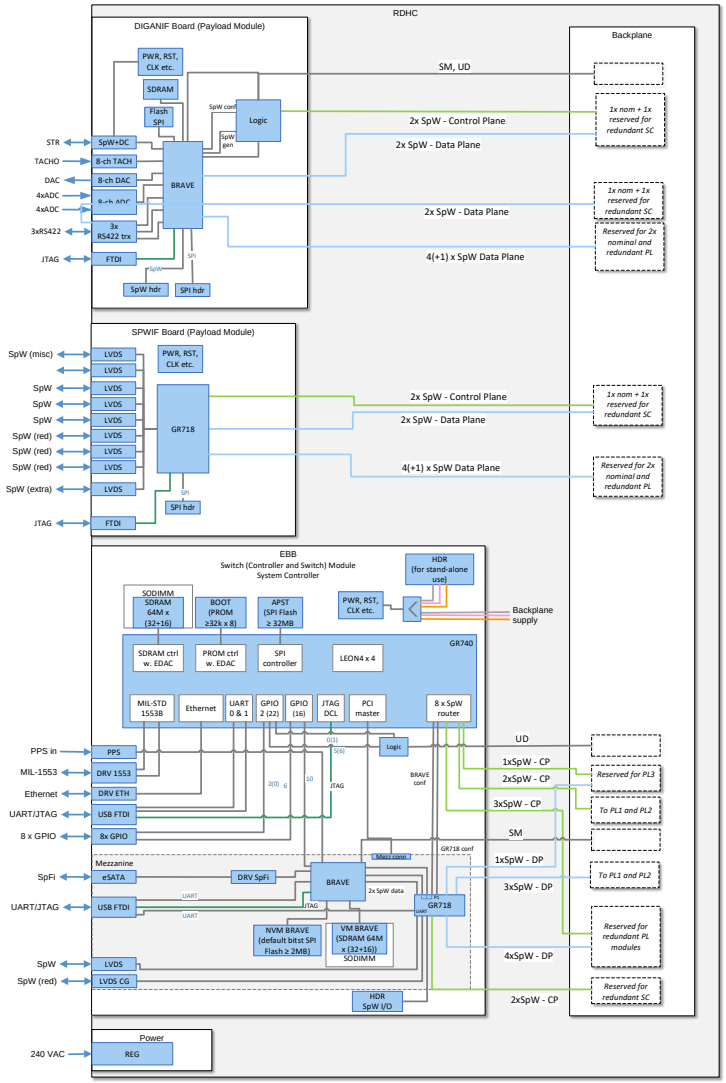
RDHC design
From Block diagram to Detailed Design



Many design iterations in areas of:

- Form factor
  - OpenVPX, VITA 65 (3U, 6U)
  - SpaceVPX, VITA 78.0 (3U, 6U)
  - SpaceVPXLite, VITA 78.1 (3U)
  - Others
- I/O interfaces
  - Specifications
  - Adaptations to SAGE activity
- Redundancy concepts
  - Backplane profile
  - Board designs
- Reconfiguration options
  - On-board and between boards
- Design support for future
  - Flight parts
  - Backplane profiles

RDHC design
Major design decisions

COBHAM

- Form factor - VPX 6U selected
  - Front-panel interfaces dimensions
    - Driven by large connectors used in space applications
    - Lots of I/O distributed externally to the unit, is generally required for most applications
  - The need for power condition circuitry for many power supply rails coupled with lack of small footprint space qualified components
  - Additional PCB real-estate to achieve fault tolerant designs
  - Thermal design constraints drive module size to be become large
  - Thus 3U module size is inadequate to meet the above-mentioned design drivers

RDHC design
Form factor

- OpenVPX 6U selected
  - COTS backplanes availability
- Backplane profile 11.2.5
  - Centralized Data Plane
  - Similar SpaceVPX Backplane Profiles
- EBB
  - For Switch Slots
- I/O Modules
  - For Payload Slots

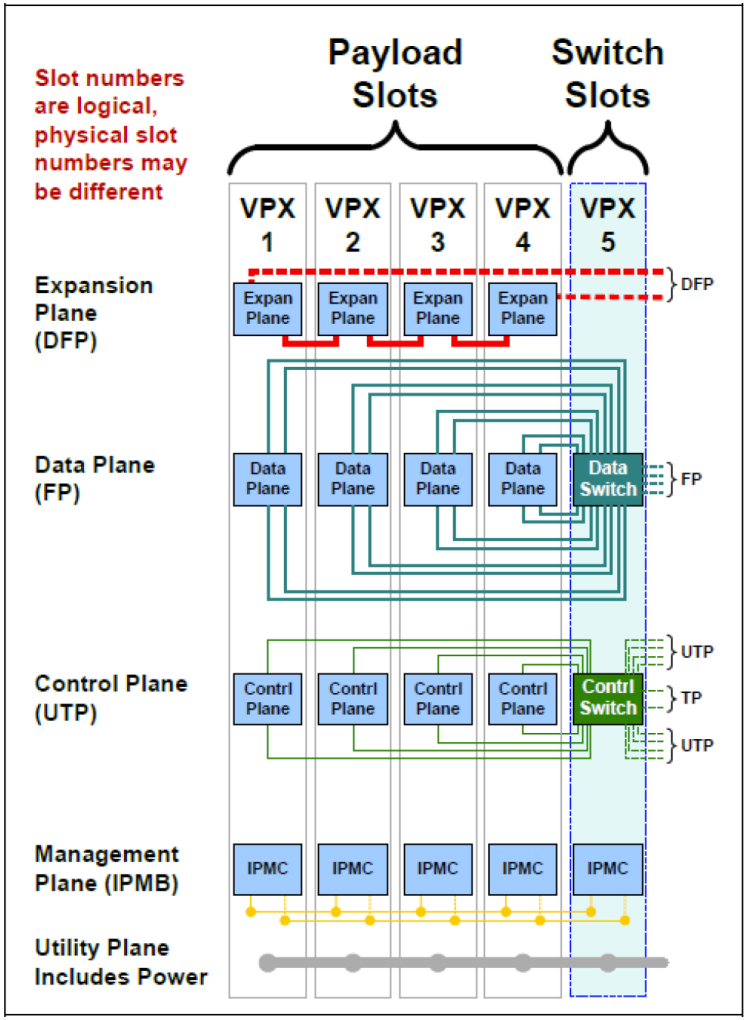


Figure 11.2.5-1 Topology of BKP6-CEN05-11.2.5-n

RDHC design
Form factor – forward compatibility

- SpaceVPX Backplane Profile 11.2.5
- EBB
  - Controller & Switch Slot
  - Factory-configuration needed
- I/O Modules
  - Payload Slots
  - Factory-configuration needed
- Designed to support redundant pairs
- No testing in the CORA activity
- Non-compliance: SpW used in Data Plane
  - Mainly driven by the lack of support for high speed serial links in the selected FPGA technology (BRAVE NG-Medium)
- Upgrade of the EBB FMC mezzanine will allow full compliance to the VITA dataplane in using high speed serial links e.g. SpaceFibre.

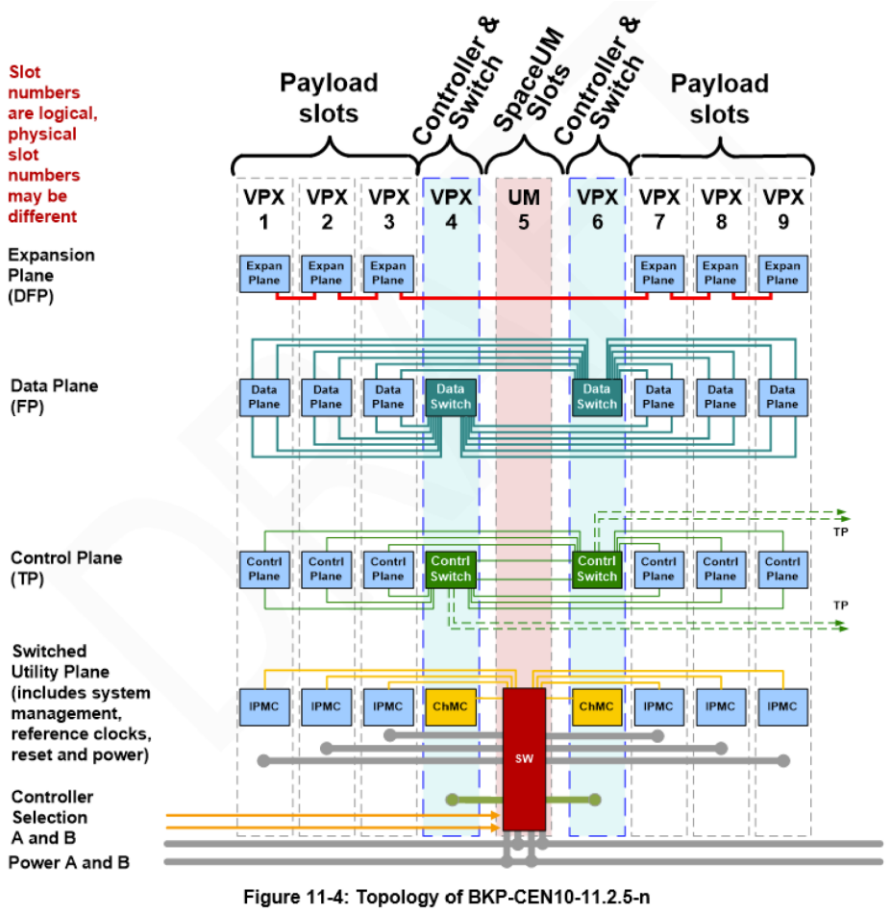
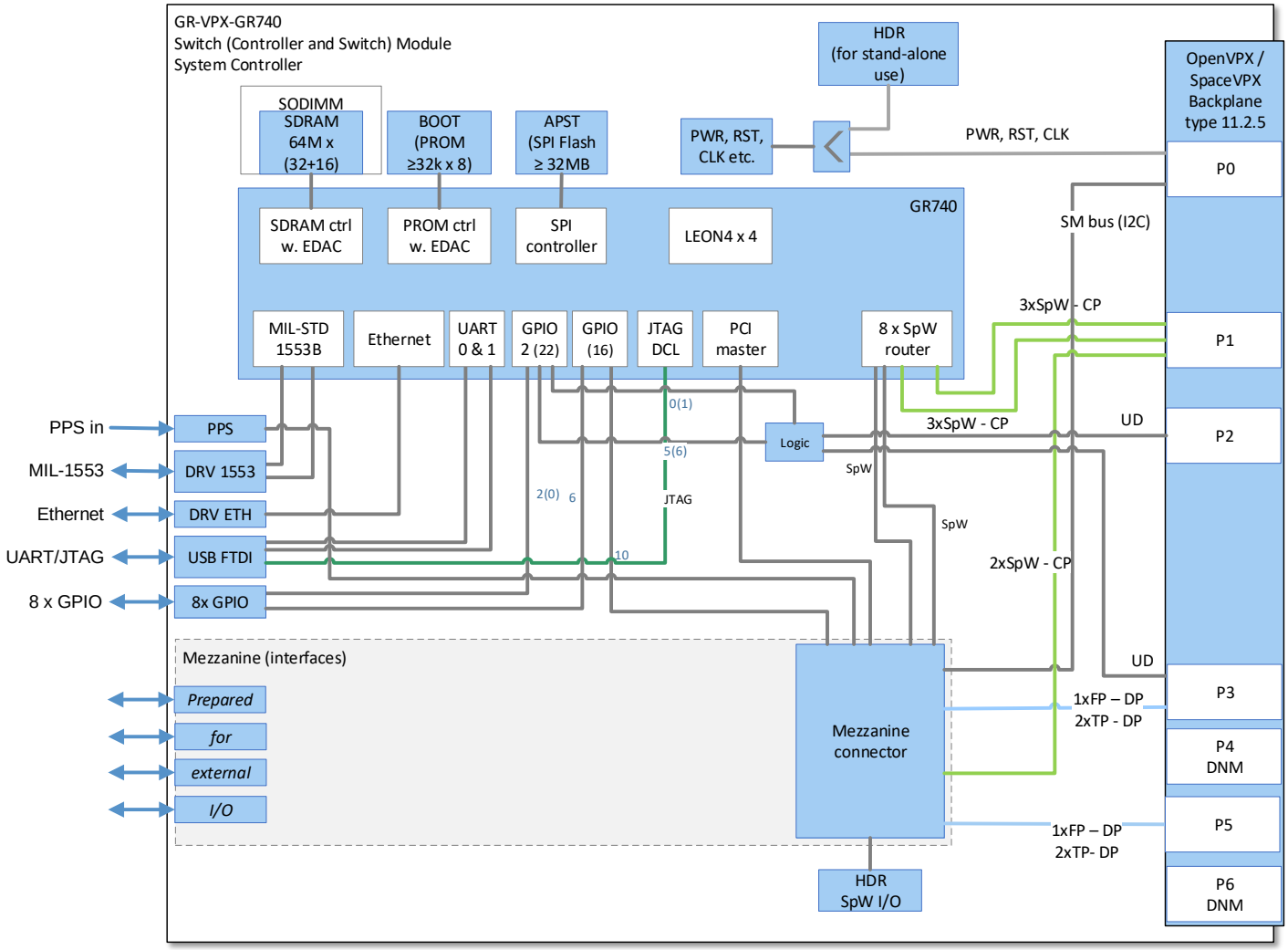


Figure 11-4: Topology of BKP-CEN10-11.2.5-n

RDHC design
EBB design for forward-compatibility

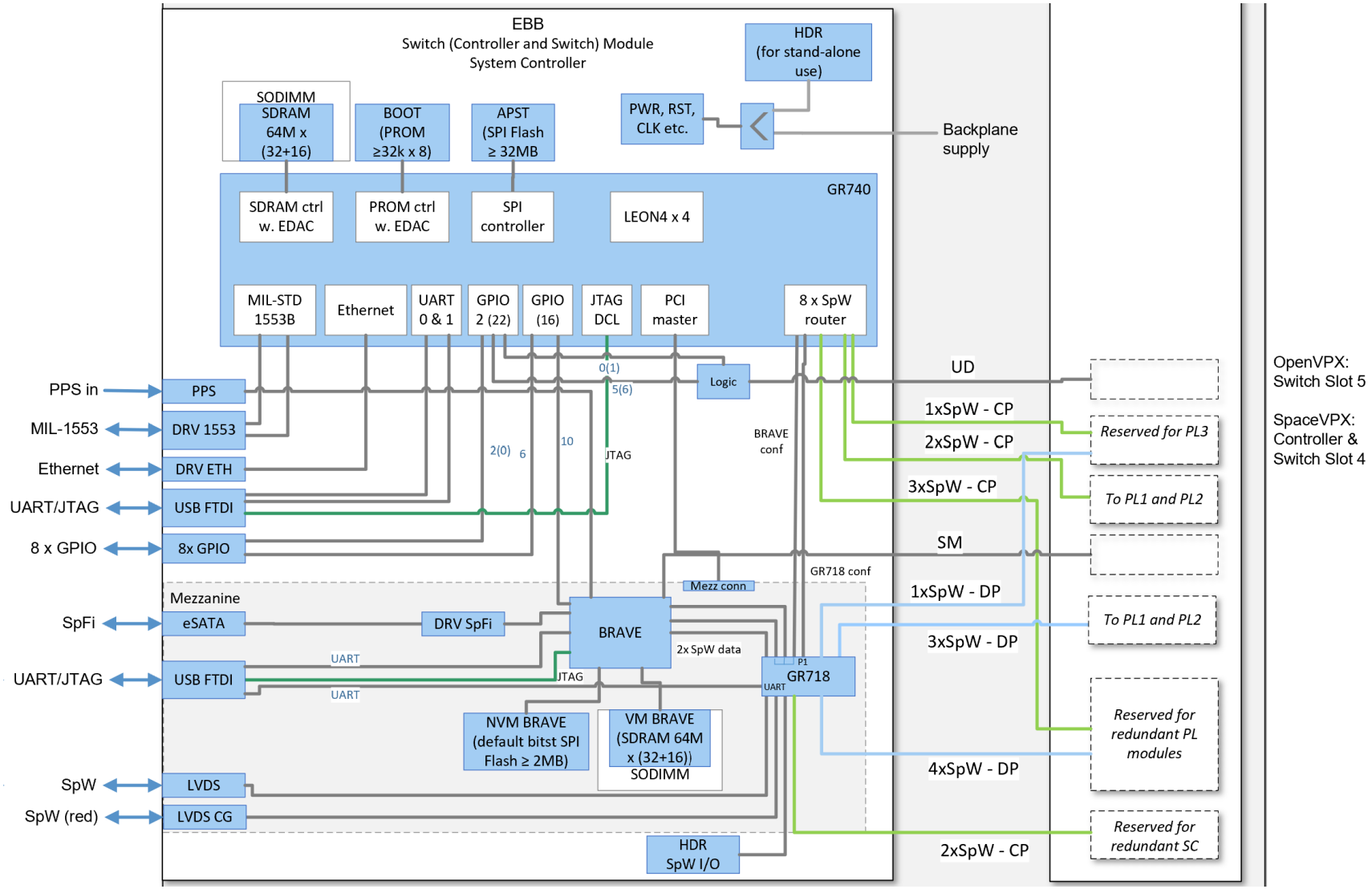
Mezzanine interface supporting Thin Pipes or Fat Pipes for HSSL to Data Plane in the backplane



RDHC design
EBB

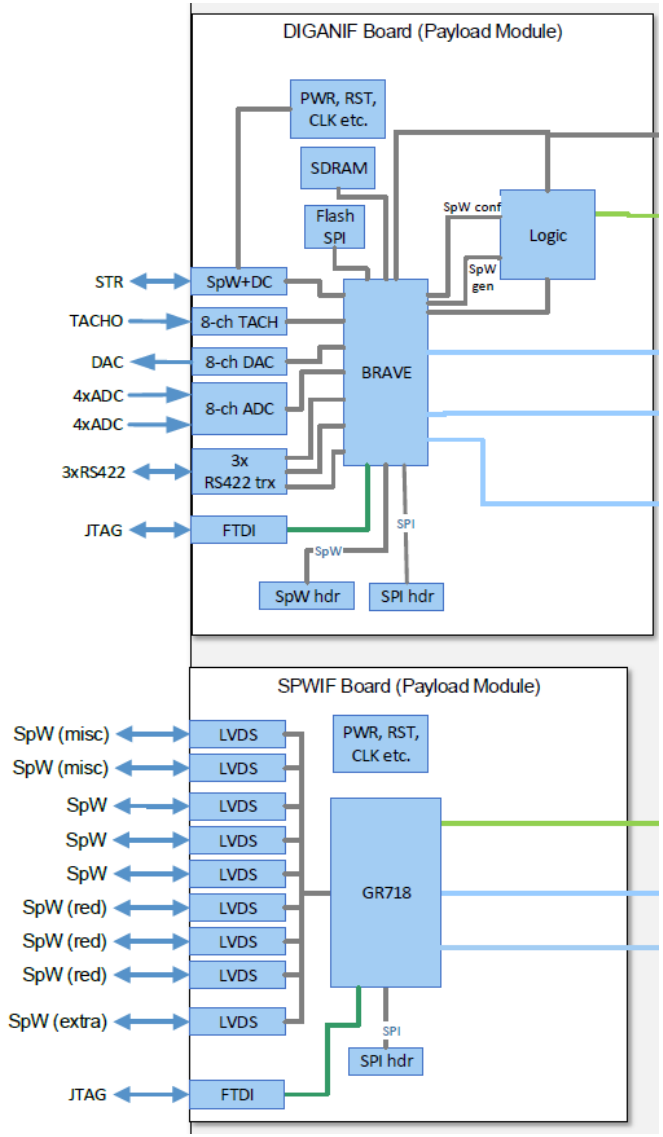
- Interfaces adapted to CORA-SAGE activity
- Supporting redundancy concepts
- Stand-alone or backplane operation
- GR740 on Main Board
- BRAVE NG-MEDIUM and GR718B on Mezzanine
  - For use in CORA
  - SpW-based reconfiguration of FPGA
  - SpFi interface routed in hardware
- Support for future Mezzanine boards
  - PCI from GR740
  - High-performance FPGA
  - SpFi routing to Data Plane
  - SpaceVPX-supported protocols

RDHC design
EBB with BRAVE Medium Mezzanine

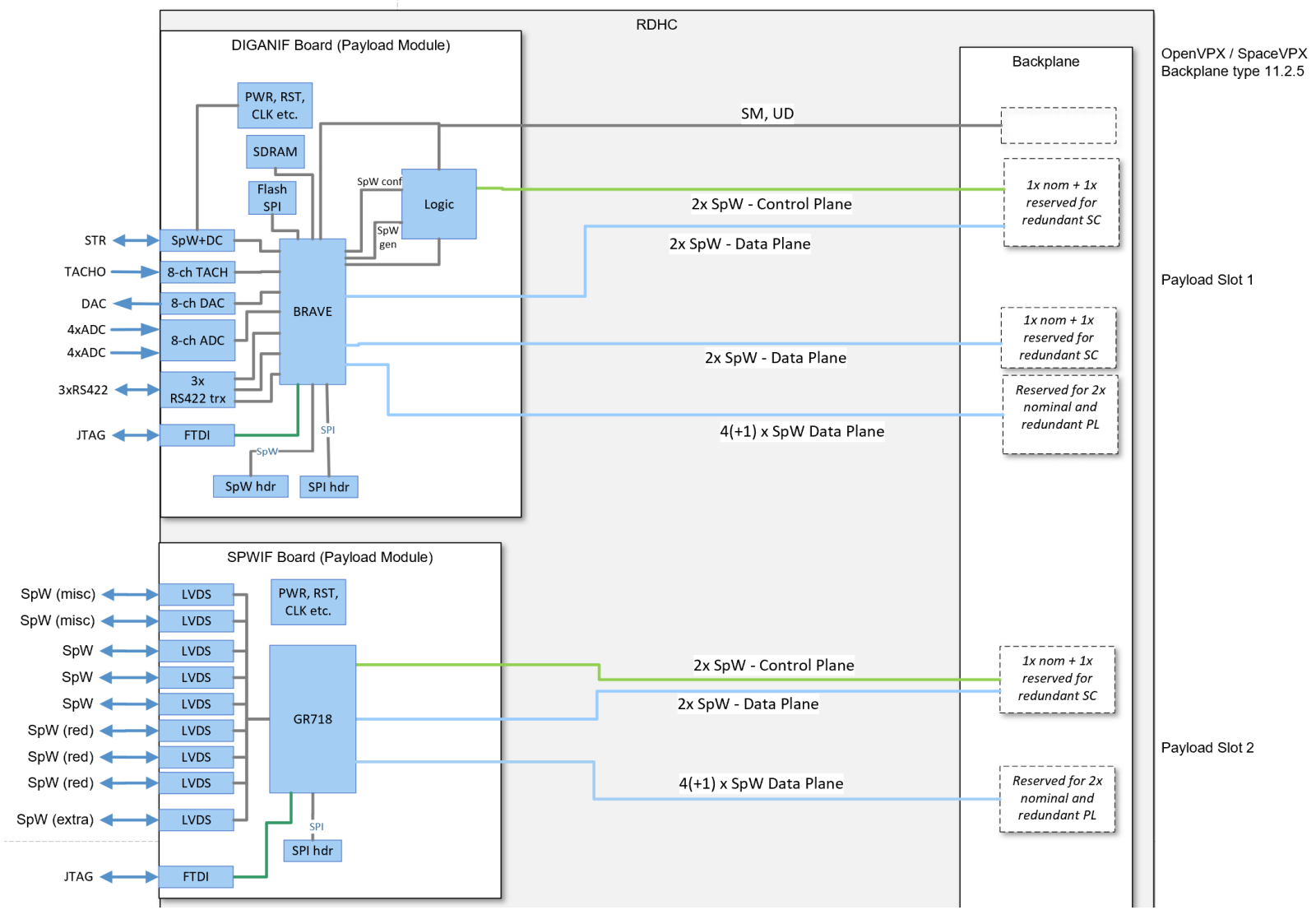


RDHC design
I/O Modules

- Mainly for CORA use
- Interfaces adapted to CORA-SAGE activity
- Supporting SpW-based redundancy concepts
- Stand-alone or backplane operation
- Limitations: no HSSL in Data Plane, no formal SpaceVPX compliance
- DIGANIF board
  - BRAVE NG-Medium
  - PCB design for SpW reconfiguration
  - SPI bitstream in CORA
- SPWIF board
  - GR718B
  - Mainly a SpW router board
  - Supporting the three redundant pairs of SpW instrument



RDHC design
I/O Modules – backplane interfaces

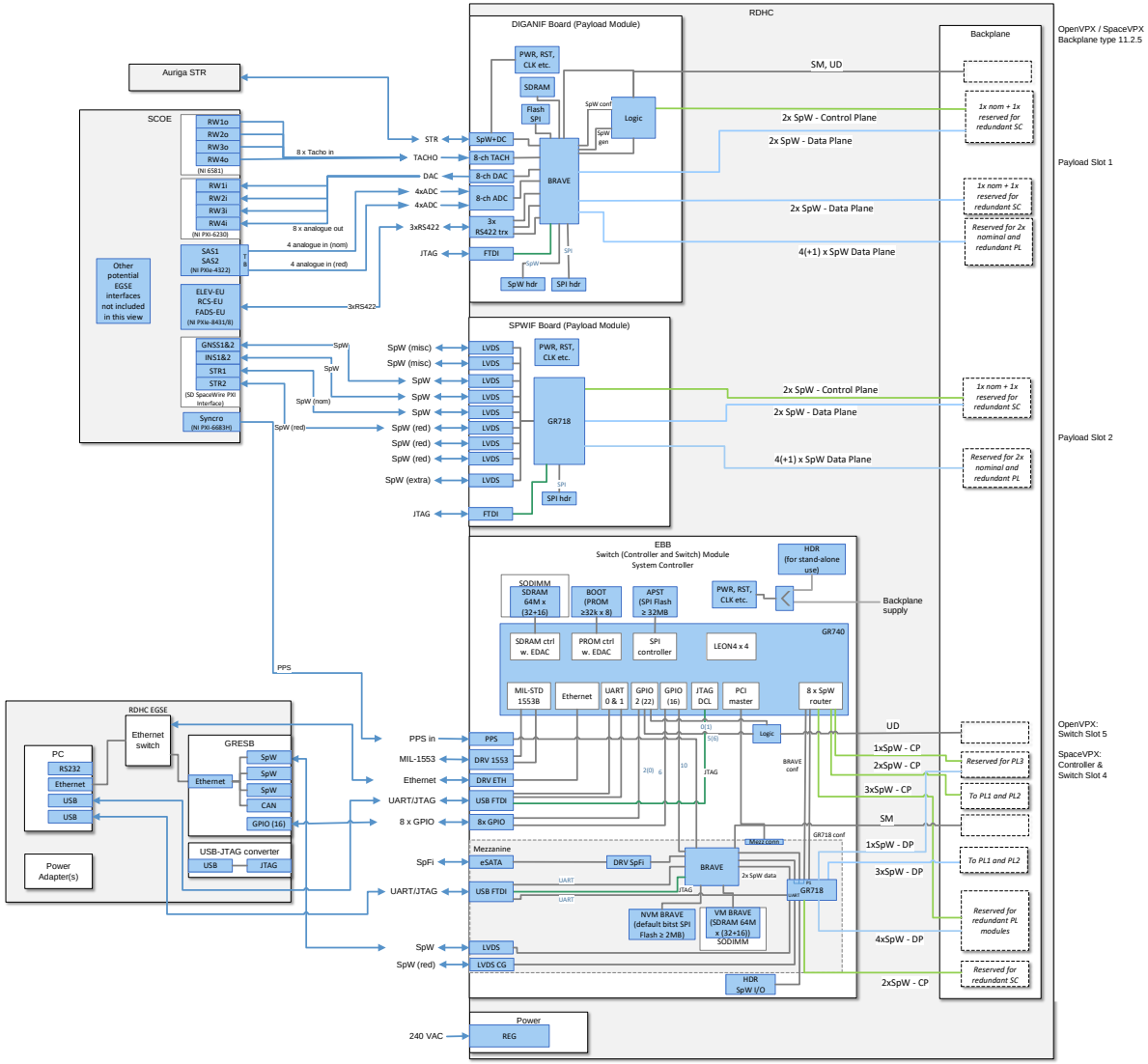


RDHC design

Summary overview - complete CORA hardware system

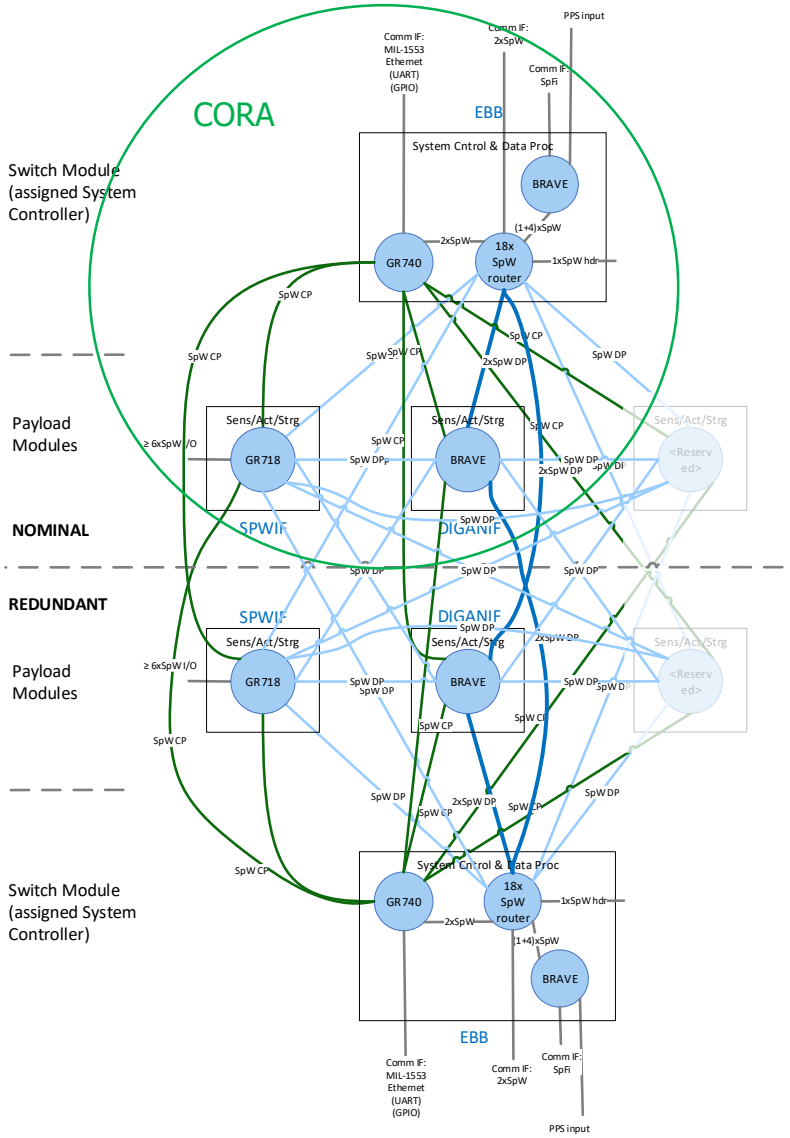
Simulated AOCS units developed by CoRA-SAGE team

EGSE for RDHC control



RDHC design
Module-redundant architecture

- Path-to-flight concept
- Dual-star Control and Data Plane
- PCB design prepared
- EBB supporting SpFi on Data Plane needs updated Mezzanine



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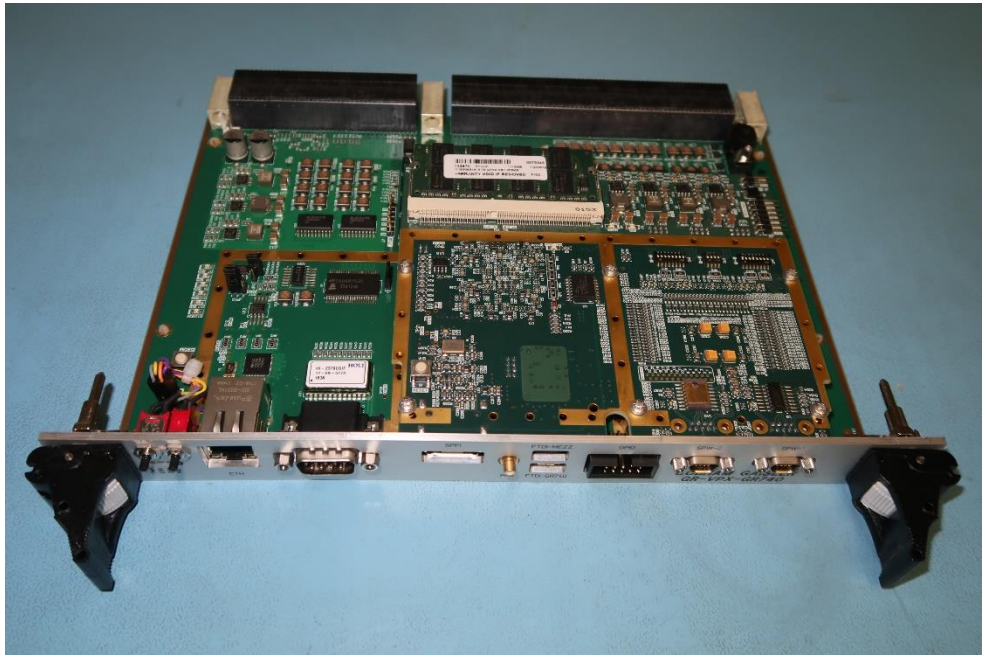
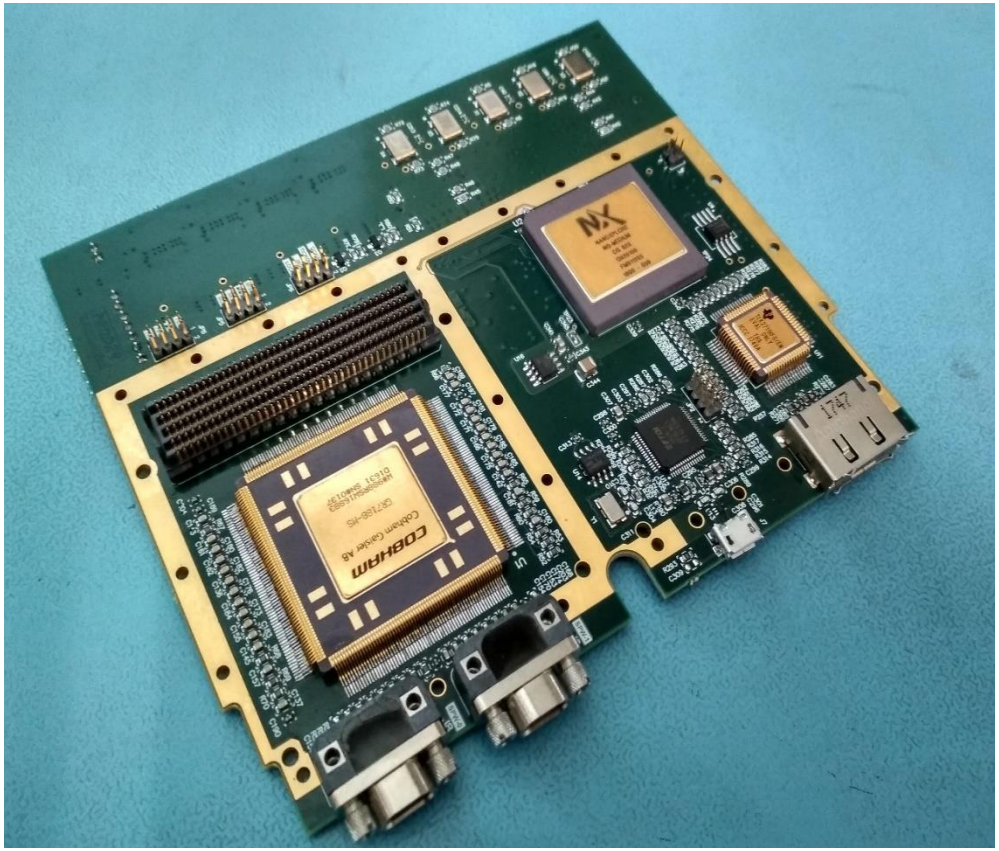
RDHC hardware
EBB – Main Board

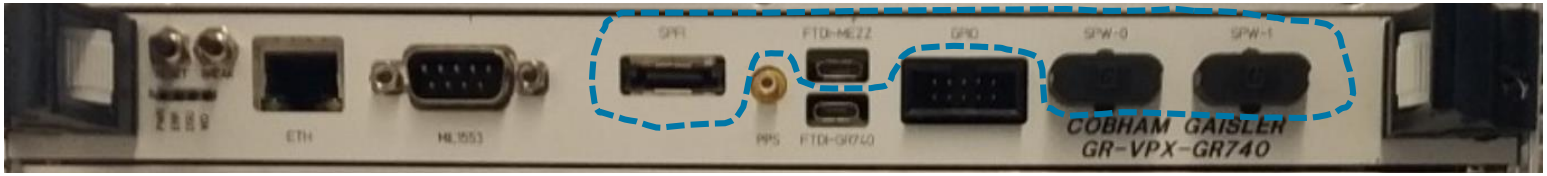
- GR-VPX-GR740
- GR740, SDRAM, SPI Flash
- Illustrated with Mezzanine Board
- Development completed



RDHC hardware
EBB – Mezzanine

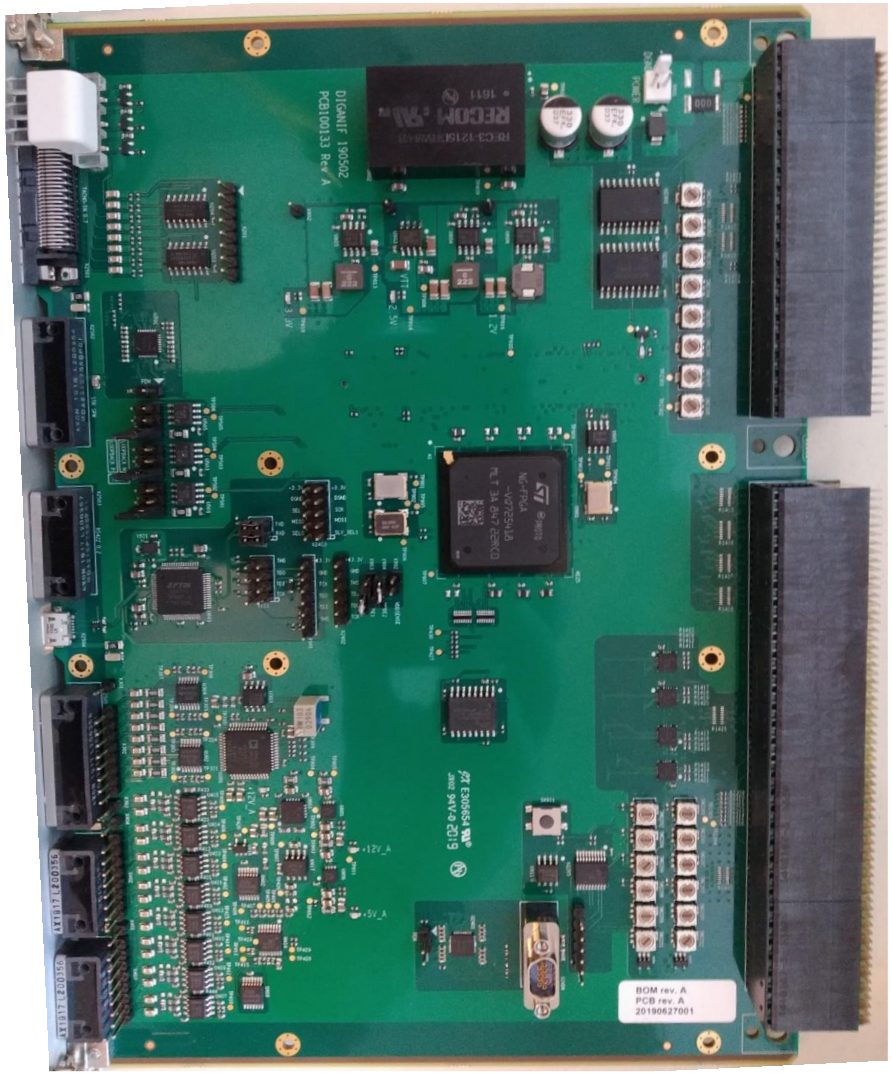
- GR-VPX-BM-MEZZ
- BRAVE NG-Medium (ceramic), GR718, GR54LVDS049, SDRAM, SPI Flash
- Development completed





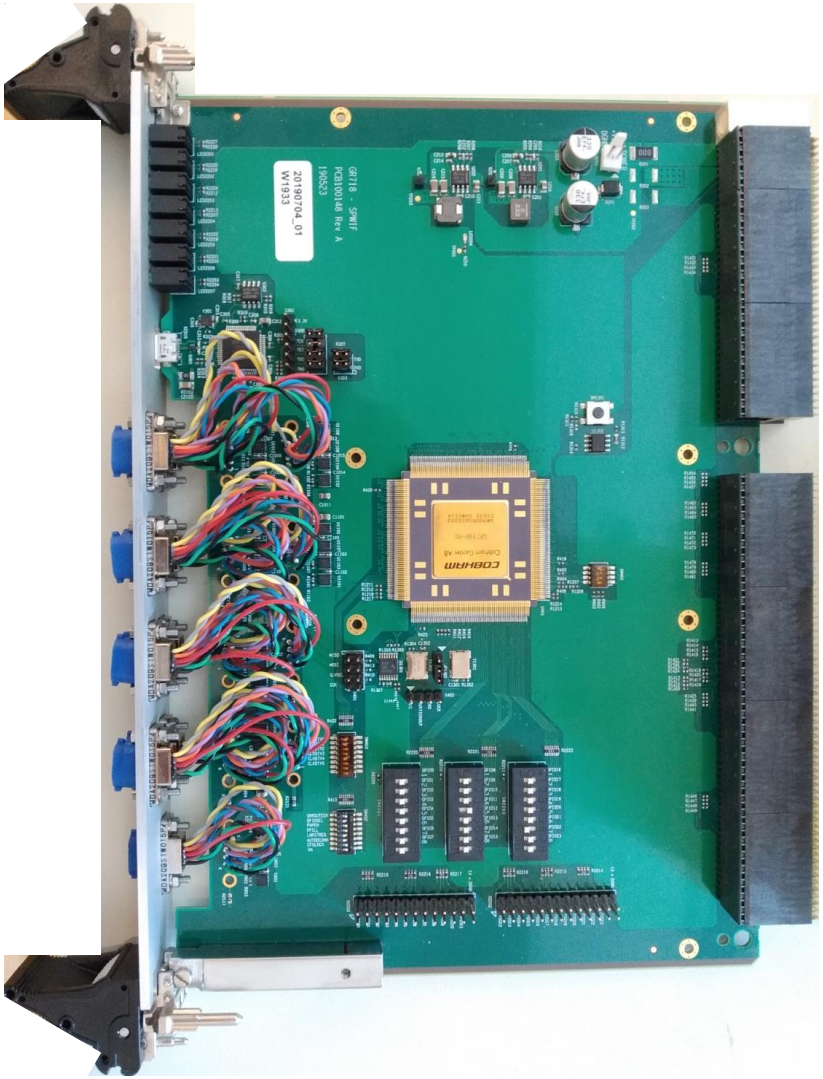
RDHC hardware
DIGANIF board

- GR-VPX-DIGANIF
- BRAVE NG-Medium (plastic), digital and analogue interfaces
- Development completed



RDHC hardware
SPWIF board

- GR-VPX-GR718
- GR718B SpaceWire router
- 9 external SpW interfaces
- Development completed



RDHC hardware
Chassis and cabling

- Chassis
  - ELMA 6U, 5 slots
  - OpenVPX Backplane profile 11.2.5
  - Procured and delivered

Other hardware developed:

- I/O cabling
  - Custom-designed
  - RDHC to SCOE (SAGE) interface
  - Development completed

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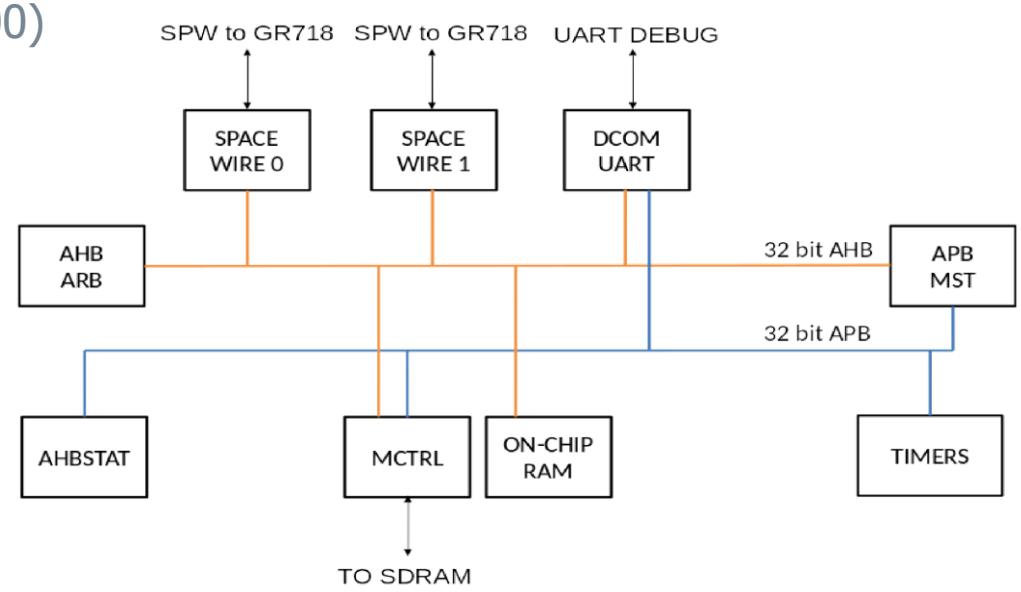
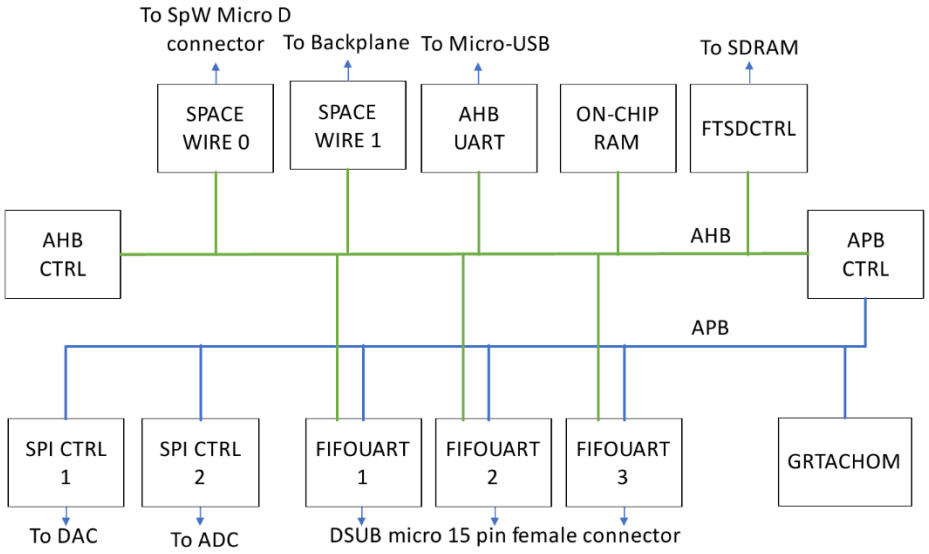
- IP cores used
  - SpaceNet – RMAP IP Core (v 1.00)
  - AHBARB
    - AHB arbiter and decoder
  - APBMST
    - AHB/APB bridge
  - AHBRAM
    - On-chip RAM with AHB slave interface
  - TIMERS
    - Two general purpose timers and one watchdog
  - DCOM
    - UART for debug support unit
  - MCTRL
    - Controlling 128 MByte of usable external SDRAM with EDAC
  - AHBSTAT
    - AHB status register. Latches the address and bus parameters when an error is signaled on the AHB bus



- Modules included
  - One SpaceWire codec
    - With AHB host Interface and RMAP targets
  - Three UARTs
    - With FIFO and separate baud rate generators
  - Two SPI controllers
    - Configured as SPI master, with one slave select signal and FIFO depth equal to 8
  - One AHB UART
    - Usable as a debug Link
  - An on-chip RAM
    - Size 2 KB
  - A GRTACHOM IP
    - To acquire (measure) the RW Discrete Digital Tacho inputs



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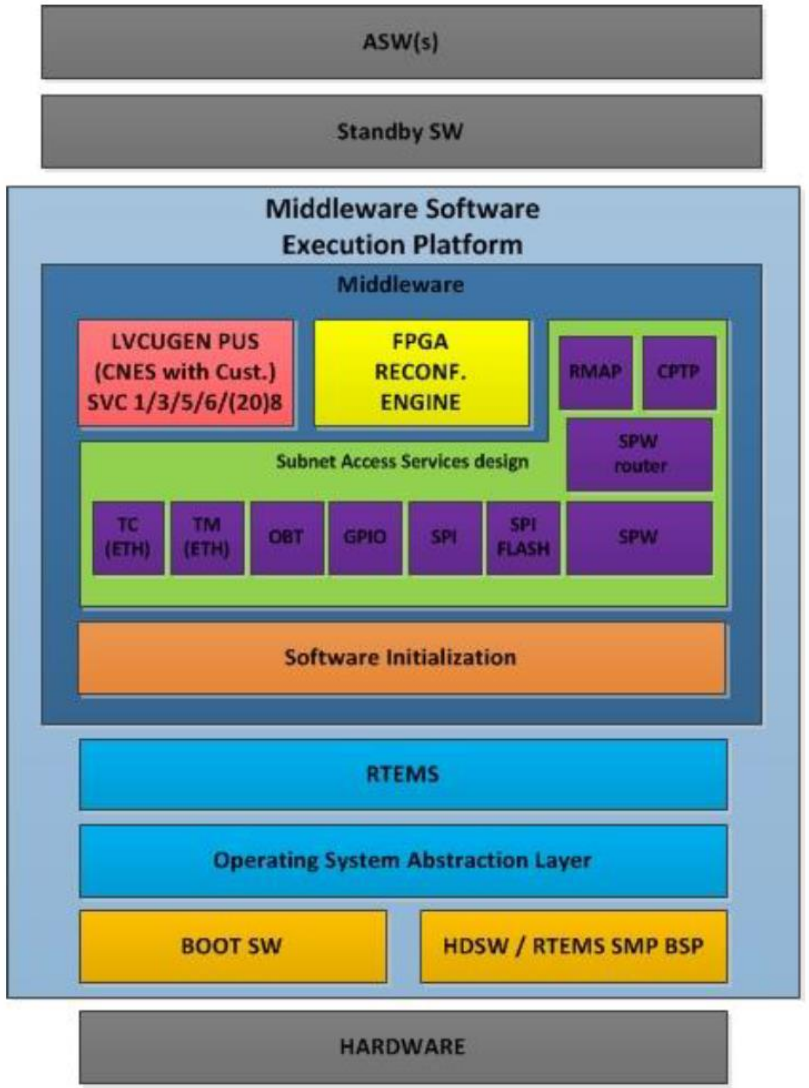
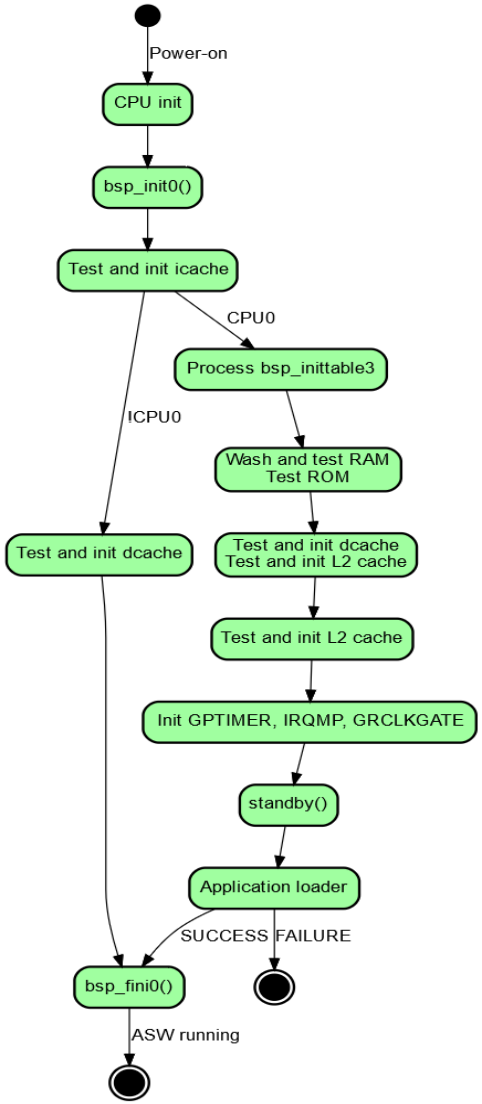
Software
Overview – execution platform

- Application layer with an abstraction suitable for RDHC operation
- Main components
  - RTEMS 5.1 SMP
  - RDHC BOOT SW
  - RDHC BSP and Drivers (HDSW)
  - RDHC FPGA Reconf. Engine (for BRAVE Medium)
  - LVCUGEN LIBPUS from CNES
  - RDHC Middleware



Software
Low-level initialization (boot)

- GR740/RDHC Boot SW
- Compliant with ESA initialization requirements
- Peripheral initialization
- Self-tests
- Application loader
  - Application stored in SPI flash
- Support for SMP boot
  - RTEMS
  - Linux, VxWorks
- Available as a product outside CORA



- RDHC Drivers (SW, validation tests, API and doc.)
  - SPI controller
  - SPI flash
  - GPIO
  - Timer
  - Clock gating unit
- RTEMS-5 provided drivers
  - SpaceWire DMA
  - SpaceWire router
  - UART
- Also provided
  - RMAP transaction example
  - SPI flash access example

Software
Middleware with FPGA reconfiguration engine

COBHAM

The middleware provides PUS services over SpaceWire:

- Service 1: TC ack and completion
- Service 3: Housekeeping TM report management
- Service 5: Event report management
- Service 6: Memory management for accessing non-volatile memories
- Service 8: Function management for custom commands

Service 6 and 8 allows for

- Upload a file to the on-board FPGA bit-stream memory
- Initiating FPGA reconfiguration using the FPGA reconfiguration engine.

FPGA reconfiguration engine

- Interface to reconfigure the FPGA on the EBB
- FPGA bitstream selected through a run time parameter
- Integrity control

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Experiences
Major challenges and lessons learned

COBHAM

- Three parallel CORA activities
  - Requirements and interfaces defined during the activities
  - External dependency
  - Focus of eliminating blocking points
  - Consolidation at workshops

  ►Top-level "system managers" for all three activities from both ESA and industry could have been beneficial

- In addition, another dimension of requirements
  - Consolidation with ESA
  - Path to flight
    - Redundancy concepts
    - Form factor
  - Platform for reconfiguration concepts

  ►Sometimes driving the schedule but not being beneficial for the triple-CORA activity (but justified for other reasons)

Experiences
Major challenges and lessons learned, cnt'd

- Complex hardware
  - Backplane interfaces allowing up to 728 pins for each board
  - ►Careful end-to-end reviews recommended for signals over backplanes
  - ►Do not mount unused connectors (to limit board insertion forces)
- New technologies
  - Characteristics of BRAVE Medium components were not fully known
  - Synthesis tool for BRAVE Medium was not fully mature
  - ►Margins in duration and resources needed
- Support to external parties
  - The amount of HW- and SW-support provided by RDHC to the other CORA activities was underestimated at project kick-off
  - ►Workload for support should be planned from start

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Major results

- COTS BB platform delivered
  - Supporting MBAD and SAGE activities
- RDHC hardware developed and delivered
  - One rack with all three modules plus I/O cabling verified and delivered
  - Currently in use with the CoRA-SAGE team for closed-loop testing.
- FPGA design
  - VHDL source code delivered for BRAVE NG-Medium on the Processing Module
  - FPGA bitstream delivered for the I/O module
- Software developed
  - Boot software and basic drivers verified and delivered
  - Middleware software tested and delivered
  - FPGA reconfiguration software tested and delivered
- User manuals for all hardware and software delivered
- Duration
  - Approx. 6 month longer for HW deliveries than originally planned
  - Main reasons: comprehensive hardware analyses and extensions, plus triple-activity dependencies

Summary
Way forward

- In the CORA-RDHC activity
  - Prepare and perform ESTEC Avionic Lab testing with CORA partners
  - Complete related deliverables

- Potential post-CORA use
  - Commercialize parts of the hardware, whereof in near-time
    - The 2nd GR-VPX-GR740 (EBB) has been manufactured
    - Draft datasheets available
    - The OpenVPX rack is a defined product
  - Development of mezzanine for GR-VPX-GR740 supporting HSSL
    - On-going planning
    - BRAVE Large replacing BRAVE Medium on Mezzanine and DIGANIF
  - Platform for other ESA activities

Thank you for your attention!


COBHAM