REDOUBT – Reliable FPGA Datapath Design Using Control Techniques

During the REDOUBT project, a novel fault tolerant technique for digital arithmetic data paths based on control engineering techniques has been developed. The proposed technique aims at reducing or mitigating the errors that appear in these circuits, by applying correction factors to a set of data registers on the datapath. In order to determine the correction factors, we have considered the faulty circuit as a process with disturbances, and a dynamic model has been provided for it. For this model, we have determined a number of output states – registers that are compared to a reference –, and a number of corrected states – registers to which the correction factors are added. This dynamic model has been linearized and reduced after applying a balanced transformation. Using the reduced dynamic model, a linear controller is developed, and a gain matrix is computed. The correction process, applied to the original nonlinear model, is performed in several iterations, by re-performing the computations associated to the sub-modules that contain the corrected registers. A key issue is represented by the necessity of a reference, for which we have provided the solution of using two controlled circuits in feedback. The results are comparable to a modified TMR from which non-admissible values have been excluded, while the implementation costs are reduced by 10%.