REDOUBT - Reliable FPGA Datapath Design Using Control Techniques

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Title of Presentation

- *Budget: 48,260 €*
- *Duration: 12 months*
- *Prime: Universitatea Politehnica Timisoara (UPT, RO)*
- *Subco: Universitatea Tehnica Din Cluj-Napoca (UTCN, RO)*
- *Main Objectives:*
    1. Develop novel fault tolerant techniques for digital datapath circuits by applying control feedback loops
    2. Minimise the overhead implementing the fault-tolerant system with the application knowledge, in this case, control feedback loops