

Assessment studies – FPGA Verification Tool

This project was established to improve the verification of space related FPGA functionality – in order to improve quality and reduce development time. The project is based on UVVM (Universal VHDL Verification Methodology) – as the only VHDL verification methodology with standardised handling of verification components, high level commands, functionality extension, split transactions and interface synchronisation, - focusing on overview, maintainability, extensibility, debuggability and efficient reuse.

The target for this project was to improve UVVM further to handle space related FPGA projects even better. The main functionalities to be added were generic scoreboards, structured control of randomisation, functional coverage, error injection and property checking, monitor, watchdogs, local sequencers, transaction transfer from VVCs (VHDL Verification Components) to models, hierarchical VVCs and specification coverage. Some of this was totally new functionality, whereas other parts were just structuring the concepts, methodology, commands, parameters, etc.