

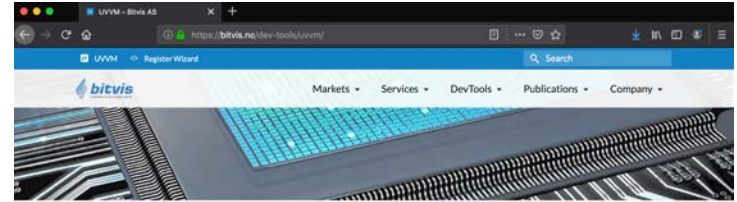
Assessment studies – FPGA Verification Tool - UVVM

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FPGA Verification Tool - UVVM

- *Budget: 210,000 € + 73,463 € (CCN)*
- *Duration: 18 months (+ 6 months CCN)*
- *Prime: BITVIS (NO)*
- *Main Objectives:*
 1. Enable more productive verification by simulation, a key phase in ASICs and FPGAs
 2. Extend the Universal VHDL Verification Methodology



Universal VHDL Verification Methodology

UVVM is a VHDL testbench infrastructure, Architecture, Library and Methodology for making better VHDL testbenches. UVVM is used world wide to speed up verification and improve the overall FPGA design quality. Applicable for both FPGAs and ASICs.



VVC Framework Utility Library

Benefits

- Open Source library
- Testbench kickstart
- Great overview and readability
- Efficient and easy to maintain
- Modular, reusable and extendable
- Vital for FPGA development quality
- Allows simple control of Constr.Rand. and Func.Cov.
- Seamless integration with OSVVM Constr.Rand and Func.Cov
- Modern verification methodology



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Extensions within the scope of the activity:

- Scoreboarding
- Monitors
- Controlling randomisation and functional coverage
- Error injection (Brute force and Protocol aware)
- Local sequencers
- Watchdog (Simple and Activity based)
- Controlling property checkers
- Hierarchical VVCs - And Scoreboards for these
- Direct Transaction Transfer
- Specification Coverage

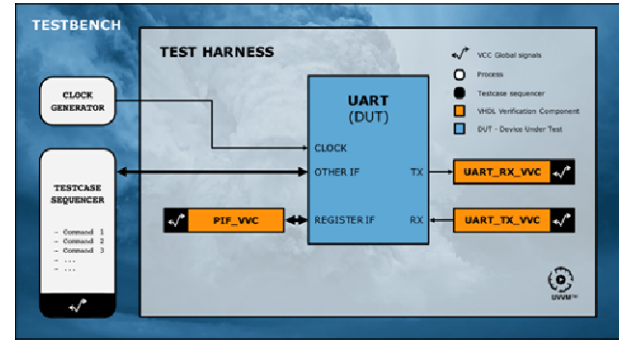


Figure 1: UART Testbench in UVVM (courtesy of Bitvis).

