Assessment studies – FPGA Verification Tool - UVVM

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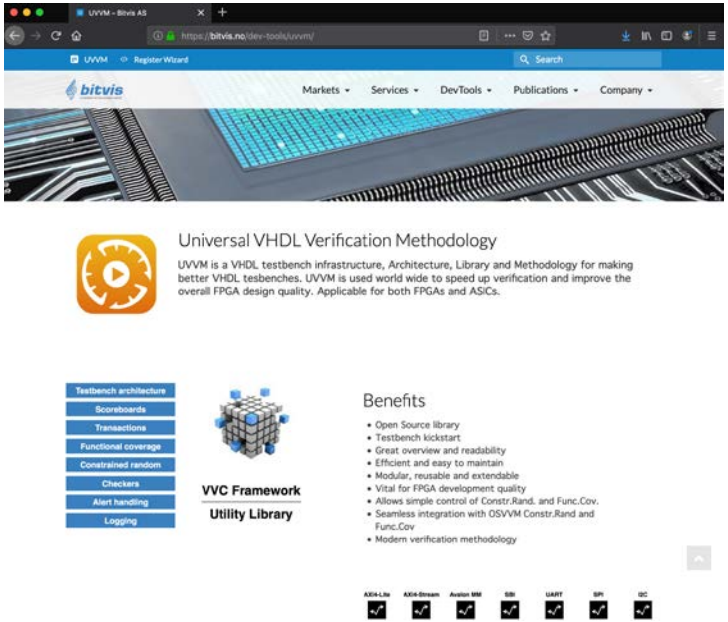
FPGA Verification Tool - UVVM

- *Budget: 210,000 € + 73,463 € (CCN)*
- *Duration: 18 months (+ 6 months CCN)*
- *Prime: BITVIS (NO)*
- *Main Objectives:*
    1. Enable more productive verification by simulation, a key phase in ASICs and FPGAs
    2. Extend the Universal VHDL Verification Methodology



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Extensions within the scope of the activity:

- Scoreboarding
- Monitors
- Controlling randomisation and functional coverage
- Error injection (Brute force and Protocol aware)
- Local sequencers
- Watchdog (Simple and Activity based)
- Controlling property checkers
- Hierarchical VVCs - And Scoreboards for these
- Direct Transaction Transfer
- Specification Coverage

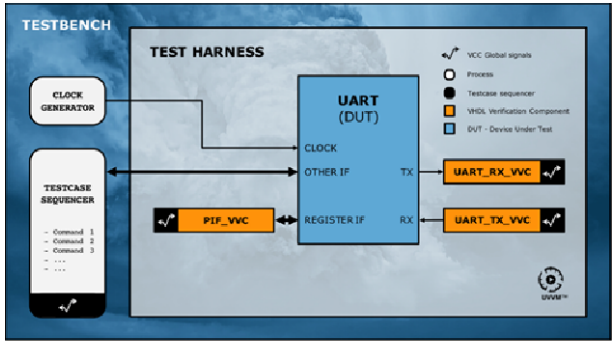

Figure 1: UART Testbench in UVVM (courtesy of Bitvis).