Single chip dc-dc controller with high voltage input Primary

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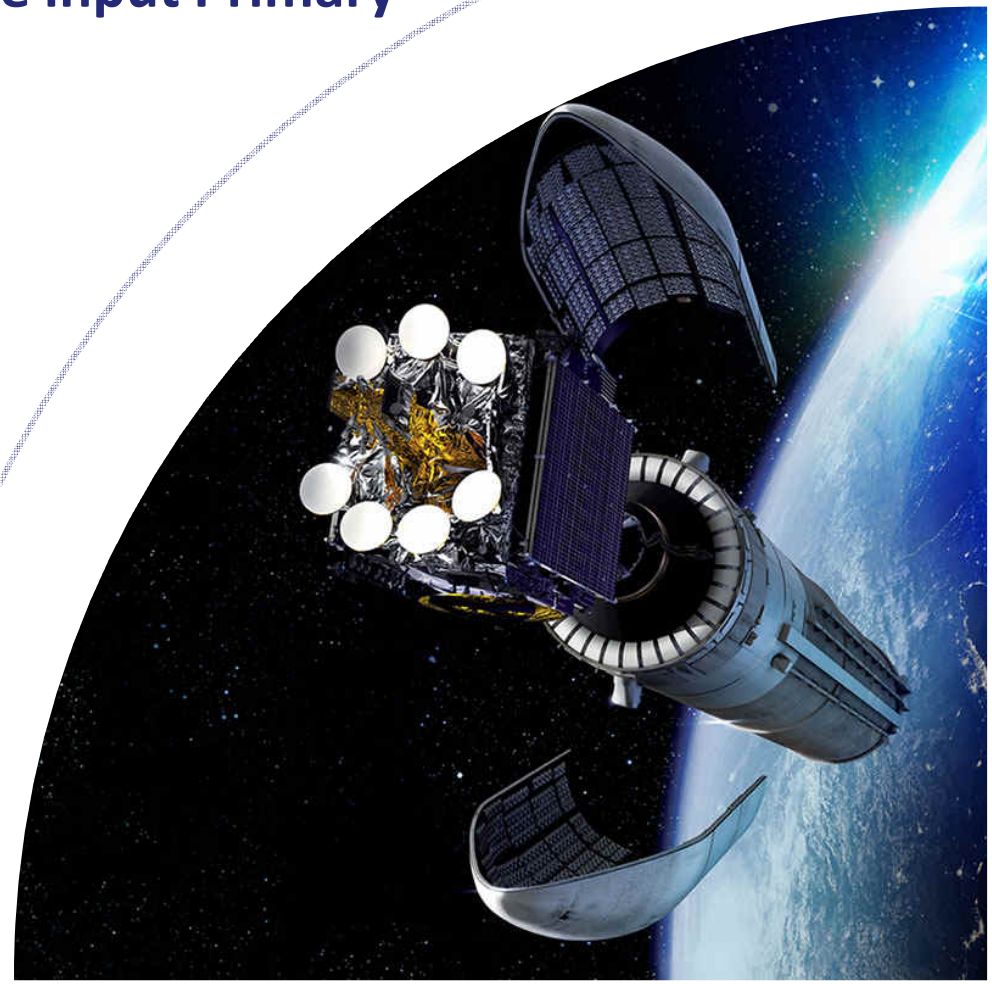

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Date: 26/05/2021
Ref: HSC-RUN2-TASB-XR-0103 rev1.0
Template: 83230347-DOC-TAS-EN-010

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HIGH SPEED CONTROLLER (HSC)

a lot more than a “PWM controller” ➔ Swiss knife for dc-dc designer

Several Band gap voltage reference: segregation regulation & protection

Protections:

- OVER-VOLTAGE & UNDER-VOLTAGE
- OVER-CURRENT
- OVER-TEMPERATURE: 2X EXTERNAL & 1 INTERNAL

HF signals to cross galvanic barrier

- OPTO-COUPLERS ➔ 20MHZ ULTRA COMPACT TRANSFORMERS
- 2X ALARMS + 1X PWM

RC Oscillator + ext. Sync input

VCO ➔LLC variable Switching freq. converter

Soft Start

Bus undervoltage lock out (UVLO)

Auto-restart with HICCUP / TC on & TC off control.

Power requirement ~20mA / 5V

No need for additional active control / monitoring devices whatever the dc-dc type.

HIGH SPEED CONTROLLER (HSC)

High voltage features …

/// High voltage transistors used & managed such as to be tolerant to radiations

➔ **Nothing (no discrete semiconductor) else required in dc-dc design than power devices**

OK for power diodes & transistors, Mosfet or GaN

/// Connection to Vbus

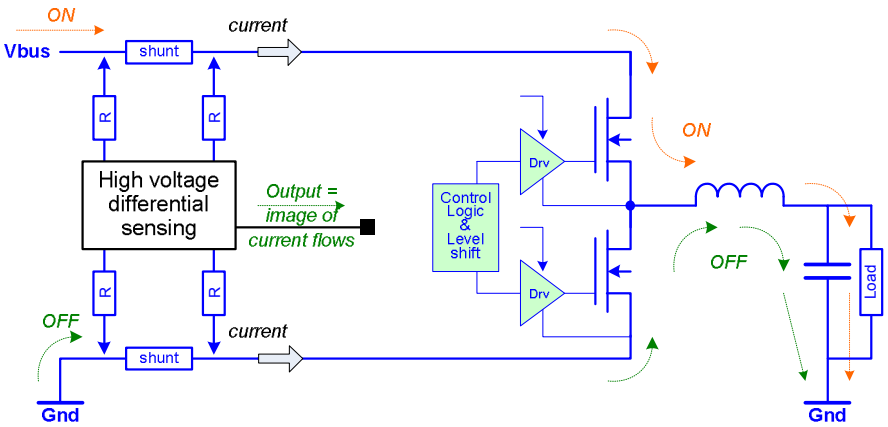
➔ continuous operation on +100V bus with ripple & 33% transients ie. >135V peak

/// High voltage drop / low current linear regulator to enable supply of …

- Startup of the dc-dc
- Holding of the On/Off status of the dc-dc
- Bus under-voltage protection & over T° protection

/// Current sensing on a shunt in the hot Vbus line

- Double differential amplifier with very high common mode.



HIGH SPEED CONTROLLER (HSC)

Half-bridge GaN ➔ new dc-dc topologies & higher speed

Capable to control complex topologies

- PHASE SHIFTED FULL BRIDGE
- SMART: ZVS BUCK + ZVS PUSH-PULL
- LLC: HALF BRIDGE OR FULL BRIDGE

Ready for 1MHz switching ⇨ GaN HEMT technology

- ON CHIP OSCILLATOR
- HIGH BW CURRENT SENSING AMPLIFIER
- HIGH SPEED PWM COMPARATOR
- CURRENT LEADING EDGE BLANKING FUNCTION

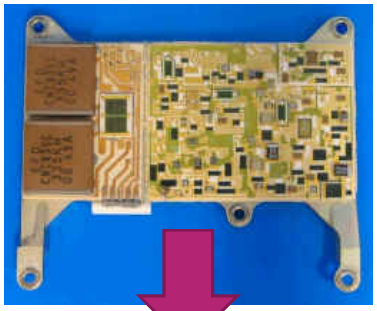
Multiple regulation/control schemes

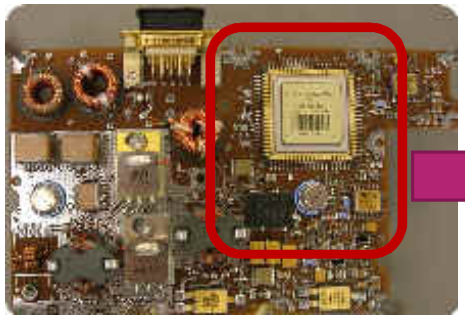
- CURRENT AVERAGE MODE
- CURRENT PEAK MODE + SLOPE COMPENSATION & EDGE BLANKING
- NEW PVCC PEAK & VALLEY CURRENT CONTROL

PRODUCT CONSTRUCTION ROADMAP

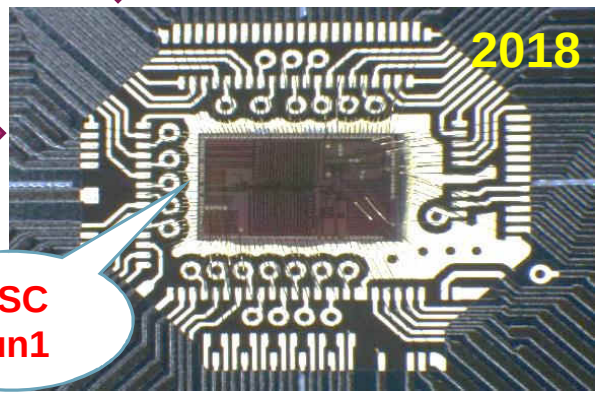
= IC design house
+ characterization &
volume production testing

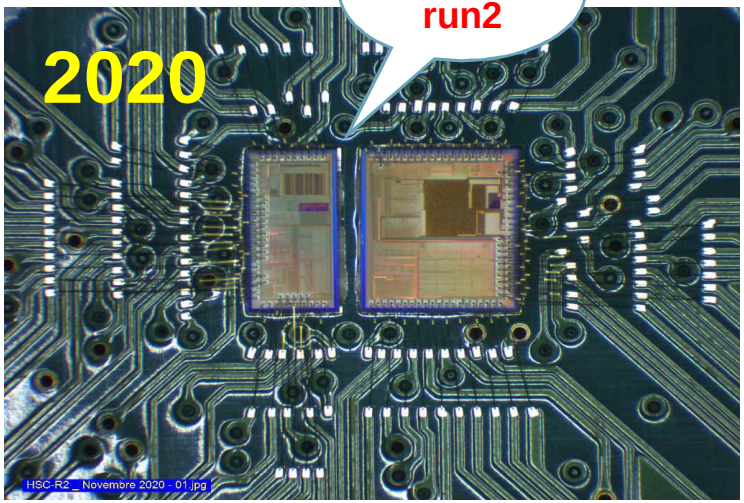
Return of experience from
20 years TAS-be dc-dc
designs included





AGENTSCHAP
INNOVEREN &
ONDERNEMEN





/// HSC-run1: Functionnal validation in real dc-dc applications
Characterization over T° / dose & heavy ions

/// HSC-run2: bug fixes + new feature = PVCC

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SEGREGATION

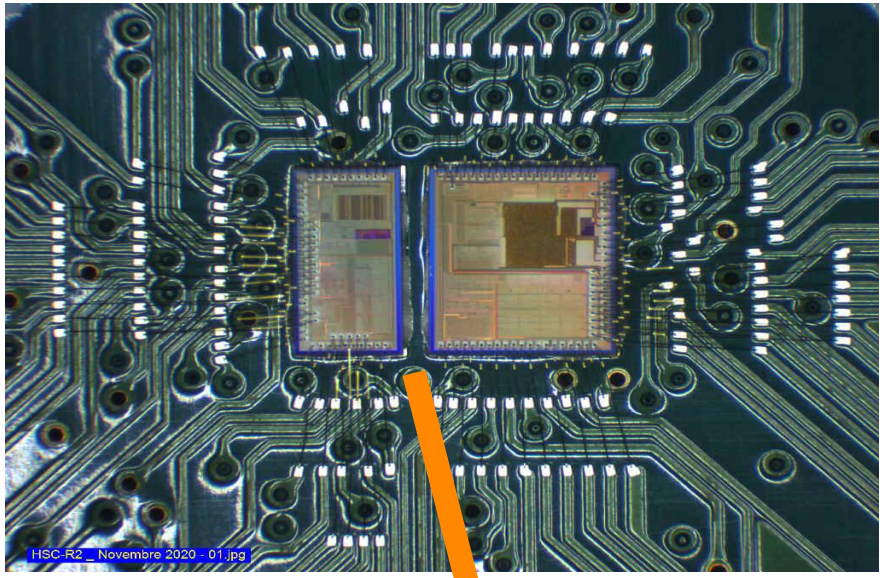
Regulation & protection may not share an element potentially leading to simultaneous failure

/// Regulation

/// Band-gap

/// OSC + PWM

/// Current sense



/// High voltage drop bootstrap supply

/// Band-gap

/// Protections

Physical rupture of the mono-crystalline wafer due to defect or crack at edges during dicing.

→ Physical split: 1/3 left & 2/3 right

Each side ➔ bandgap

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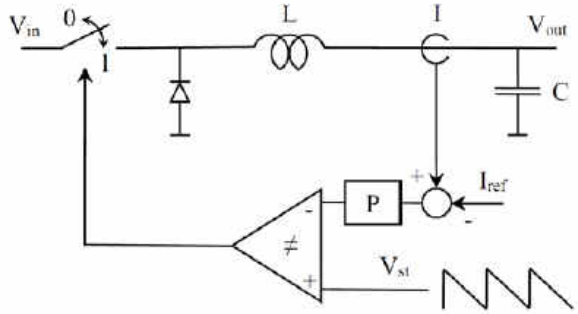
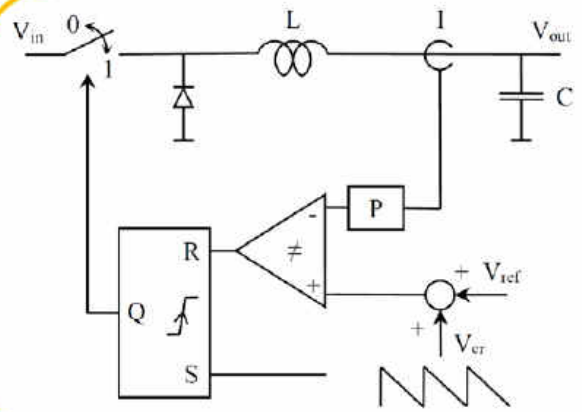
2. Current Control Loops



ACC

Average Current Control [2]

- ✓ Much used on spacecraft PF with symmetrical sawtooth



PCC

Peak Current Control [1]

- ✓ Sawtooth called compensation ramp
- ✓ Much used for terrestrial applications

Slide reprint from :
AVERAGE CURRENT CONTROL WITH ASYMMETRICAL SAWTOOTH OR PEAK CURRENT CONTROL
Christophe Delepaut, HadrienCarbonnier
ESPC 03/10/2019

[2] "PWM Conductance Control", D. O'Sullivan, H. Spruyt, A. Crausaz, IEEE Power Electronics Specialists Conference, Kyoto, Japan, 11-14 April 1988

[1] "Simple Switching Control Method Changes Power Converter Into a Current Source", C. W. Deisch, IEEE Power Electronics Specialists Conference, Syracuse, New York, 13-15 June 1978

PEAK & VALLEY CURRENT CONTROL SCHEME

Higher closed loop BW ~2x

Average current control with single sawtooth & single comparator
➔ limited loop gain (stability)
➔ limited closed loop BW

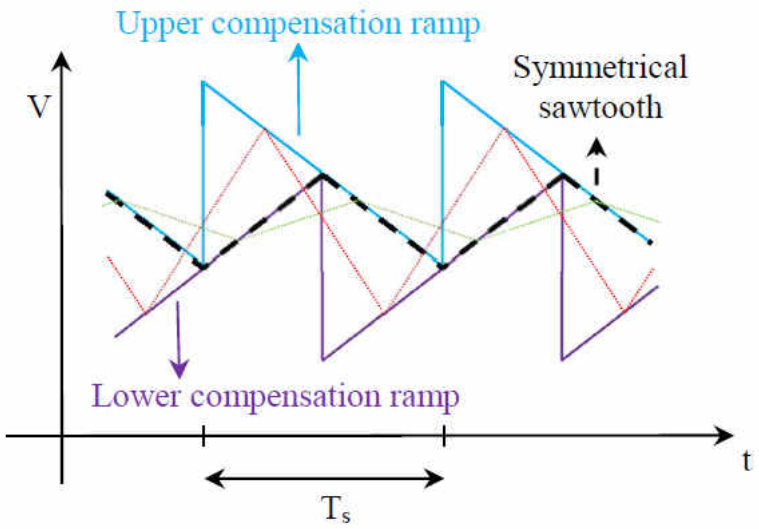
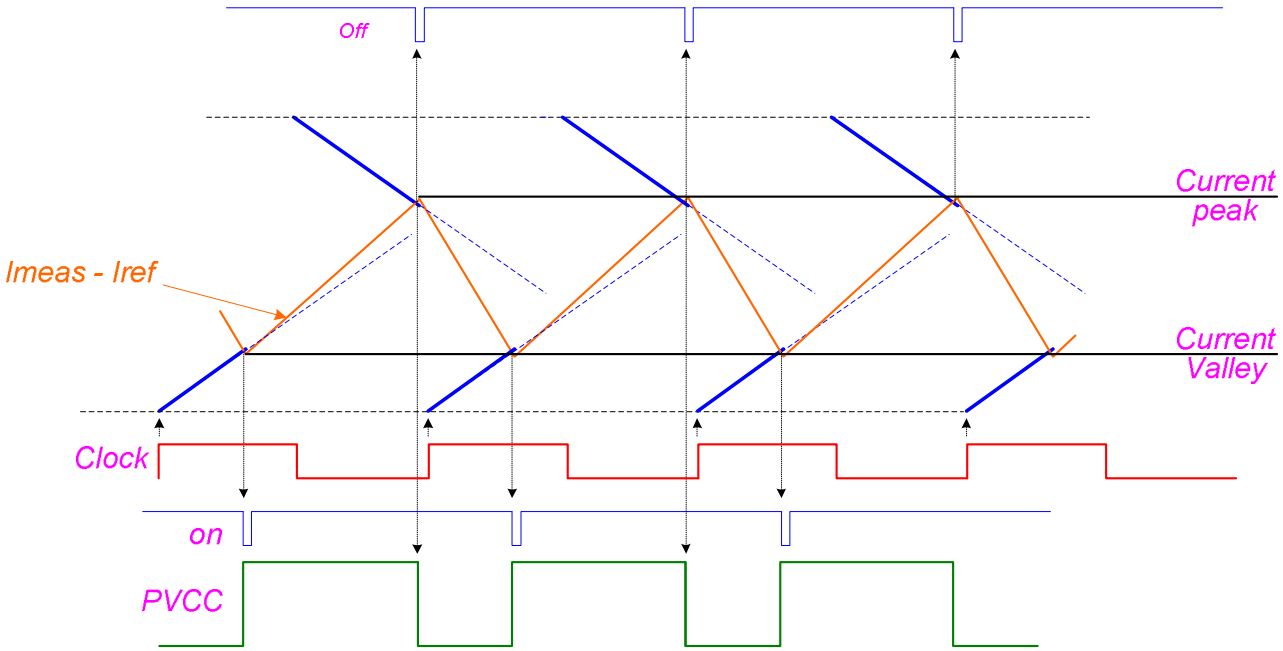


Fig. 9. Symmetrical sawtooth or upper and lower compensation ramps

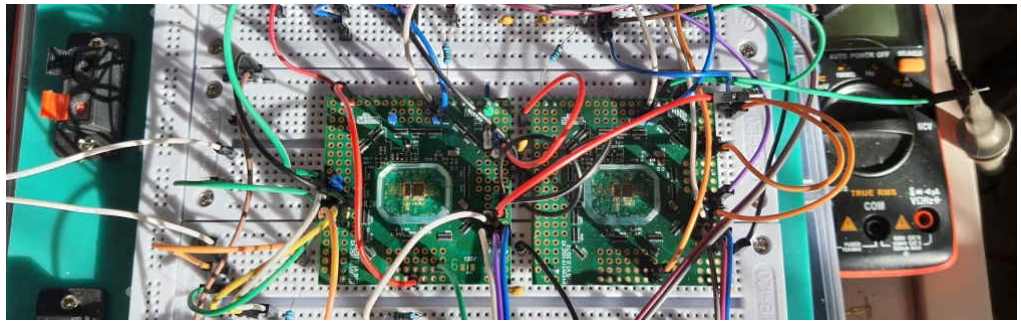


New implementation requires 2 sawtooth & 2 comparators + set / reset logic
➔ loop gain increase without stability issues

Average Current Control with Symmetrical Sawtooth or Peak and Valley Current Control
Christophe Delepaut & Hadrien Carbonnier ESTEC, ESA

ONGOING & FUTURE WORK

Formal performance verifications engaged



/// First electrical functional test completed:

/// ~1000 BGA packages expected in June

/// Electrical detailed characterization

/// Development of automated recurrent production test means

MINCET. Custom Integrated Power Management Solutions

/// ESD & Radiation (dose + heavy ion) tests

/// 1st batch Qualification according to ESCC-Q60-13C

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ThalesAlenia Space

ACKNOWLEDGMENTS

Project = High Speed integrated analog dc-dc Controller for space applications = HSC-run2

ESA Contract No. 4000126321/19/NL/AF

“Integrated power switch ASIC for small dc-dc converters”

Project = High Voltage Silicon for Radiation Hardened applications = HV-Si-Rad