

# Single chip GaN half-bridge with integrated drivers

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# ! REVOLUTION IN POWER CONVERTERS : MOSFET → GAN

## /// Silicon power MOSFET

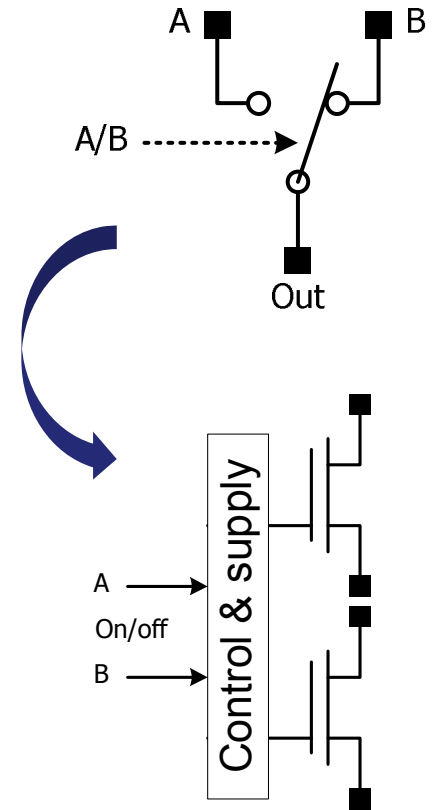
- Specific transistor design for radiation hardening → rare → expensive & restrictive export control rules apply.
- Bulky → easier to cool down.

## /// GaN

- Faster switching → more compact design
- Lower losses → better efficiency
- No (so far) specific transistor design required for radiation hardening
  - terrestrial automotive grade components produced in volume → lower cost
  - Up-screening & specific SOA for space applications
- Very compact → a lot more difficult to cool down

## /// Holy Grail for power converter designers = half-bridge module with GaN !

/// Supply chain through Eu suppliers & foundries → Eu independency



# CHALLENGES OF DRIVING GaN

## Pitfalls:

A GaN HEMT is not a MOSFET:

/// Lower and tighter controlled gate turn-on voltage

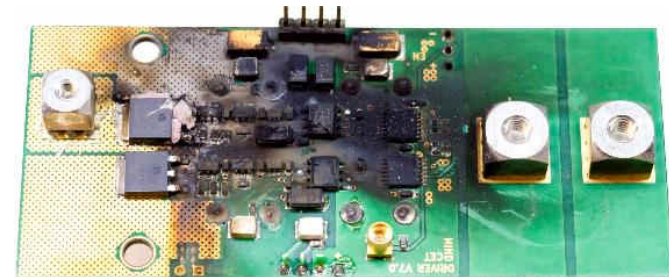
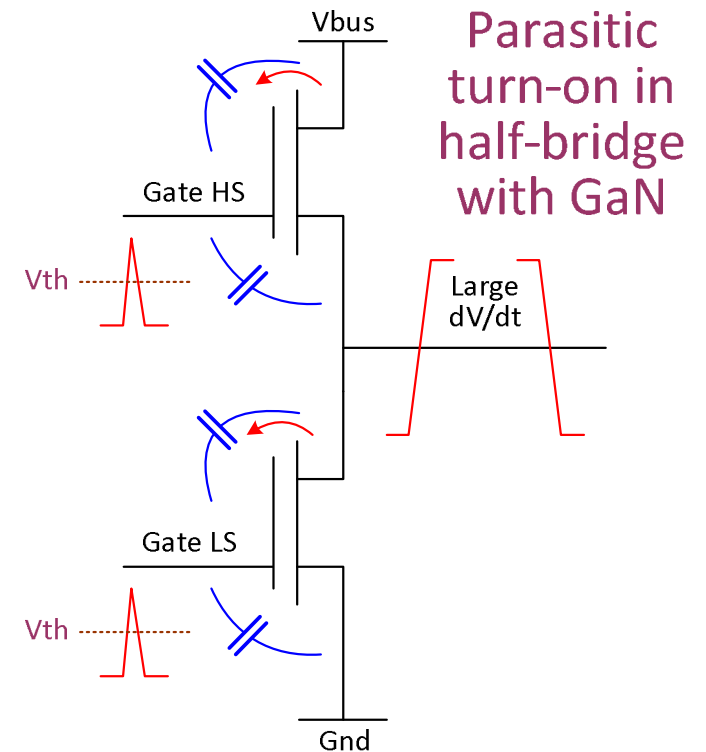
/// Lower threshold voltage ( $V_{th}$ )

/// Significantly faster Turn On and Off times -> High  $dV/dt$

/// Lower  $C_{gate-source} / C_{drain-gate}$  ratio

⇒ An ideal recipe for expensive fireworks

⇒ Needs an optimized gate-drive approach



# CHALLENGES OF DRIVING GAN

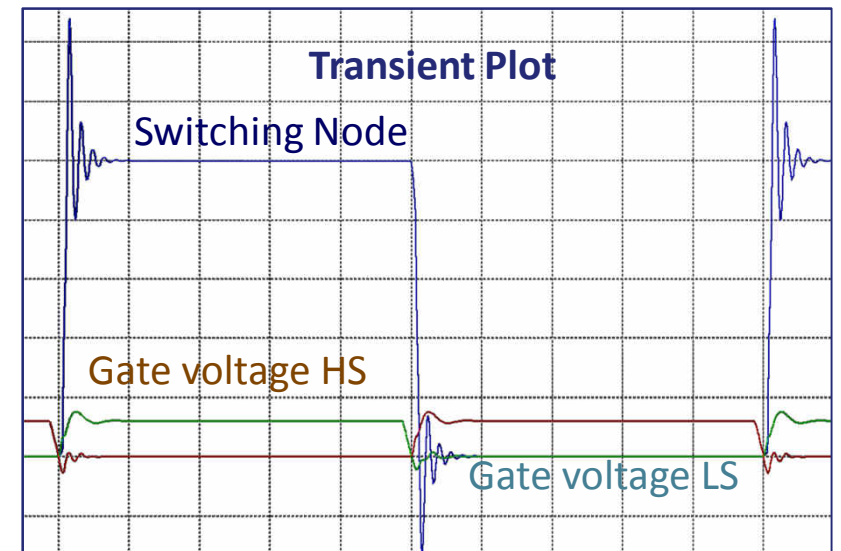
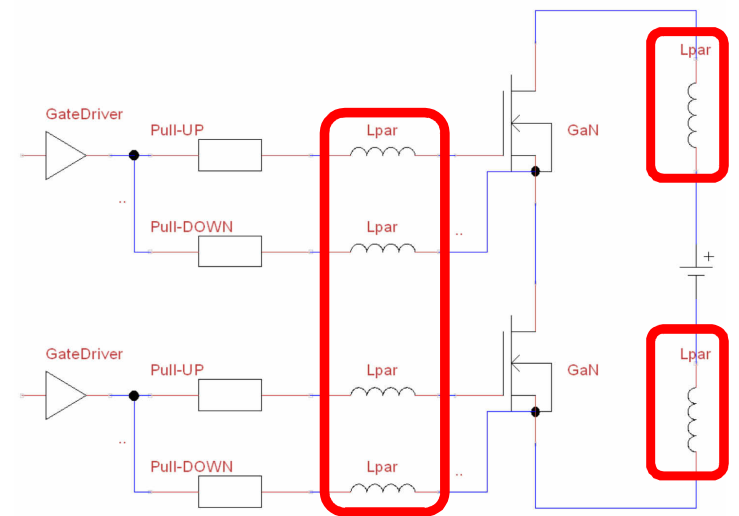
External gate driver:

## On PCB level:

- /// Gate-loop inductance
- /// Supply inductance
- /// Gate resistors
- /// Drain-source inductance

## On Gate-driver IC level:

- /// Dead-time control
- /// LS/HS delay-matching
- /// dV/dt immunity
- /// Negative source voltage from GND inductance
- /// GaN gate stress with overvoltage



# MONOLITHIC GAN HALF-BRIDGE + GATE DRIVER

## Challenges & differences :

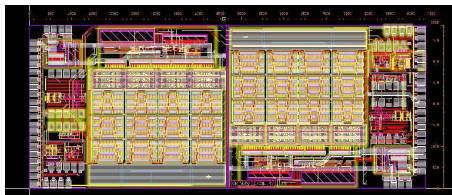
/// Reduce # external components in the system →

Increasing the overall system power density

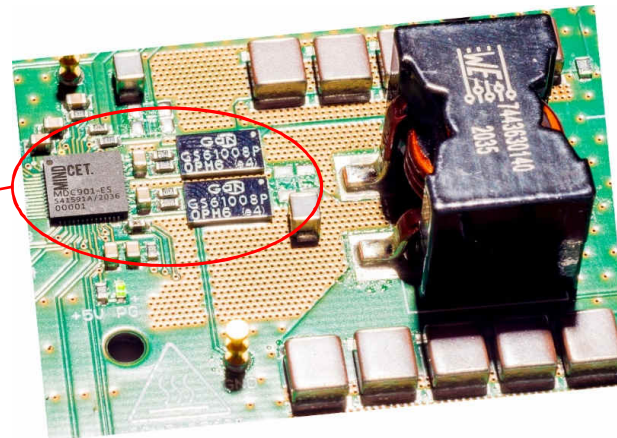
/// Strongly drive ( high & also low ! ) GaN up to speed by killing gate-loop parasitics

/// Reliability: minimize the gate voltage overshoot

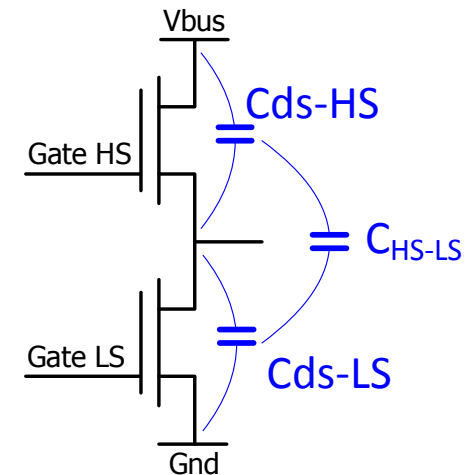
/// Require strong isolation between high side & low side power GaN



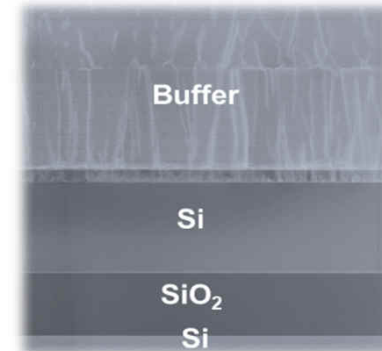
Design of full GaN ASIC !



Pictures courtesy of MinDCet



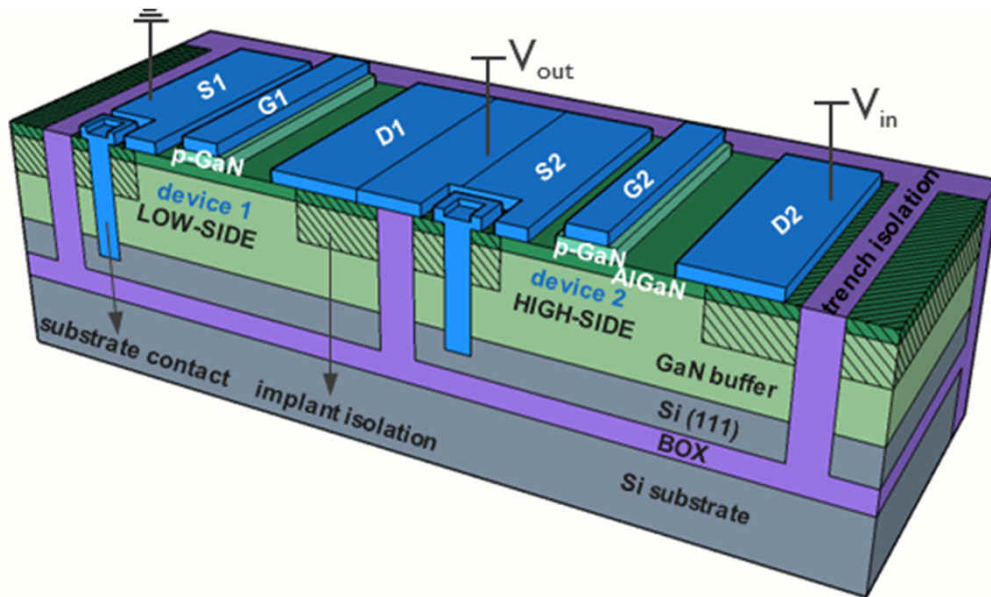
# Technology Makes the Difference



TEM cross-section of GaN/AlGaN superlattice-based buffer on SOI substrate.

/// Low cost (vs. SiC) SOI wafer as base for GaN HEMTs

/// DTI to electrically insulate HEMTs from each other



Schematic cross-section of GaN-on-SOI structure, featuring buried oxide, oxide filled deep trench, local substrate contact and p-GaN HEMT devices.

*Pictures courtesy of IMEC*



### /// Multi-Project Wafer Service @ imec - GaN IC MPW Service

Maritza Tangarife Ortiz <Maritza.TangarifeOrtiz@imec.be>

[https://www.youtube.com/watch?v=AwBA6gnw\\_xE](https://www.youtube.com/watch?v=AwBA6gnw_xE)

### 8-Inch GaN Power Device and GaN-IC Technology to Unleash Your Power IC

Denis Marcon, Senior Business Development Manager, IMEC:

<https://www.youtube.com/watch?v=S3d3E4LosNY&t=23s>

### /// ASCENT+ Webinar: GaN IC for Power Electronics

Urmimala Chatterjee (imec)

<https://www.youtube.com/watch?v=ILPLGivE-WY>



# DIE LAYOUT & MANUFACTURING

Multi-project wafer using GaN on SOI technology from IMEC\*

\* <https://www.imec-int.com/en/what-we-offer/development/system-development-technologies/GaN/IC-prototyping>

/// 7 $\mu$ m thick copper current redistribution layer at top

/// die size 9.3 x 3.8mm<sup>2</sup>

/// HS & LS GaN: ~22 mOhms each note: ~40 mOhms @ 150°C

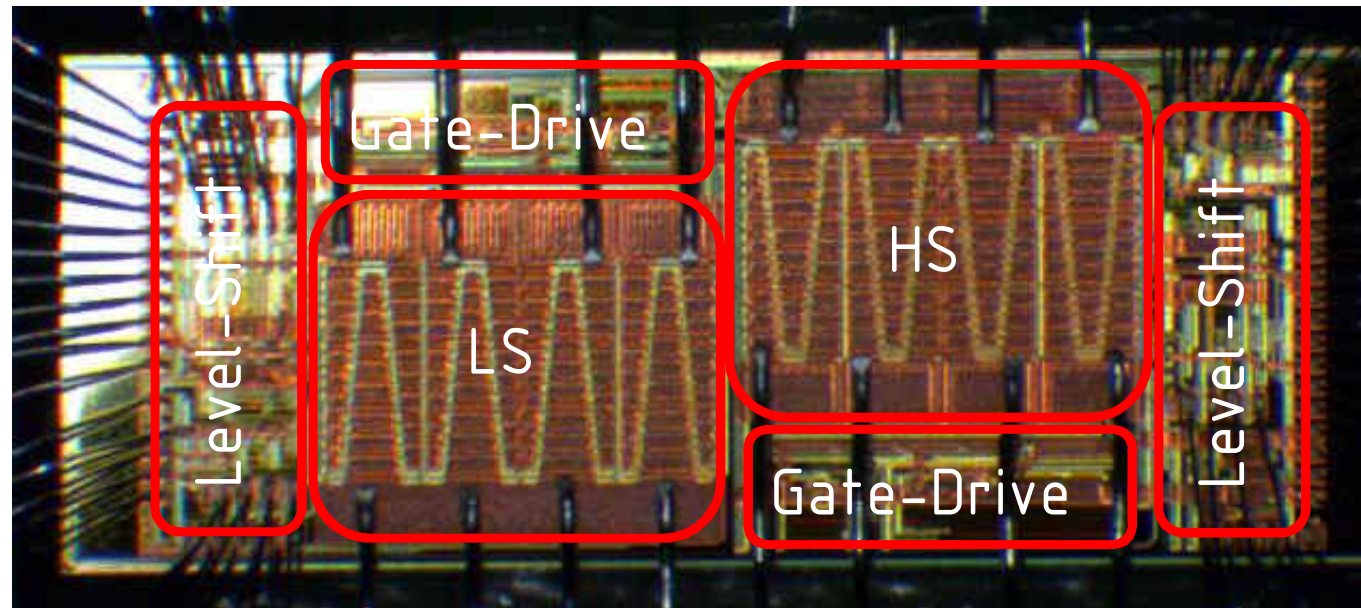
/// 200V Pgan HEMT

Ideally suited for 100Vbus main supply

/// Accessible freq. & currents:  
Limitation = die cooling !

5 MHz switching tested OK

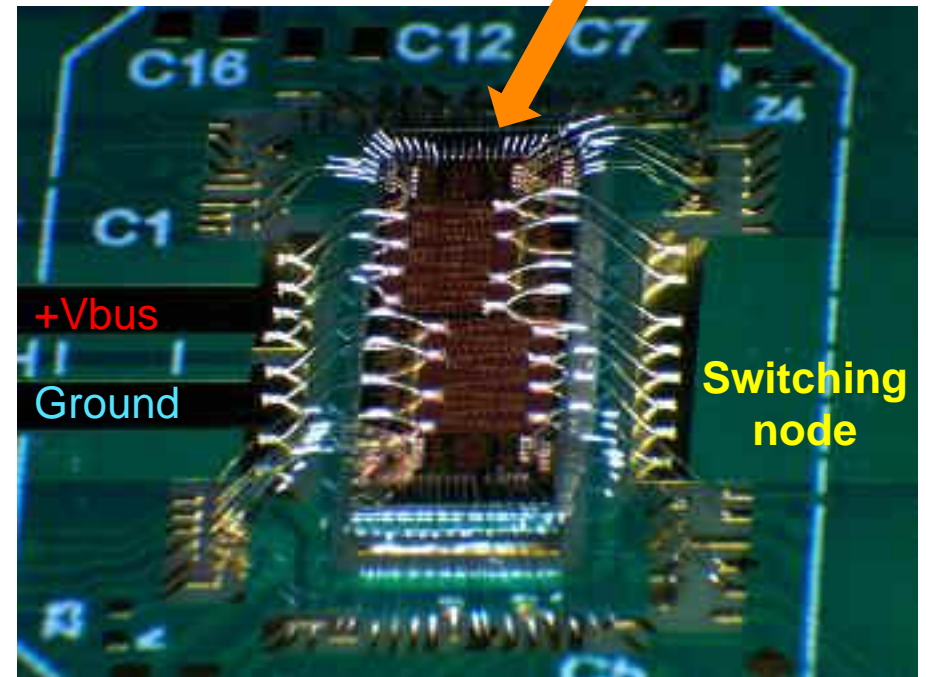
10 Amp current tested OK



# BUCK POINT-OF-LOAD IMPLEMENTATION

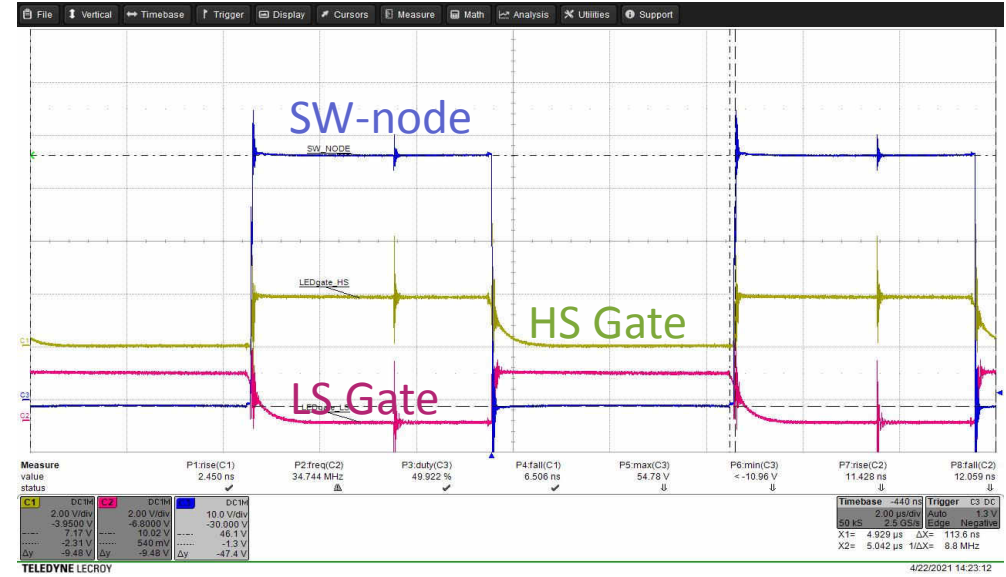
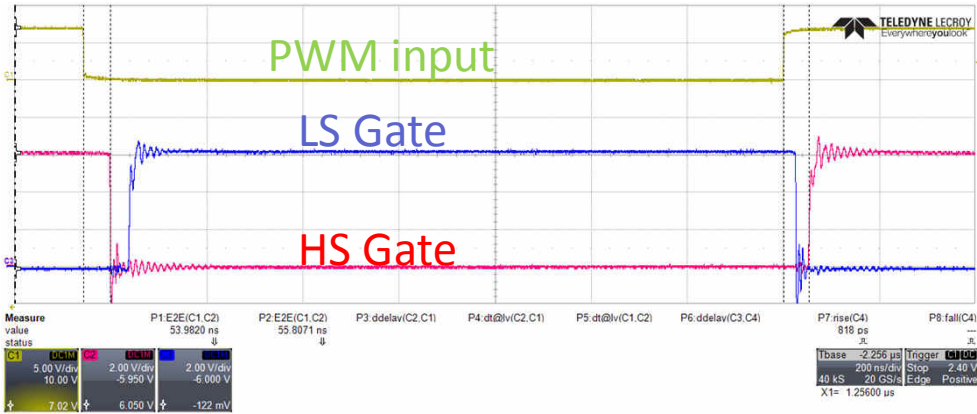
Preliminary prototype assembly without package

- /// Chip-on-Board: FR4 low cost PCB
- /// 4x 5mils bond wires in // for power pads  
~1,4 & ~2 mOhms extra due to bond wires
- /// 2mils bond wires for signals & test pads
- /// Thermally conductive glue
- /// Array of via throughout the whole PCB to transfer heat to opposite side → heatsink
- /// Silicone dam & fill for mechanical protection



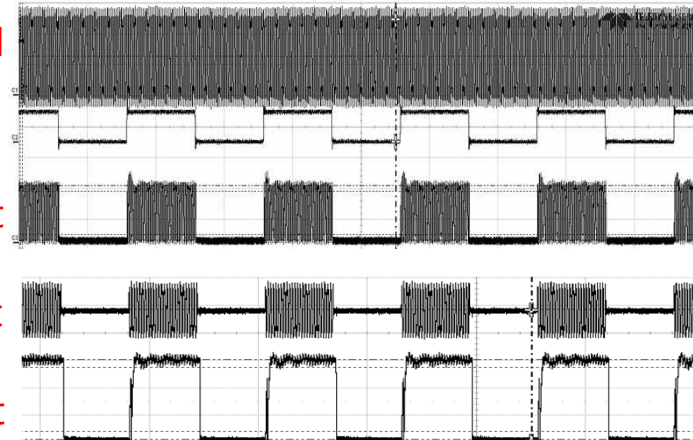
# GAN IC MEASUREMENTS

## On-chip dead-time generation:



## Isolated Level-Shifter using off-chip transformer :

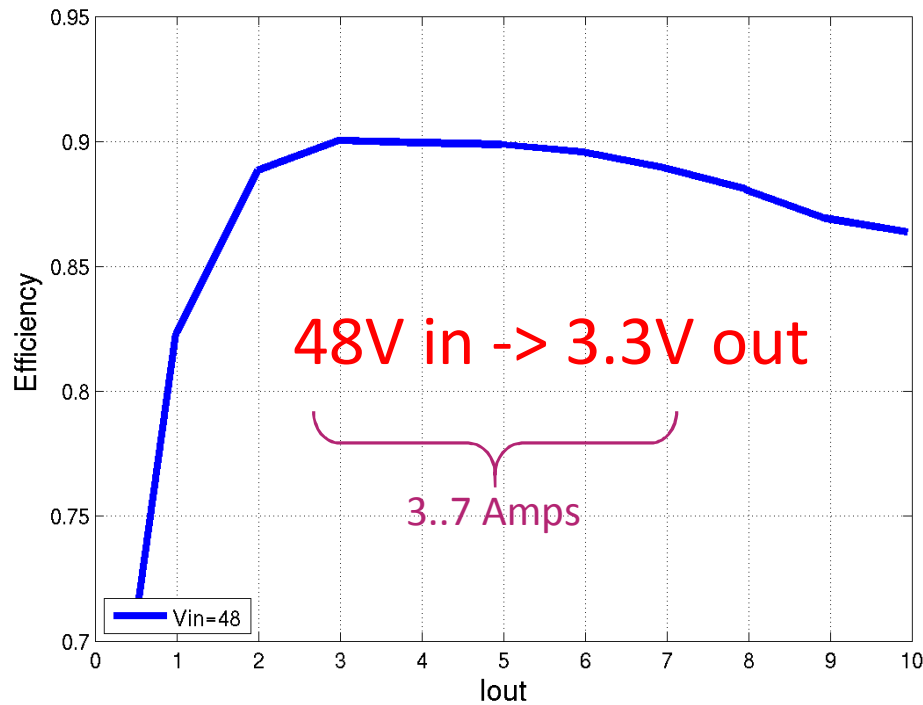
- RF signal
- PWM input
- Modulator output
- Demodulator output
- PWW output



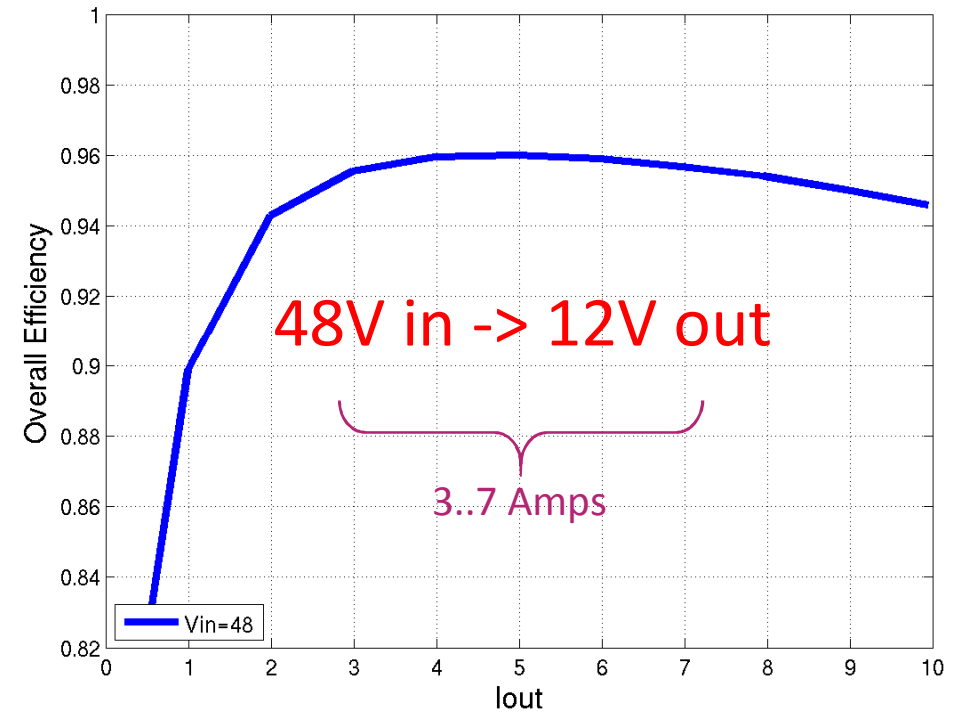
# GAN IC MEASUREMENTS

## Efficiency vs. output current

Sample S4 Efficiency vs Iout  
300KHz DC = 8%



Sample S4 Overall Overall Efficiency vs Iout  
300KHz DC = 25%



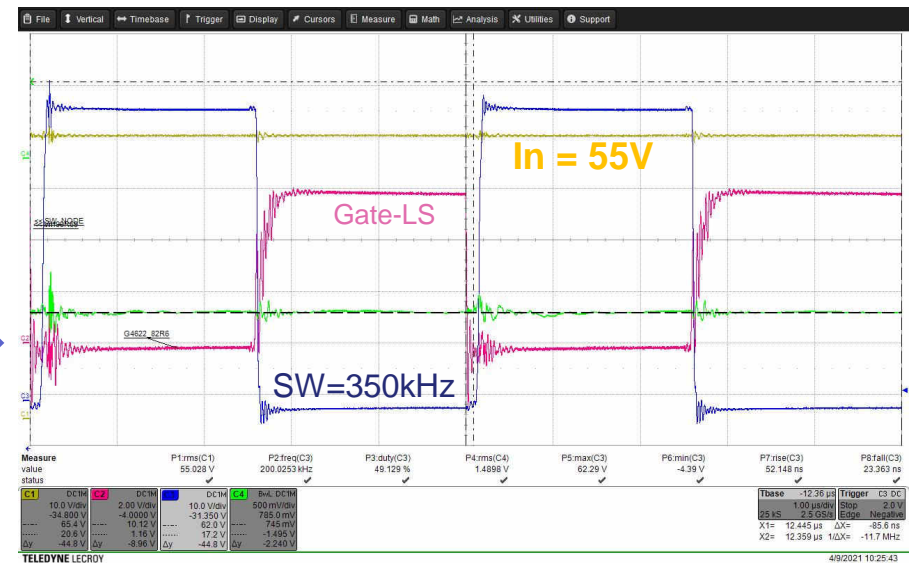
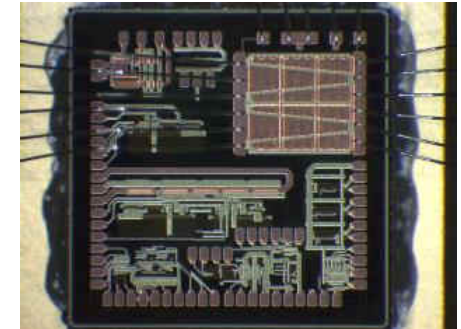
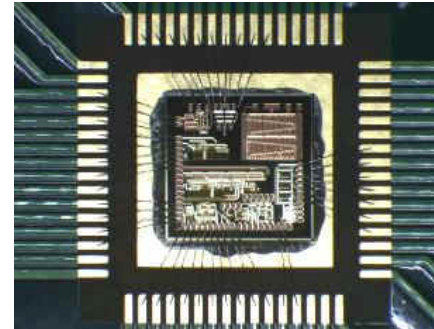
# ONGOING & FUTURE WORK

/// Tape-out run2 → 19 may 2021

Level shifter with improved dV/dt immunity

/// Radiation heavy ions testing

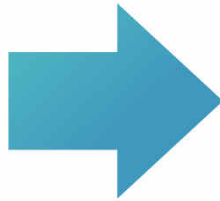
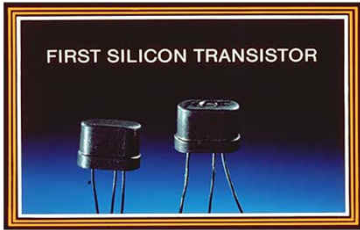
/// die characterization in PCDU like buck dc-dc



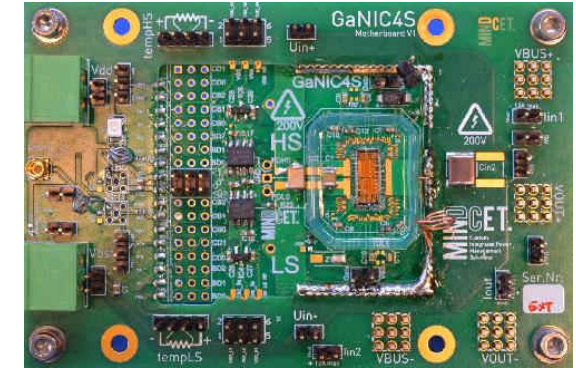
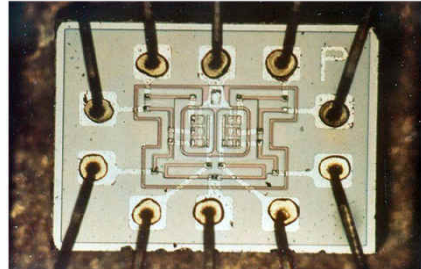
# A new flavor of ASIC: GaN !

Achieved 😊 !

In 1954, Texas Instruments was the first company to start commercial production of silicon transistors instead of using germanium.



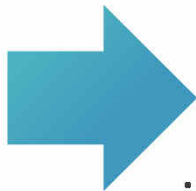
Fairchild 1961: logical NOR IC from the computer that controlled the Apollo spacecraft



Fully-qualified  
650 V GaN FET with the lowest  
R<sub>DS(on)</sub> in a TO-247

- Low R<sub>DS(on)</sub> 41 mΩ
- Increased power density
- Higher efficiency

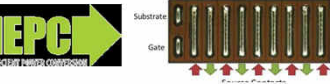
Discrete  
power  
transistors



2021

Integrated GaN IC with on chip:  
Half-bridge: HS & LS GaN  
200V / 3..7 Amp

- 2x gate driver
- 2x gate voltage regulators
- 2x PWM logic signal level shifters
- Deadtime generator
- Temperature sensor



## Impacts for space dc-dc designs:

- 👍 Faster switching → more compact
- 👍 Lower losses → better efficiency
- 👍 Monolithic IC → cheaper & very compact  
→ easy to use
- 👍 Radhard & European technology  
→ Eu export rules

# ACKNOWLEDGMENTS



Project = GANIC4S

“Monolithic integration of GaN gate driver and power transistors  
witching functions” ESA TDE Contract No.4000128515/19/NL/FE

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