esa imec MINDCET. Custom Integrated Power Management Solutions ThalesAlenia a Thales / Leonardo company Space

From: M.Fossion Date : 18/4/2021

Ref. : GANIC4S-TASB-GL-0003

Subject : ESA AMICSA conference May 2021 / paper submission abstract

Single chip GaN half-bridge with integrated drivers

Mike Wens / Jef Thone / Deniz Aygün from MinDCet
Marc Fossion from Thales Alenia Space Belgium
Stefaan Decoutere from IMEC
Andrew Barnes / Christophe Delepaut from ESA

IMEC has partnered with MinDCet (IC design house) & Thales Alenia Space in an ESA program for the development of a single chip half bridge with integrated pre-drivers. The IC is designed on IMEC's GaN on SOI & high voltage (200V) process.

The component includes follow features:

- High-side and low-side, high current (22 mOhms) P-GaN HEMT
- Integrated high-side & low-side gate drivers
- Temperature sensing
- Gate driver voltage regulation
- Isolated level-shifter for gate control signal propagation to floating levels
- Dead-time generator

Clearly this IC is a breakthrough as it is stepping away from traditional GaN and silicon co-packaging, where the performance limit is defined by package integration. Key enabler is the GaN on SOI technology developed by IMEC. This technology allows to co-integrate several devices on the same die using deep trench isolation. Although the co-integration of high-side & low-side power devices sounds straightforward, practical parasitic substrate capacitances often cause the exercise to fail.

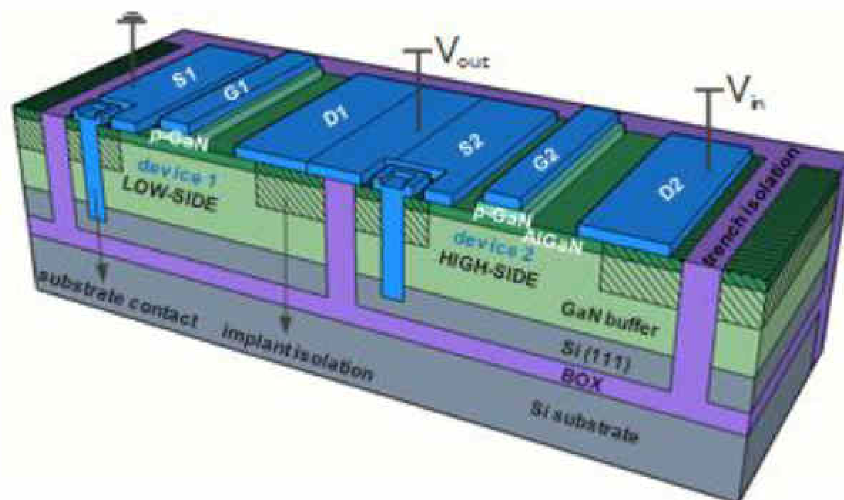

Figure 1 Cross-section of monolithic integration of HS and LS switch

A step forward in integration is the combination with on-chip gate drivers. Gate driving of discrete GaN HEMTs is well known to be challenging. Firstly , the high-side gate driver is floating between ground and Vbus. Furthermore, this happens at high dV/dt in the order of multiple tens of V/nS, making any parasitic capacitor a path for large current flow. Secondly, the parasitic turn-on through the Cgd capacitance leads to complex layout exercises between gate driver & discrete power devices. Co-integration of the driver will make sure that a strong active clamp is possible to avoid any parasitic turn-on.

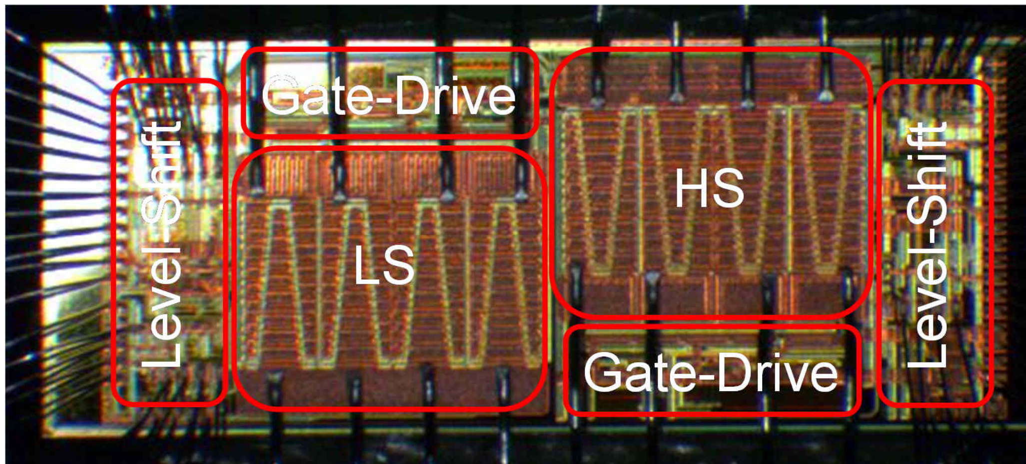

Figure 2 P-GaN HEMT Half-bridge 2x 22mOhm 200V with integrated drivers

First GaN Half-bridges were developed and tested in the frame of SloGaN VLAIO project. The aim was to achieve integration of high voltage & high current transistors with low voltage control & gate drive devices.

A full feature integrated GaN IC Half-bridge is currently in development under an ESA GSTP program. Figure 2 shows the IC, Figure 3 shows the buck dc-dc converter prototype.

Figure 3 10A point of load converter using integrated GaN ½ bridge

The IC performances reveal to be according to expectations & simulations. Figure 4 shows measured efficiencies in 2 difference point of load configurations.

All rights reserved, 2017, Thales Alenia Space

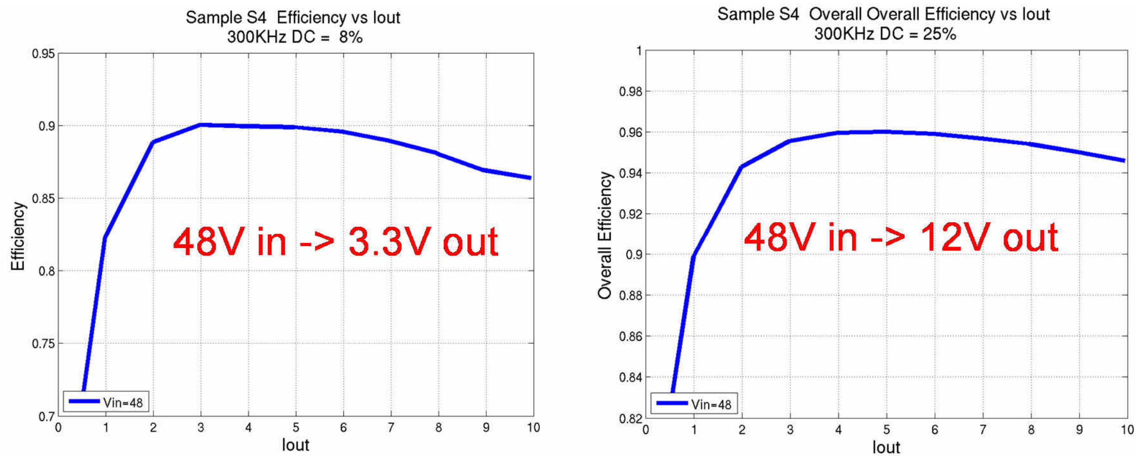

Figure 4 Efficiency results of **10A p**oint of load converter using integrated GaN ½ bridge

Acknowledgments

1. Project SloGaN System Level Optimization of GaN-based power devices funded by Agenschap Innoveren & Ondernemen (VLAIO) and ICON https://www.imec-int.com/en/what-we-offer/research-portfolio/slogan

2. Project GANIC4S Monolith ic integration of GaN gate driver and power transistor switching functions under ESA Contract No.4000128515/19/NL/FE

All rights reserved, 2017, Thales Alenia Space