ESCC Capability Approval of a Mixed-Signal ASIC Supply Chain

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Abstract

For space applications a proven and qualified ASIC supply chain is an advantage in terms of development time and technical success.
IMST and Tesat-Spacecom are working together in a DLR funded R&D project on the establishment of a qualified Mixed-Signal ASIC supply chain for space applications. This project is aimed to achieve the capability approval for IMST as a qualified manufacturer given by the ESCC at the end of year 2021.
The capability domain covers the design, manufacturing, inspection, test procedure and screening of the ASIC together with a quality control and traceability procedure.
A first publication of the developed Mixed-Signal radiation hard IP library as the basis for the ASIC supply chain has been given on the AMICSA 2014 in CERN [1] and ESCCON 2019 [3]. First radiation test results and evaluation test results are presented on the AMICSA 2016 in Gothenburg [2].
In this publication the qualification phase will be presented together with an introduction of the capability domain in context to the released ESCC Detail Specification No. 9202/084: Integrated Circuits, Silicon Monolithic, CMOS, Mixed Signal ASIC based on a Rad-Hard XH018 IP Library [4].

I. Preface

The ASIC design is based on a qualified and Rad-Hard tested mixed-signal IP library called HARD Lib (Hard Against Radiation Design) with multiple library elements usable for a wide range of applications. The digital design flow supports a full custom design with standard cell libraries and a post-editing script for a triple mode redundancy implementation.

X-FAB serves as the semiconductor foundry in the supply chain and will support small to high volume wafer lots either on a single-mask set or for low quantities a MLM-set. For the assembly two sizes of a pre-qualified lead frame CQFP package are supported with 256 pins and 132 pins, respectively. The capability approval includes the full screening of the devices as well as qualification and periodic testing according ESCC9000.

With the described capability domain, a faster and more reliable ASIC development, with reduced development risk, can be offered compared to a single type ASIC design and qualification flow.

The evaluation test program according ESCC2269000 has been successfully finished. Chapter II describes the IP library elements and component variants from the detailed spec. In chapter IV the work and status of the qualification phase according ESCC2439000 capability approval testing is presented. Chapter V is concluding with the design flow of the supply chain.

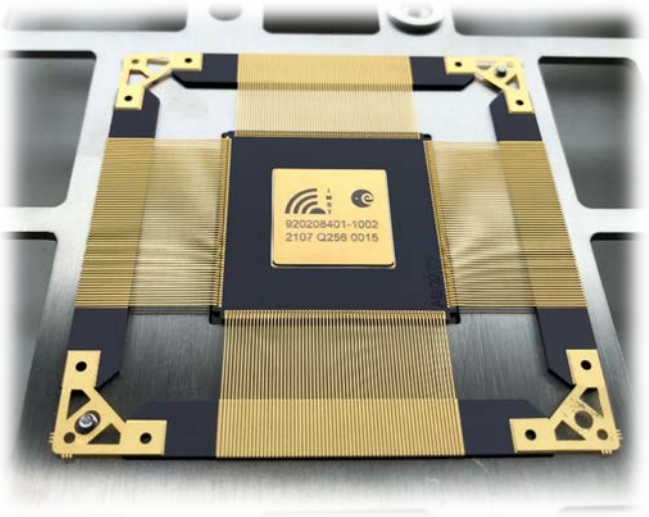

Figure 1: Photo of the assembled qualification device

II. HARD Library IPs and Component Variants

The IMST IP library is developed on XFABs XH018 technology and contains data converters, biasing cells, reconfigurable opamp, LVDS driver and receiver, SPI interface, OTP cells, clk PLL, oscillators and special I/O cells.

A list of IPs documented in the detail specification 9202/084 is shown in Table 1. Detailed descriptions of the IP library elements and test results on TID and SEE are available on request.

IP Group	IP Name	Function	IP Identific. Number
I/O Pads	pad_analog	Analog input and output pad	[IP_0_1]
	pad_tmr_out	Digital output pad	[IP_0_2]
	pad_tmr_in_out	Digital input and output pad	[IP_0_3]
	pad_lvds_in	LVDS input pad	[IP_0_4]
	pad_lvds_out	LVDS output pad	[IP_0_5]
Supply Pads	Pad_vdd_i	1.8V supply pad	[IP_1_1]
	Pad_vdd_o	5V supply pad	[IP_1_2]
	Pad_vdd_or	3.3V supply pad if no 5V is used	[IP_1_3]

IP Group	IP Name	Function	IP Identific. Number
	Pad_vdd_r	3.3V supply pad if 5V is used	[IP_1_4]
Ground and Substrate Pads	pad_gnd_all	Ground pad connecting all gnd rails	[IP_2_1]
	pad_gnd_i	Ground pad connecting i-rail	[IP_2_2]
	pad_gnd_or	Ground pad connecting or-rail	[IP_2_3]
	pad_substrate	Substrate pad	[IP_2_4]
Biasing and References	Bg_1v8	Bandgap reference for 1.8V supply	[IP_3_1]
	Bg_3v3	Bandgap reference for 3.3V supply	[IP_3_2]
	Refbiasgen_1v8	Current and voltage reference for 1.8V supply	[IP_3_3]
	refbiasgen_3v3	Current and voltage reference for 3.3V supply	[IP_3_4]
Data converter	Adc_sar_12b_222ks	12 bit analog to digital converter	[IP_5_1]
	Dac_12b_4mhz	12 bit digital to analog converter	[IP_5_2]
Frequency generation	Dcxo_5_50mhz	Crystal oscillator	[IP_6_1]
	Freq_gen_ring_0m6_to_600m	VCO with divider bank	[IP_6_2]
	Pll_frac_n	Fractional-n PLL	[IP_6_3]
	Loop_filter_325k	Integrated loop filter	[IP_6_4]
	Cml2cmos_alone	CML to CMOS converter	[IP_6_5]
	Cmos2cml_400u	CMOS to CML converter	[IP_6_6]
Analog circuits	Ldo_1v8_150m	LDO with 150 mA max. I out	[IP_7_1]
	Lvlshfthl (Note 1)	Analog level shifter from high to low	[IP_7_2]
	Lvlshftlh (Note 2)	Analog level shifter from low to high	[IP_7_3]
	Opv_multi_3v3	Multiple function operational amplifier	[IP_7_4]
	Tempsensor_ana_m40p150	Temperature sensor	[IP_7_5]
	Testmux33x4bit	Test multiplexer	[IP_7_6]
Memory	Otp_top	One time programmable ROM	[IP_8_1]
Control	Spi_shiftreg_tmr_tito	Register bank for SPI controller	[IP_9_1]
	Spi_refresh_tmr_tito	SPI controller	[IP_9_2]
	Lvlshft_tmr_1v8_3v3	Digital level shifter from 1.8V to 3.3V	[IP_9_3]
	Por_10u_porp_3u	Power on reset circuit	[IP_9_4]

Table 1: Summary of the HARD library elements

The ASIC can be ordered in two variant types as shown in Table 2. The HARD IPs have different radiation hardening because some IP elements are guaranteed with a TID of 300 kRAD(Si) and other IP elements are guaranteed with a TID of 100kRAD(Si). Therefore, the applicable Total Dose Radiation Level Letter for a specific ASIC design is defined by the used IP with the lowest Radiation Level Letter.

Variant Number	Case	Weight max g	Total Dose Radiation Level Letter
01	CQFN-256	11	A / R / no letter
02	CQFN-132_A	5.5	A / R / no letter

Table 2: Component type variants

III. Qualification Phase

A. *Development of the qualification device*

A representative ASIC has been developed to demonstrate the interaction of several IPs in a system together with a complex digital custom design. The largest die size of 10 X 10 mm^2 together with the package variant with the highest lead count of 256 pins has been chosen for the qualification phase. Figure **2** shows the block level schematic of an universal controller chip with analog and digital functionalities. The blue colored digital blocks are synthesized with standard digital cell libraries from XFAB with a triple mode redundancy scripting for hardening against SEEs.

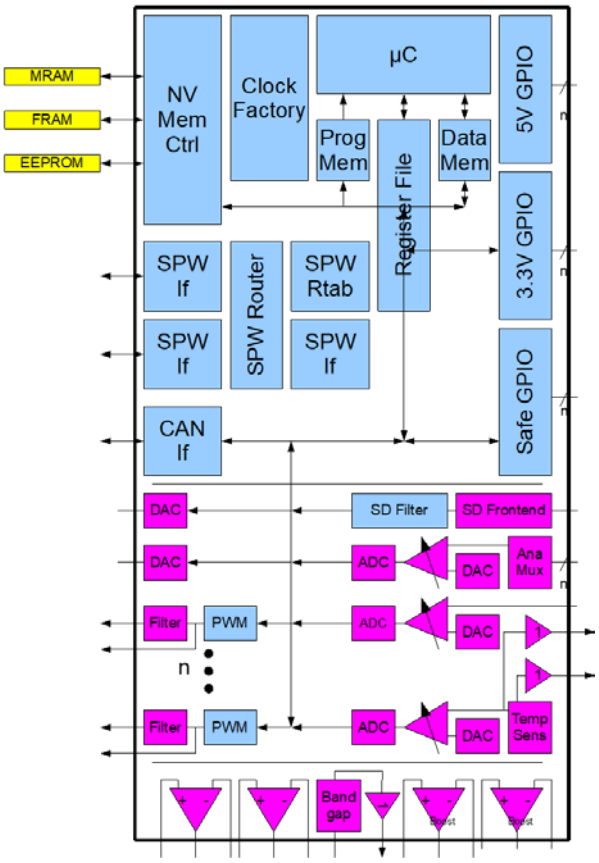

Figure 2: Qualification ASIC block level schematic: Universal Controller Chip

A digital on top design approach has been used for the layout of the qualification ASIC. For the analog IPs .lef files are available for the digital place and route tool as well as timing files. For the simulation of the analog IPs in a digital environment, VHDL models are coded for all IPs.

The test concept incorporates an analog test mux to make internal interfaces accessible for testing individual IPs as a single block, or in a smaller sub system. The digital design contains a scan chain and a JTAG controller. With the JTAG interface all analog circuits are controllable and digital outputs can be read back.

B. Production and assembly of the qualification device

A four-layer multi mask set on XH018 was used to produce a small wafer lot at XFAB. A diced wafer is assembled at the IMST wire bond facility and hermetically sealed by a subcontractor as defined in the capability domain. A chip photo of the wire bonded die is shown in Figure 3.

The capability approval testing flow chart in the ESCC2439000 requires 50 devices for environmental/mechanical subgroups together with the assembly- and endurance subgroup. In total 79 devices are assembled in one lot. Production control from chart F2A ESCC9000 has been applied for this qualification lot.

C. Screening of the qualification device

All devices are screened according to ESCC9000 chart F3A. Electrical tests are done at IMST site. In Figure 4 the test setup is shown with a thermal streamer to control the temperature. A Matlab GUI and test programme has been used to automate all tests in a sequence. The evaluation board contains a large switch matrix for the multiple analog interfaces and a FPGA to control it and to support the scan chain test and JTAG interface.

Mechanical tests are done by partner companies of IMST as a subcontractor within the capability domain.

The electrical tests have been passed without a lot failure. Seal test are currently running.

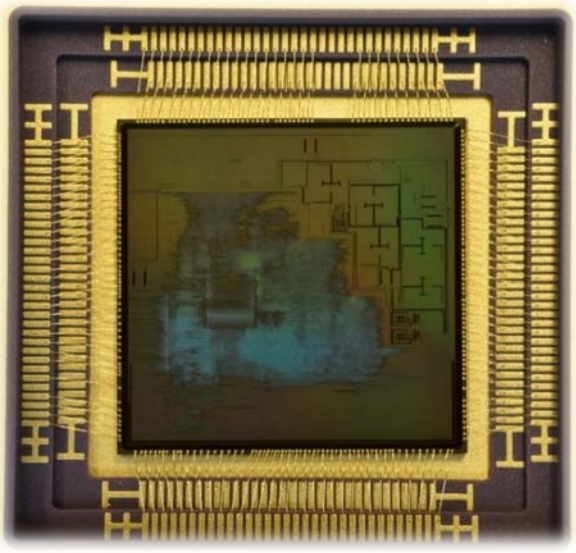

Figure 3: Assembled chip of the qualification device

D. Qualification testing of the qualification device

The qualification test phase has been started with the test flow chart from the ESCC2439000. The solderability test and terminal strength test has been passed and the 2000h operating life test is currently running. For the operating life test a FPGA controller board stimulates the 15 devices in the thermal test chamber with test pattern. The qualification device has an on-chip temperature sensor that can be read out to monitor the junction temperature. With the clock speed of the test pattern, the current consumption can be adjusted in that manner that the junction temperature is constant at 135°C with a constant 125°C environmental temperature as it is specified for the burn-in procedure in the detailed specification.

IV. ASIC SUPPLY CHAIN AND DESIGN FLOW

The design flow in the supply chain considers two different concepts: One is a turn-key design by IMST based on customer requirements, where IMST is doing the digital design and the top level of the ASIC with the mixed-signal IP elements.

If the customer wants to bring in own digital design IP the design flow supports a co-design with the customer where the customer is allowed to provide encrypted VHDL codes. For top level simulation together with analog IPs, the customer can use the provided VHDL models for the HARD library. IMST is doing the synthesis, implements TMR structures, scan chains and a JTAG controller in this case in order to guarantee a RadHard design with test functionality. Analog features are handled by IMST using the IP library and the whole ASIC will be placed and routed by IMST as well.

On either cases IMST delivers a tested, qualified and assembled RadHard ASIC.

A simplified flow chart of the supply chain is shown in Figure 5. Required wafer lot acceptance, lot verification or periodic testing are not shown in this chart, however considered in the process flow.

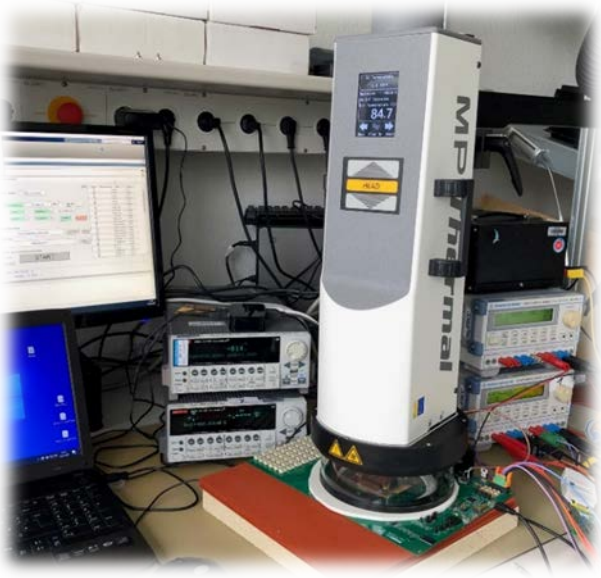

Figure 4: Screening tests: electrical measurement over temperature at IMST

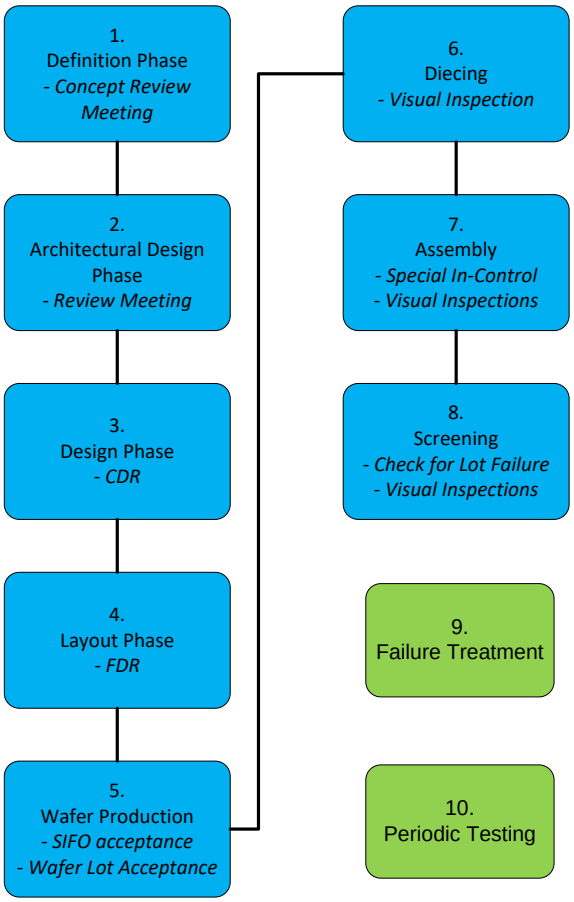

Figure 5: Simplified supply chain flow chart from ASIC definition to deliver after screening

For the quality assurance, the design and test phase are following the "Space product assurance - ASIC and FPGA development" described in the ECSS-Q-ST-60-02C.

V. Conclusion

This paper presented the ASIC supply chain documented in the detailed specification No. 9202/084 [4] and the status of the qualification. Technical issues delayed the project like outgassing and early aging of the adhesives, or expired shelf times of delivered pre-form lids e.g.. The root cause analysis and correction of the issues were time consuming, so that the project end needed to be delayed several times. The qualification time phase is now defined by the running operating life test until August 2021, so that a successful capability approval on the supply chain is expected to reach in Q4/2021.

VI. Acknowledgement

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VII. References

[1] J. Steinkamp, F. Henkel, V. Lück. 180nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain. AMICSA 2014

[2] J. Steinkamp, F. Henkel, V. Lück, H.-D. Herrmann Approval Process of an ESCC Qualified ASIC Supply Chain based on a Mixed-Signal IP Library. AMICSA 2016

[3] R. Wittmann, J. Steinkamp and F. Henkel, "Innovative, Mobile and Satellite Communications", European Space Component Conference (esccon 2019), Proceedings, Session 3 High-Performance Components, 11-13 March 2019, ESA-ESTEC, Noordwijk, Netherlands

[4] ESCC Detail Specification No. 9202/084 Issue1, Feb. 2020 https://escies.org/download/specdraftapppub?id=3829