DARE65 Phase-Locked Loop Design

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Abstract

This paper presents DARE65 Phase-Locked Loop (DARE65T_PLL) developed in the context of the ESA project. The DARE65T_PLL is implemented in a 65nm process, operating at 1.2V using a P-sub/Twin-well commercial CMOS technology. In 60MeV.cm^2/mg SET strike condition, this radiation-hardened PLL guarantees less than 280ps of clock period fluctuation from the nominal clock period that is 833.333ps (=1.2GHz) and double-edge free. Also, the guard-ring achieves TID and SEL mitigation up to the maximum 100krad and 70MeV.cm^2/mg, respectively.

I. Overview of DARE65T_PLL

The DARE65 Phase-Locked Loop (DARE65T_PLL) is composed of a Voltage-Controlled Oscillator (VCO) based on a ring oscillator, a programmable Charge-Pump (CP) synchronized with a loop divider, a Phase Frequency Detector (PFD) and a 2nd order Low Pass Filter (LPF). Besides the loop, there are three more sub-circuits in the PLL: an input divider, an output divider, and a lock detector. Figure 1 shows the block diagram of the DARE65T_PLL.

As a radiation-hardened PLL, the DARE65T_PLL is implemented with several radiation-hardening techniques. These techniques have been applied sub-block by sub-block in the PLL. Details of radiation-hardened sub-blocks will be explained in Chapter II, III, and IV.

II. Voltage-Controlled Oscillator (VCO)

The VCO consists of the voltage-to-current converter and the inverter-based ring oscillator. The radiation-hardening techniques are separately applied for these two sub-blocks because the voltage-to-current convert is an analogue circuit, but the ring oscillator is a digital circuit.

The voltage-to-current converter is implemented with the averaging-by-redundancy technique. The voltage-to-current converter is a current mirror to generate the current for the ring-oscillator's power supply and the amount of the current is proportional to the input control voltage (VCTRL). The current mirror is split by identical three units, which is the averaging-by-redundancy as shown in

Figure 2. If the V_{G1} has a voltage fluctuation by an SET strike, I_{D1} is fluctuated but I_{D2} and I_{D3} maintain their nominal current values. The amount of the current fluctuation is suppressed with a factor of 3. In an extreme case, although the V_{G1} goes to AVDD1V2 by a SET strike and no current flows on I_{D1} branch, the ring oscillator is still able to receive the 2/3 of the nominal current.
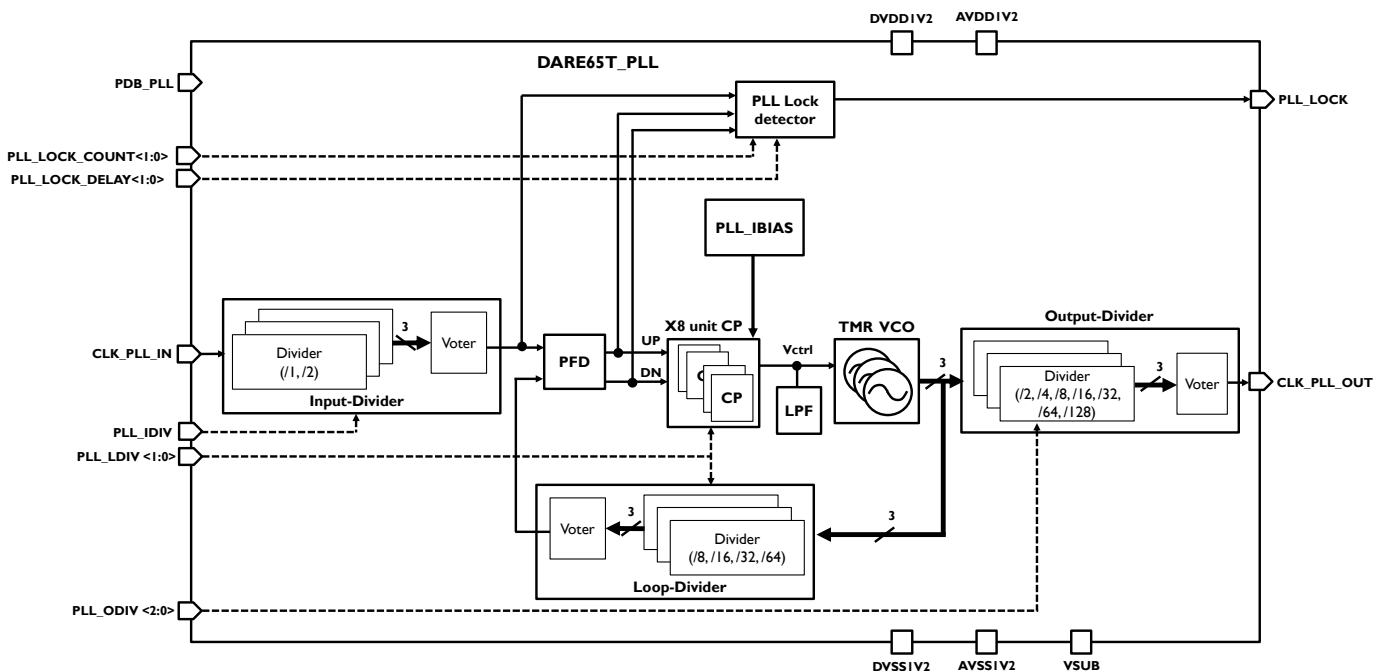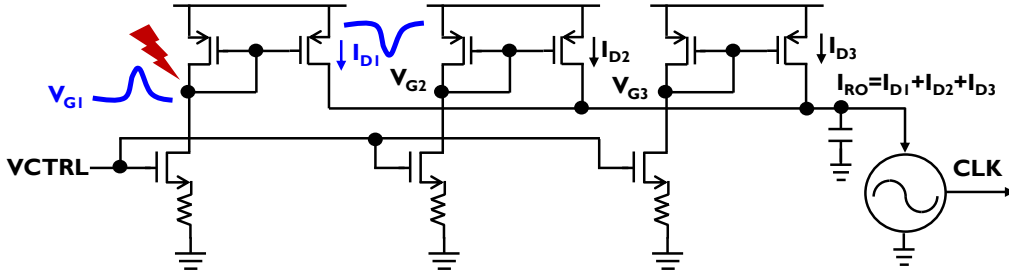

Figure 1: *Block diagram of DARE65T_PLL*

Figure 2: *Averaging-by-redundancy for VCO*

The ring oscillator employs the Triple Modular Redundancy (TMR) for radiation-hardening, which consists of three ring oscillators and three C-elements-based voters as shown in Figure 3. Those three voters are used for synchronizing the three ring oscillators when the PLL is settling, and clock perturbation occurs. If one of three VCO outputs generates a perturbed clock period by a SET strike, the voter in the output divider (ODIV) and the loop divider (LDIV) creates a correct clock at their outputs. For this radiation-hardening strategy, the ODIV and LDIV are

Figure 3: *TMR-based ring oscillator*

implemented with TMR technique.

III.   Charge-Pump (CP) & Low Pass Filter (LPF)

The CP requires to prevent a voltage fluctuation at the output because its output is the input of the VCO (=VCTRL) and the VCO's output frequency is changed by the fluctuation. A SET strike at the switch connecting to the CP output (SW1 & SW2) is the critical case which creates the

aforementioned voltage fluctuation. As a radiation-hardening technique, a series resistor is added at the CP output to attenuate the SET-caused fluctuations on VCTRL as shown in Figure 4.

In the LPF, radiation-hardening is unnecessary. It is implemented with MOSFET capacitor, MOM capacitor, and poly-salicide resistor. The MOM capacitor and the poly-salicide resistor have no active region (=diffusion) to collect charges by a SET strike while the MOSFET capacitor has active regions. Nevertheless, its active regions and the well are connected to the ground node in this PLL design. Thus, a SET strike on this MOSFET capacitor is unable to cause any charge collection in the active regions.

IV.   Phase-Frequency Detector (PFD) & Dividers (IDIV, LDIV, ODIV)

The PFD uses radiation-hardened digital cells that have strong driving strength. Compared to dividers, the PFD state-machine is too complex to use the TMR technique. The TMR-based state-machine needs an additional circuit to correct a corrupted state from a SET strike. Due to the complexity, the TMR-based PFD leads to more area overhead and design cost.

Three dividers, which are the input divider (IDIV), LDIV, and ODIV, are implemented with the TMR technique. Every divider includes three identical dividers, a re-synchronization circuit for the three dividers, and a voter as shown in Figure 5. The re-synchronization circuit is essential because these dividers are state machines. Figure 6 shows the purpose of the re-synchronization circuit. Once one of those three state machine experiences a change of state by an SET strike, the divider still generates correct clocks at the output
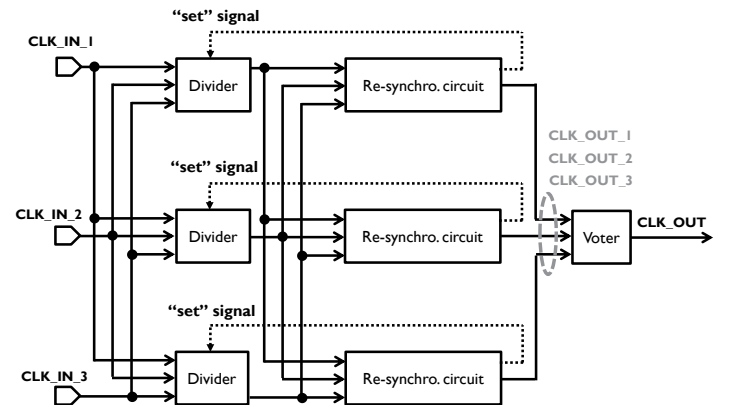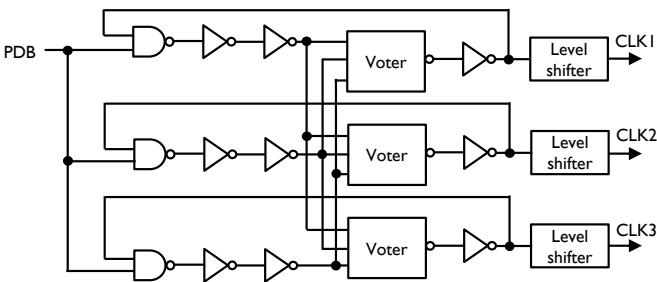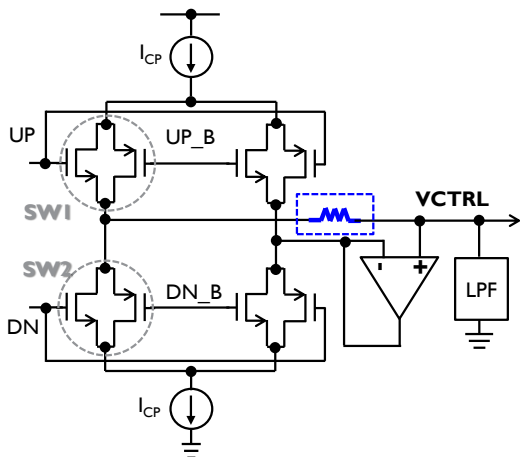

Figure 5: *CP with a series resistor*
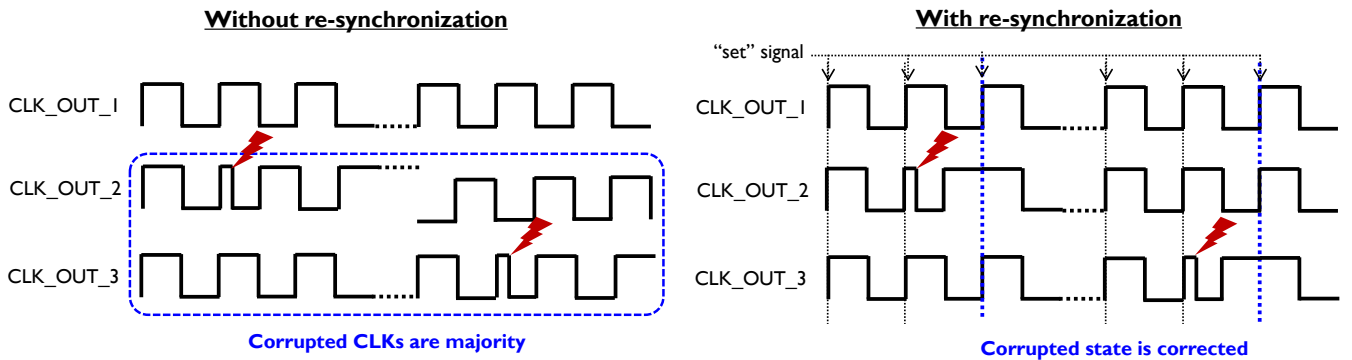

Figure 4: *TMR-based divider*

Figure 6: *Purpose of the re-synchronization circuit*

due to the voter. Without the re-synchronization, the corrupted state remains and eventually the corrupted states will become the majority of the voter's inputs when one of the others has an SET strike. To avoid this problem, the re-synchronization circuit creates set signals and applies to the three identical dividers at every rising edge of the output clock of the dividers. As a result, the corrupted state is corrected by the set signals on every clock period. The voters also need to be protected from an SET strike, otherwise the output clock will be suffered by glitches. For voters, the large size transistors are used to ensure high driving strength and suppress the glitches by SET strikes.

V.   Layout

The previous chapters presented mainly SET-hardening techniques. In DARE65T_PLL, not only the SET-hardening but also TID and SEL-hardenings are required to mitigate up to 100krad and 70MeV.cm^2/mg, respectively. The TID effect for the gate oxide almost disappears under 180nm process due to the tunneling effect. Nevertheless, the oxide for Shallow Trench Isolation (STI) is still thick enough to have the TID effect in the 65nm process. In the TID hardening point of view, the design with a 65nm process needs to consider the inter-device leakage, which is inducted by parasitic n-channel under the STI. The consequence of the parasitic n-channel is that two different devices get shorted. To mitigate the TID-induced leakage current, guard-rings are inserted around the NMOS transistors because the p+ guard-ring prevents to induce the parasitic n-channel. Also, the guard-ring mitigates SEL, which makes the gain of latch-up loop lower.

VI.   Summary

The PLL guarantees less than 280ps of timing error, which is the amount of output clock period fluctuation comparing to nominal clock period, caused by a 60MeV.cm^2/mg SET strike. This timing error is verified for a 1.2GHz output clock, meaning that the rising edge of the output clock experiences 280ps of shift during the 833.333ps period. The output divider can be programmed to 1, 2, 4, 8, 16, 32, 64, and 128 of division ratio and the VCO has 800MHz – 1.2GHz output frequency range. Due to these circuit performances, users can obtain a wide-range of SET-immune clock signal from the DARE65T_PLL: 6.25MHz – 1.2GHz. Its radiation test is in preparation and the PLL will be validated by radiation tests soon. Table 1 shows the summary of DARE65T_PLL's performance.

Table 1: *DARE65T_PLL performance*

Process	65nm bulk CMOS twin well
Supply voltage	1.2V
Input clock frequency	20-100MHz
Output clock frequency	6.25-1200MHz
VCO frequency	800-1200MHz
Jitter	< 15ps
Timing error @ 60MeV.cm^2/mg	< 280ps for 833.333ps
TID mitigation level	< 100krad
SEL threshold	70MeV.cm^2/mg
Operating current	3.7mA