Concept Design and Realization of the Next Generation Magnetometer Front-End ASIC

To date most of the front-end implementations for spaceborne fluxgate magnetometers are built using a mix of discrete components and multiple integrated circuits. The MFA-3 (Magnetometer front-end ASIC) initiated a first step towards miniaturization, integrating parts of the whole front-end electronics on a single chip [1]. This ASIC is based on an outdated process technology and offers a small measurement range. A further drawback is the limited radiation hardness against single event effects. Since the requirements on sensor front-ends that are used in satellites are rising, performance and miniaturization are key elements. Further radiation hardness and power efficiency are also essential development goals. Therefore, it is crucial to improve the required functionality and integrate it on a single chip. This work describes the design of the next generation front-end ASIC for spaceborne fluxgate magnetometers. This upcoming ASIC is built using a technology with a smaller process node. Further the dynamic range should be increased up to 65000 nT.

Fluxgate magnetometers are used to measure the magnetic field. They are made of a soft magnetic ring core and different types of excitation, feedback and sense windings. The excitation coil periodically saturates the soft magnetic ring core at a fundamental frequency of several kHz. The output signal of the sense coil contains odd and even harmonics of the fundamental drive frequency. The even harmonics are proportional to the external magnetic field along the magnetic axis of the sensor. The odd harmonics result from the feed-through signal coupled from the excitation coil and the soft magnetic core to the sense coil. The forward path of the front-end ASIC has to perform the extraction of the magnetic field information by translating the even harmonics into a slowly changing output voltage according to the bandwidth of the magnetometer. Then digital signal processing is used to calculate a feedback signal that is used to compensate the ambient magnetic field. This compensation is done by the feedback path, that creates a loop formed by an additional feedback coil hereby extending the linearity and measurement range of the magnetometer. The feedback path consists of a high resolution DAC (digital-to-analog converter) that controls the feedback coil driver. This coil driver must provide highly linear currents of up to 20 mA to compensate the ambient magnetic field. The feedback path is required to have a dynamic range of up to 20 bits depending on the mission scenario. To achieve a higher dynamic range than the space qualified predecessor MFA-3 (Magnetometer front-end ASIC) new concepts for the feedback path have been evaluated. The forward path consists of a low-noise amplifier and a medium-resolution analog-to-digital converter. The forward path is currently in the concept phase.

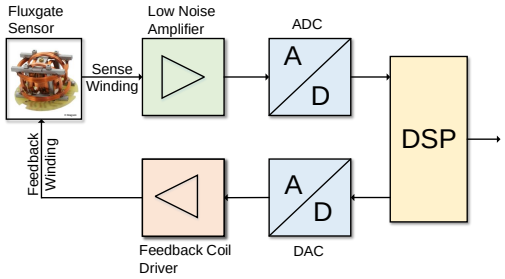

Fig. 1. Block diagram of the next generation magnetometer front-end ASIC, showing the different blocks of the forward and the feedback path.

To evaluate different concepts two test chips have been designed and fabricated. The first test chip contains a configurable high-resolution DAC. This DAC is composed of a two-stage Delta-Sigma-modulator that uses a current steering DAC in the final D/A stage. The second test chip contains another high-resolution DAC based on a single-bit D/A-cell realized using a chopped current-steering cell and a circuitry to drive the feedback coil. Further a dedicated block to monitor the system conditions was implemented on chip. To increase the radiation hardness different techniques have been used. The first test chip was hardened by design, taking the degradation mechanisms of different transistor types into account. The second test chip was hardened by the use of guard rings to reduce latch-up events. The overall goal is to achieve a TID (Total Ionizing Dose) immunity of more than 300 krad and improve SEL (Single Event Latch-up) up to 50 MeV-cm²/mg. Both test chips are currently in an evaluation phase. Depending on the outcome of the evaluation phase the concepts will be adapted and implemented on the final ASIC. The final front-end ASIC should be able to readout and drive a 3-axis fluxgate sensor. It then contains the forward path and the feedback path for each axis (x-y-z) as well as a system monitoring block. First measurements results based on the proposed concepts as well as a brief outlook of the upcoming MFA development is intended to be shown at the AMICSA.

References

[1] W. Magnes, M. Oberst, A. Valavanoglou, H. Hauer, C. Hagen, I. Jernej, H. Neubauer, W. Baumjohann, D. Pierce, J. Means, and P Falkner, "Highly integrated front-end electronics for spaceborne fluxgate sensors," *Measurement Science and Technology*, vol. 19, no. 11, p. 115 801, 2008.