Integration of two High-Performance Mixed-Signal Data Conversion IPs

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***Abstract*—This brief presents the experience of integrating two high-performance Data Converter IPs, an ADC and a DAC, in a single rad-hard test-chip. A system-level perspective is taken, underlining the importance of Design-for-Testability (DfT) structures and tuning structures for debugging purposes and achieving first-time right silicon. Modeling the interactions between domains (PCB, package, analog and digital) is also highlighted as a key to success, particularly for high performance circuits operating at the limits of technology.**

I. System Description

The system implemented in the test-chip is depicted in Fig.1. It contains two converters, a pipeline ADC and a current-steering DAC nominally designed for $2V_{pp}$ Full-Scale, $15b$ resolution, $100MS/s$, both with foreground calibration [1], [2]. These two IP blocks consist of a full-custom analog core with special design rules for radiation hardening and a digital section implemented in the rad-hard DARE library [3], in a standard $0.18\mu m$ CMOS technology. In addition, some peripheral circuitry is added, namely: a bandgap block, a low-jitter custom clock receiver circuitry to convert the LVDS external clock to CMOS and a digital wrapper to properly interface the SPI buses of the two IPs and cope with the pin count limitation. For the same reason of pin count limitations, both the ADC and the DAC IOs are provided in DDR mode. The pad ring and LVDS IOs are supplied at 3.3V while the IPs operate at 1.8V.

In order to enable debugging and diagnosis, as well as to provide mitigation path in case of subsystem failures, a number of Design-for-Testability features have been introduced in the design:

- Bandgap by-passing capability. A dedicated pad is used to input an externally generated voltage. In addition, this pad can be used to monitor the internal bandgap voltage when the external generation is disabled.
- An analog test bus is implemented to monitor critical signals at system level or in the pipeline ADC: the full-scale references, the common-mode voltages for the different amplifiers, the output of intermediate pipeline stages, etc.
- A multiplexer is also implemented to allow the ADC input signal to be directly sent to the input of any pipeline stage.
- The biasing sections can rely on the bandgap voltage (internal or external) but also eventually on an external current reference, which removes the feedback loop introduced by a current conveyor.
- The calibration registers of the ADC and the DAC can be externally read and written, which allows error monitoring and external calibration.
- The calibration sequence for the IPs can be split in separated modes to identify issues.
- Both for the ADC and the DAC IPs, several master clock options are multiplexed. For instance, the SPI clock pin could eventually serve as a CMOS clock input for the ADC and/or the DAC in case of complete failure of the clock receiver.
- An internal temperature sensor has been implemented.
- A subsystem based on a ring-oscillator to identify process corner is also available.

Similarly, in order to enable first-time-right integration, tuning capabilities are a must. Indeed, designing close to the technology limits does not allow to take large design guard-bands and there is a risk of approaching the accuracy limits of the models provided in the PDK. For that reason, most calibration registers, both in the ADC and the DAC have been oversized with respect to the variation range observed in the process and mismatch Monte Carlo simulations. As well, the bias conditions in both IPs can be significantly altered.

The DAC operating current can be altered by $\pm 25\%$ through the programmability of a biasing resistor. As well, the internal output load resistors can also be altered in the same amount to maintain the Full-Scale output voltage to a constant level.

For the ADC, which is architecturally much more complex than the DAC, the list of trimming is much larger: the biasing currents of the two-stage op-amps, the biasing current of the common-mode buffers, the reference levels, the biasing current of the reference buffers,the delays in the non-overlapping phase generator and the calibration DAC current.

For the peripheral circuitry, the biasing of the clock receiver can also be trimmed.

II. Integration

With respect to the integration of the IPs into a practical testchip, the realistic modeling of the package parasitics is fundamental to the design of an adequate damping network for the power supply noise. The inductance (and mutual inductance) associated to the wire bonds and to the package lids greatly degrade the performance of the IPs, essentially due to the highly dynamic supply current profiles. Indeed, the pipeline ADC is a switched capacitor circuit, and while the major current contribution of the Current-Steering DAC is

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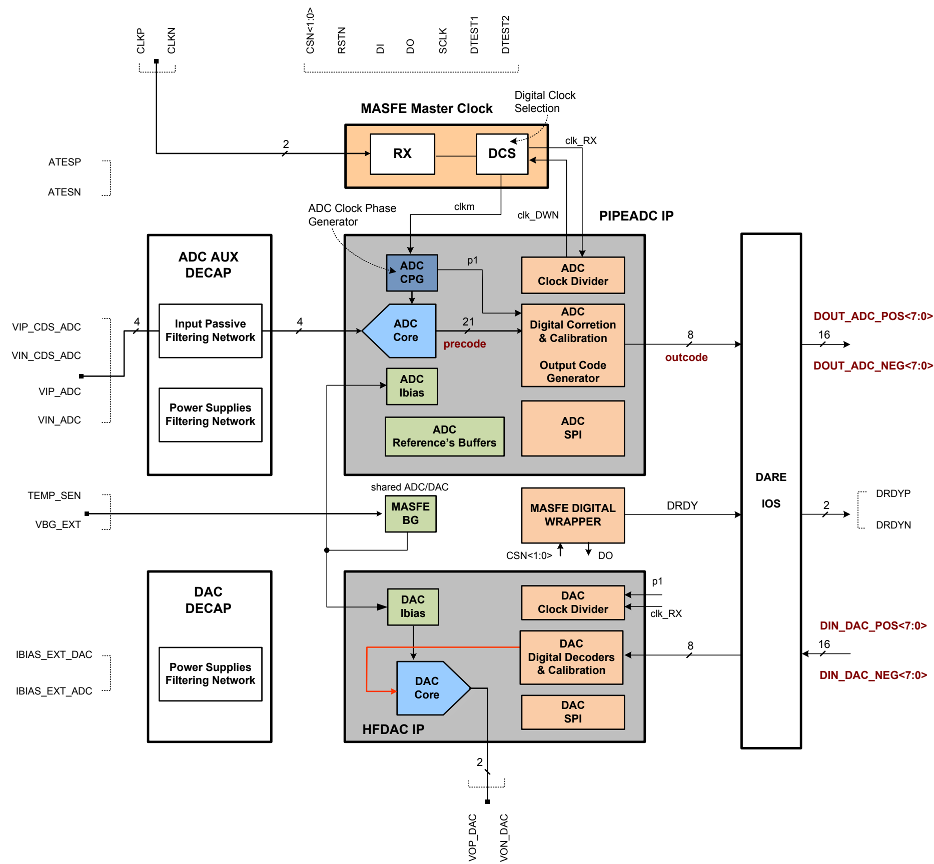

Fig. 1. Simplified system-level diagram.

static, the fast switching scheme necessary to reach 100MS/s still consumes a significant amount of power. In our case, a package with exposed pad was mandatory since it greatly reduces the inductance associated to the ground and at the same time lowers the pin count of the test-chip and thus enables a smaller package with smaller wire bonds and lids for the rest of the pins. For the final test-chip design, a QFN100 package was selected.

As an example, a simulation of the pipeline ADC core in a QFN100 package (with exposed pad) showed that, in the absence of damping network, the effective number of bits would be reduced from 12.5bits (at schematic level, without considering package parasitics) to only 5bits. Similarly, for the DAC the SNDR for a sine-wave of 5MHz at 100MS/s would fall from 78.5dB (13 effective bits) to 59dB (below 10 effective bits).

Even with a damping network, the impact of inductive parasitics appears clearly, as illustrated in Figure 2. It displays a close-in of the DAC differential output with a damping network optimized for the QFN100 package. Three curves are displayed which correspond to three mutplying factors applied to the inductances in the package model. It comes that these perturbations do not significantly alter the performance of the DAC in terms of ENOB because their impact is located beyond the first Nyquist zone. However, for the sake of reliability, it is preferable to limit the amplitude of the oscillations.

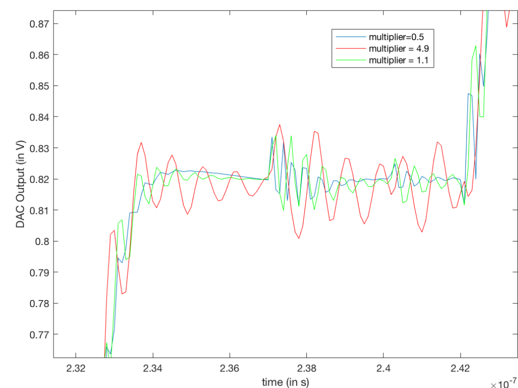

Fig. 2. DAC differential output for an implementation in a QFN100 package with an optimized damping network. Three multiplying factors are considered for the inductances.

To increase signal integrity for that package model and noise immunity between analog and digital sections, several sections in the pad ring have been considered:

- Power domains for the analog mixed-signal section of the ADC IP: analog , mixed-signal, clock phases, and DC reference section. The analog DfT bus is contained in the mixed signal section of the ring.

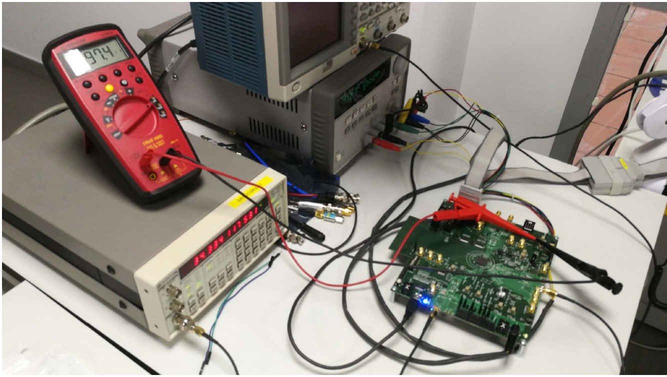

Fig. 3. Photo of the test setup

- Power domain for the DAC.
- Power domain for the clock receiver.
- Power domain for the bandgap.
- A single section for the 1.8V domain for the IPs core and 3.3V for the DARE I/O pads.

The distinction between these power domains has been also done in the internal distribution of the power and ground signals. Due to feasibility constrains in the number sections, some of the domains in the core (for instance reference buffers and op-amp power domains) are joined together in the pad ring. To reduce noise coupling between sub-sections, a star signal distribution has been considered, performing the connection as close to the pads as possible. The analysis of signal integrity should also consider with care the contribution of the package and bonding parasitics. Due to the great cavity of the selected package, the parasitics associated to the bonding become quite significant. To reduce this contribution, double and triple bounding to the same pin have been considered. The total area of the optimized decoupling networks is greater than $5mm^2$.

III. Experimental Results

The designed test-chip has been successfully fabricated and is currently being tested at our facilities as illustrated in Fig. 3. Preliminary results are very promising and validate our design strategy.

Noticeably, some of the tuning knobs have had to be set to a value out of the range predicted by the process and mismatch Monte-Carlo simulations which exemplifies the limits of the simulation-based approach when dealing with technology limits.

As an example of the obtained results in nominal conditions, Fig.4 shows the effective number of bits of the ADC at a sampling frequency of 61MS/s, for an input signal of almost full-scale at 2.71MHz. It can be seen that an effective resolution of almost 12bits is obtained.

As well, Fig.5 shows the output spectrum of the DAC, as obtained by the spectrum analyzer, after calibration operating at 100MS/s and for an output sine-wave of about 10MHz at Full-Scale. A THD above 75dB is obtained.

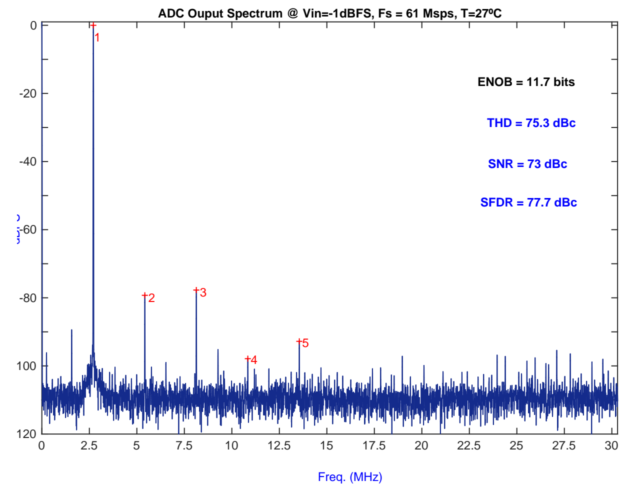

Fig. 4. Output spectrum of the ADC for a 2.71MHz input sine-wave, at 61MS/s

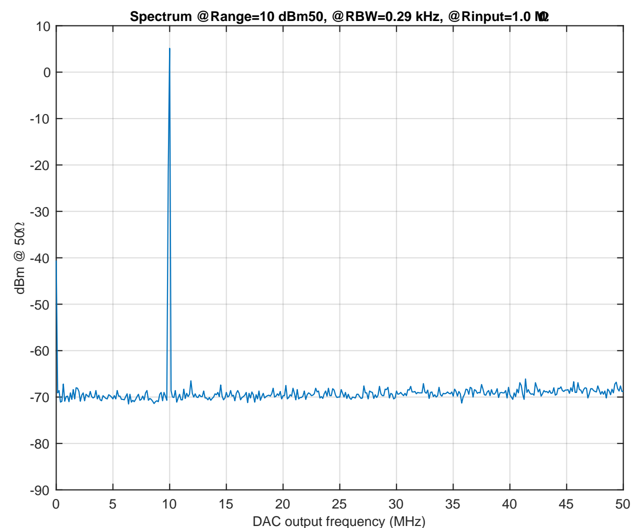

Fig. 5. Output spectrum of the calibrated DAC operating at 100MS/s, for a full-scale sine-wave of 10MHz

Acknowledgment

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