Applicability of FinFET Technologies for Space Applications

Dan Alexandrescu. Maximilien Glorieux, Vincent Correas, Issam Nofal
IROC Technologies, Grenoble, France
name.surname@iroctech.com

David Levacq
ESTEC ESA
Noordwijk, The Netherlands
David.Levacq@esa.int

As soon as FinFET technology was shown to be a viable alternative to planar technology for nodes lower than 28nm, the radiation community has begun tests to characterize available technology from manufacturers such as Intel, Samsung, Global Foundries, TSMC and radiation testing and service providers [1][2][3][4]. A reduced SEE sensitivity has been observed due to lower carrier collection in the FinFET structure. TID effects are qualitatively similar to planar technology with a small threshold voltage shift and an increase of subthreshold current and STI induced leakage current. As FinFET are majority carriers displacement damage is not anticipated to be important. But Single Defect or Defect Clusters induced by protons or heavy ions in a nuclear collision may be important to consider in 12nm technology. The influence of a single defect depends upon its position in the channel and may modify the electrical characteristics of a single FinFET.

To elaborate on these aspects, this paper will include a global survey of radiation effects on FinFET technology. The synthesis of available results published in selected reviews (Nuclear Science, …), published in conferences (NSREC, RADECS, IRPS, SELSE..) or other public sources will present the sensitivity to total ionizing dose (TID), displacement damage (DD) and single event effects (SEE).

SEE EFFECTS

As an example, the SEE evaluation of the Kintex Ultrascale+ FPGA from XILINX (manufactured with TSMC's 16nm FinFET process) promises a good behavior regarding SEE :

For 64 MeV protons the sensitivity per bit is given below [5][6][7]

ZU9EG CRAM	ZU9EG BRAM
3.3 E-16	1 E-15

For Heavy ions [5][6][7] have tested Kintex Ultrascale+ under heavy ions and obtained cross-section versus LET . At high LET cross-sections are given below:

Flip-Flop (per Flip-Flop)	1E-8
BRAM (per bit)	2E-9

However, SEL [8] was observed with a relatively high cross section of 2E-3 on power supplies VccAux=1.8V and VccINT=0.85V. The origin of this sensitivity is probably related to the small depth of the STI in FinEFT technologies and should be investigated further.

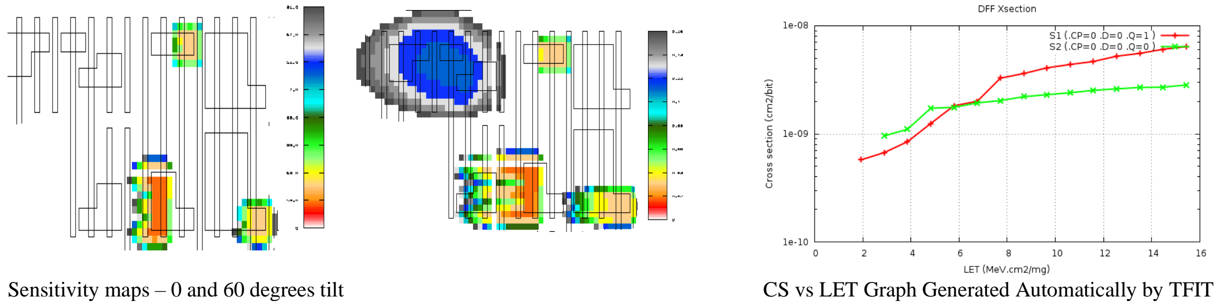
TID EFFECTS

For Global Foundry 14nm, King et al [9] has studied TID effects on FinFET transistors, SRAM cells and Ring Oscillators for high and low Vth transistors showing only small variation of Ioff below 100krad. IdsOn/Idsoff ratio is reduced from 1E6 at D=0 to 1E2-1E3 at 1 Mrad. Worst case bias conditions are identified. High threshold voltage devices show a smaller response linked to differences in process.[1]

The available results seem to suggest that FinFET technologies are a good match to the requirements of space applications. However, many of the studies focus on the ground-level reliability, relevant for today's industry's hot

[1] This work is supported by the ESA Contract No. 4000128352/19/NL/GLC = Definition of Radiation Effects Mitigation Techniques for Ultra-Deep Submicron Technologies

topics such as automotive. The evaluation of the SEE effects in harsh environments dominated by heavy ions or protons is complicated by the particular 3-D structure of the FinFET cells and the fine-grained sensitive device volumes. The paper will present simulation and analysis methods and tool frameworks that can accurately predict SEE performance for complex cells. Particularly, State-of-the-Art (SOTA) EDA frameworks working at TCAD or transistor-level abstraction levels can produce a very exhaustive picture of the device weaknesses and strengths for analog, digital or mixed-mode designs: cross-section of internal cell transistors with a very fine spatial granularity for each possible state of the cell, particle characteristics and impact angle and so on.



Sensitivity maps – 0 and 60 degrees tilt

CS vs LET Graph Generated Automatically by TFIT

In [10], authors from TSMC show a remarkable correlation of test results and simulations for their 16nm FinFET process:

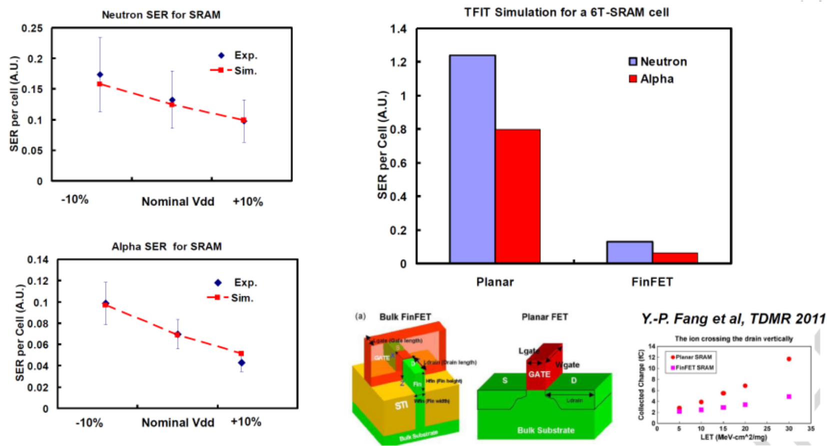


FIGURE 1. CORRELATION OF TEST AND SIMULATION RESULTS IN TSMC 16NM FINFET

This correlation is valid for any type of events, including MCUs:

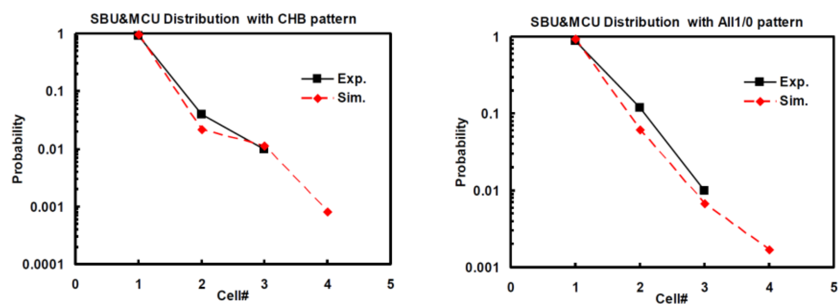


FIGURE 2. TEST VS SIMULATION FOR SBU/MCU IN TSMC 16NM FINFET

Not only TSMC authors have shown a very good correlation of simulation results with actual radiation testing results. [11] presents a very exhaustive validation of simulation tools used with Samsung's 14nm FinFET process who was later licensed by GlobalFoundries and evolved to the current GF's 12nm process.

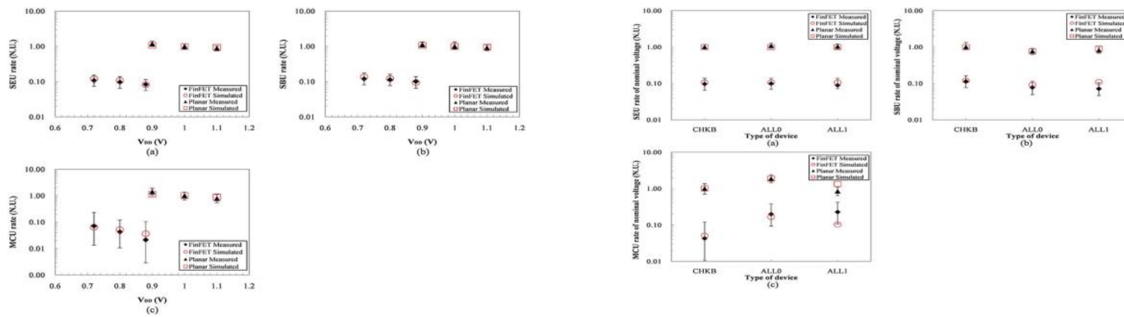


Figure 3. Simulation Validation for Samsung's 14nm FinFET

TSMC is also using the simulation tool for SEE studies in advanced nodes, beyond 16nm. A very recent study by TSMC's authors and published at IRPS 2018 shows how simulation is able to help the SEE evaluation of 16, 10 and 7nm process nodes.

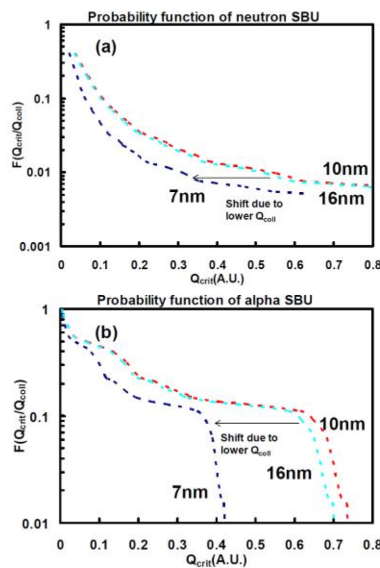


Figure 6. (a) Simulated probability functions of terrestrial high-energy neutrons for 7nm, 10nm, and 16nm. The function is shift to lower or higher Q_{crit} due to different Q_{coll} in different SRAMs. (b) Simulated probability function of an Am-241 alpha source. The simulated probability functions were performed by T-FIT [16].

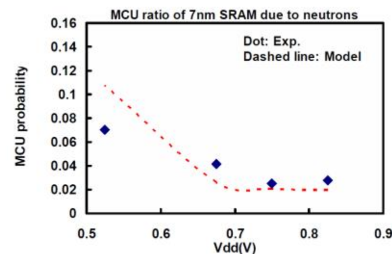


Figure 7. Neutron induced MCU probability (MCU/total error events) of 7nm SRAM as a function of Vdd compared to modeled MCU ratio.

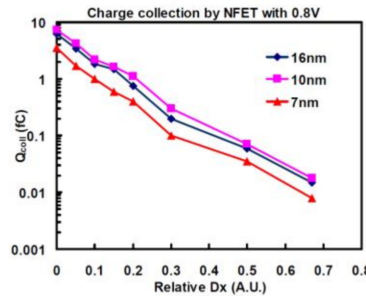


Figure 8. Simulated Q_{coll} as a function of Dx for 16nm, 10nm, and 7nm SRAM. Dx is the distance between strike location of an heavy ion with LET of 150fC/um and the drain edge of NFET in the SRAM along BL or WL direction. The operation voltage of SRAMs is set to 0.8V.

Figure 4. Simulation in 16nm, 10nm and 7nm Process Nodes

Experimental and simulation results can provide invaluable, actionable data that can be used effectively during the hardening phase of the selected technologies or libraries. In addition to non-destructive Single Event Transient/Upset analysis and hardening, a special consideration will be provided to Single Event Latch-ups as previous tests on the UltraScale+ FPGA shown that this type of event can significantly affect the behaviour of devices implemented on FinFET nodes.

In conclusion, FinFET technologies show a great promise for space applications, provided that their behavior is well studied and critical SEE events such as SELs are managed.

[1] Yi-Pin Fang, Anthony S. Oates, Kader Belhaddad, Vincent Correas, Issam Nofal and Olivier Lauzeral, "Neutron and Alpha Soft Error Rate Simulations for Memory and Logic Devices at Advanced Technologies", SELSE 2013

[2] Yi-Pin Fang and A. S. Oates, "Cell Level Soft Error Rate Simulations of Planar and FinFET Processes", TSMC OIP, 2014

[3] Jinhyun Noh, Vincent Correas, Soonyoung Lee, Jongsung Jeon, Issam Nofal, Jacques Cerba, Hafnaoui Belhaddad, Dan Alexandrescu, YoungKeun Lee, and Steve Kwon, "Study of Neutron Soft Error Rate (SER) Sensitivity: Investigation of Upset Mechanisms by Comparative Simulation of FinFET and Planar MOSFET SRAMs", IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 62, NO. 4, AUGUST 2015

[4] Y. Fang and A. S. Oates, "Soft errors in 7nm FinFET SRAMs with integrated fan-out packaging," *2018 IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA, 2018, pp. 4C.2-1-4C.2-5.

[5] David S. Lee, Michael King, William Evans, Matthew Cannon, Andrés Pérez-Celis, Jordan Anderson, Michael Wirthlin, William Rice, "Single-Event Characterization of 16 nm FinFET Xilinx UltraScale+ Devices with Heavy Ion and Neutron Irradiation"

[6] Pierre Maillard, Member, IEEE, Michael Hart, Member, IEEE, Jeff Barton, Jue Arver, Christina Smith, Member, IEEE, "Neutron, 64 MeV proton & alpha single-event characterization of Xilinx 16nm FinFET Zynq® UltraScale+™ MPSoC"

[7] Thomas LANGE, Maximilien GLORIEUX, Adrian EVANS, A Duong IN, Thierry BONNOIT, Dan ALEXANDRESCU, iRoC Technologies France, Cesar BOATELLA POLO, Carlos URBINA ORTEGA, Veronique FERLET, CAVROIS, ESA/ESTEC, Netherlands, Maris TALI, Ruben GARCIA ALIA, CERN Switzerland/France, « Single Event Characterization of a Xilinx UltraScale + MP SoC FPGA", SEFUW 2018

[8] Glorieux, Maximilien & Evans, Adrian & Lange, Thomas & In, A-Duong & Alexandrescu, Dan & Boatella-Polo, Cesar & Alia, Ruben & Tali, Maris & Urbina Ortega, Carlos & Kastriotou, Maria & Fernández-Martínez, Pablo & Ferlet-Cavrois, Veronique. (2018). Single-Event Characterization of Xilinx UltraScale+ ® MPSOC under Standard and Ultra-High Energy Heavy-Ion Irradiation. 1-5. 10.1109/NSREC.2018.8584296.

[9] M. P. King, Member, IEEE, X. Wu, M. Eller, S. Samavedam, M. R. Shaneyfelt, Fellow, IEEE, A. I. Silva, B. L. Draper, W. C. Rice, T. L. Meisenheimer, J. A. Felix, E. X. Zhang, Senior Member, IEEE, T. D. Haeffner, Member, IEEE, D. R. Ball, Member, IEEE, K. J. Shetler, M. L. Alles, Member, IEEE, J. S. Kauppila, Member, IEEE, and L. W. Massengill, Fellow, IEEE, "Analysis of TID Process, Geometry, and Bias Condition Dependence in 14-nm FinFETs and Implications for RF and SRAM

[10] Yi-Pin Fang and A. S. Oates, "Cell Level Soft Error Rate Simulations of Planar and FinFET Processes", TSMC OIP, 2014

[11] Jinhyun Noh, Vincent Correas, Soonyoung Lee, Jongsung Jeon, Issam Nofal, Jacques Cerba, Hafnaoui Belhaddad, Dan Alexandrescu, YoungKeun Lee, and Steve Kwon, "Study of Neutron Soft Error Rate (SER) Sensitivity: Investigation of Upset Mechanisms by Comparative Simulation of FinFET and Planar MOSFET SRAMs", IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 62, NO. 4, AUGUST 2015

[12] Y. Fang and A. S. Oates, "Soft errors in 7nm FinFET SRAMs with integrated fan-out packaging," *2018 IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA, 2018, pp. 4C.2-1-4C.2-5.