Content
Content

• Introduction
• LUCA test chip
• Luca principle and architecture
• Main switch and current control
• Protecting dependent supply domains
• Controlling thresholds
• Power management of LUCA
• Digital interface
• LUCA layout
• Conclusion
What is LUCA?

• Analog and mixed-mode radiation tolerant ASIC
• Control the supply of a load
  o Detects over-current event (short cut...)
  o Detects latch-up event (high and low threshold)
  o Detects over-voltage conditions
• Up to 2A, 0.8 to 10V supply voltage, low voltage drop
What is LUCA?

• Telemetry through SPI interface
  o OBC control and telemetry
  o But can also be used without SPI

• Can be daisy chained
  o Several supply domains can be linked

• XFab XT-018 process
LUCA radiation tolerant

- Radiation tolerance of load protection circuitry

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Ionization Dose</td>
<td>MIL-STD-883 method 1019</td>
<td>300</td>
<td>krad (Si)</td>
</tr>
<tr>
<td>SEL and SEU immunity</td>
<td>ESA-ESCC-25100</td>
<td>62.5</td>
<td>MeV cm$^2$/mg</td>
</tr>
<tr>
<td>SEB and SEGR immunity</td>
<td>MIL-STD-750-1 method 1080</td>
<td>62.5</td>
<td>MeV cm$^2$/mg</td>
</tr>
<tr>
<td>SET immunity</td>
<td>ESA-ESCC-25100</td>
<td>62.5</td>
<td>MeV cm$^2$/mg</td>
</tr>
</tbody>
</table>
LUCA radiation tolerant

- Radiation tolerance of telemetry circuitry

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Ionization Dose</td>
<td>MIL-STD-883 method 1019</td>
<td>300</td>
<td>krad (Si)</td>
</tr>
<tr>
<td>SEL and SEU immunity</td>
<td>ESA-ESCC-25100</td>
<td>62.5</td>
<td>MeV cm$^2$/mg</td>
</tr>
<tr>
<td>SEB and SEGR immunity</td>
<td>MIL-STD-750-1 method 1080</td>
<td>62.5</td>
<td>MeV cm$^2$/mg</td>
</tr>
<tr>
<td>SET immunity</td>
<td>ESA-ESCC-25100</td>
<td>TBD</td>
<td>MeV cm$^2$/mg</td>
</tr>
</tbody>
</table>
LUCA test chip
LUCA testchip top level layout

- Main Switch
- Digital test 1
- Digital test 2
- OTP tests
- Bandgaps
LUCA test chip results

• XT-018 is a SOI process, 0.18µm lithography
  o Natural SEL resilience (following some layout rules)
• 300krad TID
  o Core CMOS transistors ➔ as expected
  o Higher voltage CMOS transistors ➔ some expected deviation ➔ modelized
• SET as expected
  o SET and SEU resilience of the digital core cells demonstrated
  o Test chip was tested up to 300krad TID and 62.5 $\frac{\text{MeV cm}^2}{\text{mg}}$ SEE
LUCA test chip results

• More information on SEE/TID tolerance is obtained
  o TID/SEE tolerance of some analog blocks
    ▪ Bandgap (3 different structures tried)
    ▪ Bias circuits
    ▪ Main switch (SEB/SEGR)
    ▪ Control of the main switch
    ▪ Charge pump (SEGR)
    ▪ OTP programming
    ▪ Digital cells
LUCA principle and architecture
Luca principle
Luca architecture

• More detailed
Main switch and current control
Main switch and current control
• LUCA has:
  o Three different programmable current thresholds
  o One current limitation threshold
Main switch operation modes

• OFF state: when the load is not powered
• Linear low voltage drop mode:
  o When the current is lower than current limitation threshold
  o Low dissipation of power (low Ron)
• Current limitation mode:
  o When the current limitation is reached
  o Main switch becomes more resistive!
• All these modes are:
  o Monitored
  o Controlled by a state machine
Current limitation and protection during “showtime”

- **Latch-up condition**

  ![Diagram](image)

  The load is shutdown after some (programmable) delay
Current limitation and protection during “showtime”

- **Short “glitch” condition**

  ![Graph](image)

  - Current limitation
  - Excessive current threshold
  - Latch-up threshold
  - Nominal value

  - $t_{LU}$
  - $t_{RESTART}$
  - $t_{START}$

  - Too short to be a latch-up
  - Noise in the supply is “filtered”
  - Current reaches high limit → Immediate shutdown
• Accumulating (micro latch-up) conditions
High or low latch-up threshold

Switching between high and low latch-up current threshold is controlled by hardware (HILO pin)
Current detection and limitation during start-up

→ latch-up and excessive current detection is masked during the start procedure
Protection controlled by a state machine

(simplified view)
Protection controlled by a state machine

(simplified view)
Protection controlled by a state machine

- Stand-by
  - Load unpowered
  - EN pin = 0
  - Auto-start = 1
- Start procedure
  - Load is powered
  - Detections disabled
- Shut-down load
  - Auto-restart = 0
  - EN pin = 1
  - Wait "start-up" time
  - Over-voltage condition
- Possible latch-up
  - Latch-up limit reached
  - Latch-up limit not reached
- Monitoring mode
  - Detections enabled

(simplified view)
Main switch and current control

The Main Switch is layout:
- to equalize power dissipation across silicon area
- to sustain 10V voltage and 2A current
- to select of the Ron resistivity (7Ω to 50mΩ)
- to maintain voltage drop in the specified range
Main switch and current control

Main Switch radiation hardening and tolerance:

- Implemented using 10V NMOS device
- TID tolerance tested on the Luca Testchip
- $R_{on}$ and current limitation compensated
  - temperature variation
  - TID deviation by the same regulation loop
- Variation of $R_{on}$ over 300krad is < 2.5%
- In off state, the leakage increase over 300krad stays limited
- Leakage current is sink to ground, not to the load
Protecting dependent supply domains
Daisy-chaining LUCAs: one example

Start-up sequence 1 → 2 → 3

PWRGD = 1 when the supply is stable
Controlling thresholds
Controlling thresholds: with/without OBC
Controlling thresholds: with/without OBC

- Principle schematic

- TOV: over-voltage (low precision). Relates to absolute value $R_{TOV}$
- TXC: excessive current threshold
- TLU$_H$: latch-up current threshold high
- TLU$_L$: latch-up current threshold low

- DR: delay restart
- DS: delay start procedure
- DOV: delay over-voltage
- DLU: delay latch-up
Controlling thresholds: with/without OBC

• Principle schematic

- TID tolerance by proper design of current sources
- SET tolerance by redundant measurements
- Precision on TOV is ± 5%
- Precision on other values is ± 1%
Controlling thresholds: with/without OBC

- LUCA does not need an OBC to be used and programmed
  - "Stand-alone" version → 28 pins
  - Can be still over-written by OBC
  - Resistor omitted → default value in register
  - Redundancy or "safe" mode if OBC is out-of-order
Controlling thresholds: with/without OBC

• In case control by OBC is performed
  o Do not equip the resistors (or use the 20 pins LUCA)
  o Power-up LUCA
  o Program the right threshold
  o Rise enable pin (EN)
Power management of LUCA
Power management allows two supply schemes

Supply by the IN pins if IN > 4V and VDD < 3V

Supply by the VDD pin HAS PRIORITY if VDD > 3V
Power management allows two supply schemes

• Principle

- Bandgap is TID tolerant, LDO too
- SET tolerance by proper design
Digital interface
• SET tolerant SPI interface and logic
• SEU free control registers
• Cold spare IOs → allow to leave unpowered LUCA connected to the SPI bus
SPI interface

• One command is 24b:
  o 8b address
  o 8b data
  o 8b CRC check

• SET tolerance of the SPI interface
  o Obtained by repetition of the message
  o “Redundant” signaling
  o CRC check
• Cold spare IOs
  o Allow some redundant LUCAs in power down mode
Digital library: SEU Resilient D-Flipflop

- Latches used to construct the master and slave parts of FFs are based on triple-interlocked latches
- Resilient to multiple simultaneous particle strikes
- Added SET/SEU resilient reset circuitry

Digital library

• Library has been made synthesizable
  o Automatic timing characterization
  o Description under the Liberty format available
  o Synthesis with various synthesis tools

• Library has been designed placeable and routable
  o LEF abstracts available
  o Placed and routed with Innovus
LUCA layout
LUCA top level layout
Current status
Current status

• Current status
  o First layout tape-out January 2020
  o First silicon dies received January 2021
  o Packaging first engineering samples done March 2021
  o Evaluation and characterization started

• Next steps
  o First characterized devices expected in September 2021
  o First engineering samples can be ordered by September 2021
  o Radiation tolerance characterized by end 2021
Conclusion
Conclusion

• Test chip to assess radiation tolerance
  o of elementary devices
  o of analog blocks
  o of digital library

• Controlled and monitored current. Different phases

• Can be used with or without OBC

• Daisy chaining with priority scheme

• Two possible supply schemes

• SET resilient SPI interface and SEU free digital control
Contributors

• Designed by nSilition AMS IC design team
  o Alessandro Michielin
  o Drahoslav Lím
  o Quentin Wala
  o Thierry Delmot

• Specified in collaboration with ESTEC
  o Giorgio Magistrati
  o Richard Jansen

Any questions?