AMICSA 2021

# LUCA: a Dynamic Latch-up Current Protection ASIC

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# Content

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- LUCA test chip
- Luca principle and architecture
- Main switch and current control
- Protecting dependent supply domains
- Controlling thresholds
- Power management of LUCA
- Digital interface
- LUCA layout
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# Introduction

# What is LUCA?

- Analog and mixed-mode radiation tolerant ASIC
- Control the supply of a load
  - Detects over-current event (short cut…)
  - Detects latch-up event (high and low threshold)
  - Detects over-voltage conditions
- Up to 2A, 0.8 to 10V supply voltage, low voltage drop

# What is LUCA?

- Telemetry through SPI interface
  - OBC control and telemetry
  - But can also be used without SPI
- Can be daisy chained
  - Several supply domains can be linked
- XFAB XT-018 process

# LUCA radiation tolerant

- Radiation tolerance of load protection circuitry

| Parameter | Conditions | Min. | Unit |
|---|---|---|---|
| Total Ionization Dose | MIL-STD-883 method 1019 | 300 | krad (Si) |
| SEL and SEU immunity | ESA-ESCC-25100 | 62.5 | $\frac{\mathrm{MeV\,cm^2}}{\mathrm{mg}}$ |
| SEB and SEGR immunity | MIL-STD-750-1 method 1080 | 62.5 | $\frac{\mathrm{MeV\,cm^2}}{\mathrm{mg}}$ |
| SET immunity | ESA-ESCC-25100 | 62.5 | $\frac{\mathrm{MeV\,cm^2}}{\mathrm{mg}}$ |

# LUCA radiation tolerant

- Radiation tolerance of telemetry circuitry

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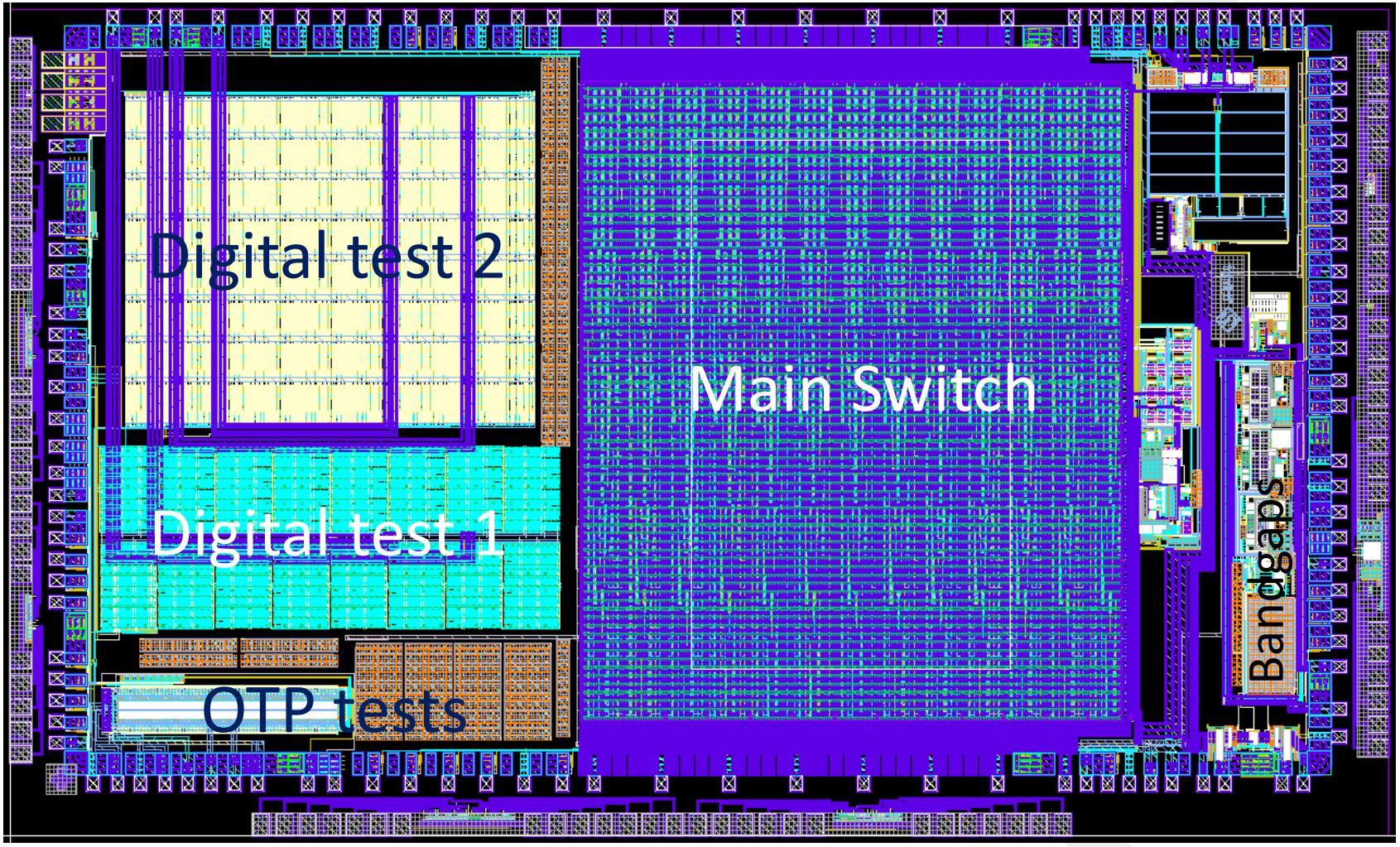
# LUCA test chip

# LUCA testchip top level layout



# LUCA test chip results

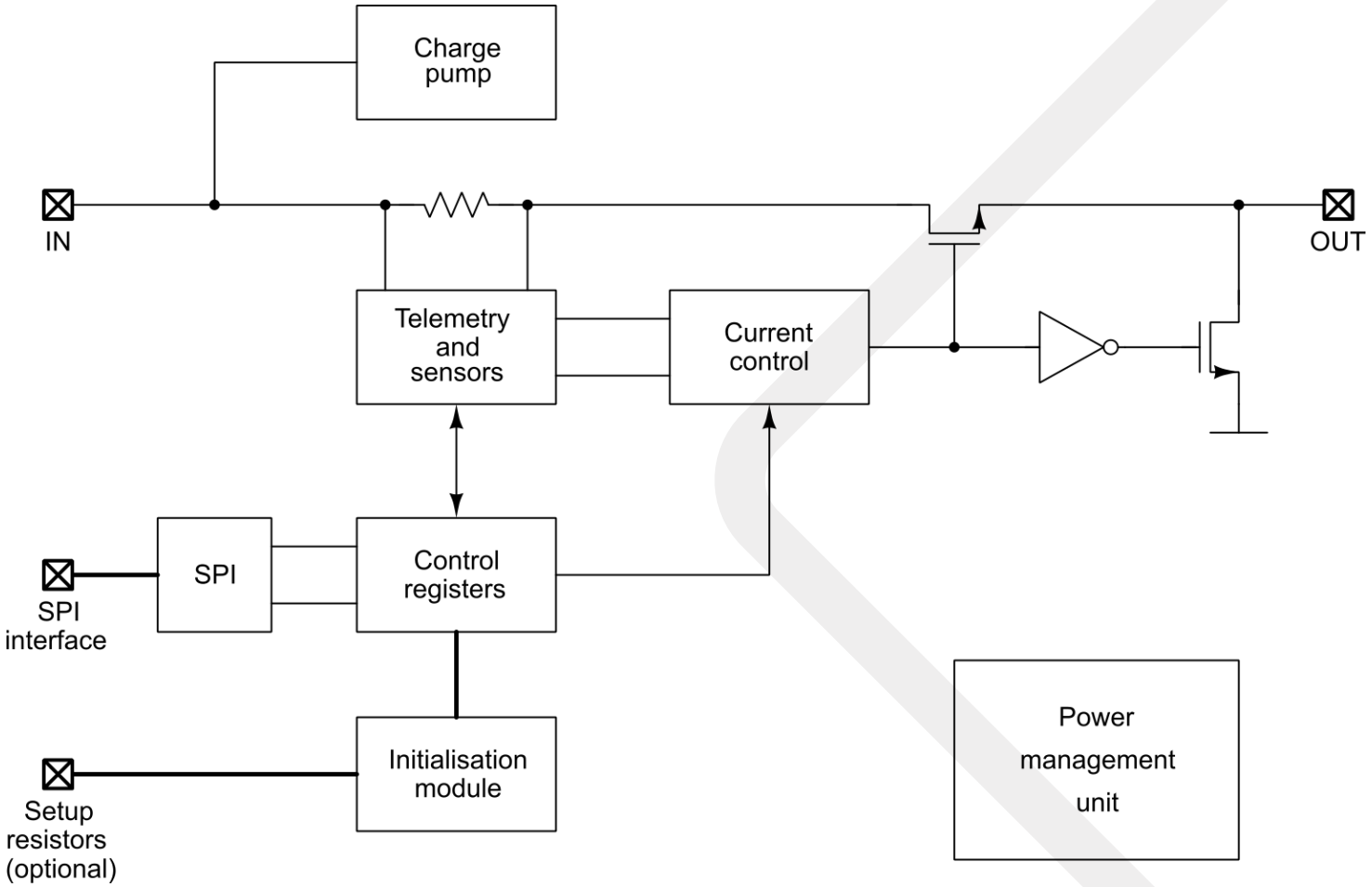
- XT-018 is a SOI process, 0.18µm lithography
  - Natural SEL resilience (following some layout rules)
- 300krad TID
  - Core CMOS transistors ➔ as expected
  - Higher voltage CMOS transistors ➔ some expected deviation ➔ modelized
- SET as expected
  - SET and SEU resilience of the digital core cells demonstrated
  - Test chip was tested up to 300krad TID and 62.5 $\frac{\mathrm{MeV\,cm^2}}{\mathrm{mg}}$ SEE

# LUCA test chip results

- More information on SEE/TID tolerance is obtained
  - TID/SEE tolerance of some analog blocks
    - Bandgap (3 different structures tried)
    - Bias circuits
    - Main switch (SEB/SEGR)
    - Control of the main switch
    - Charge pump (SEGR)
    - OTP programming
    - Digital cells

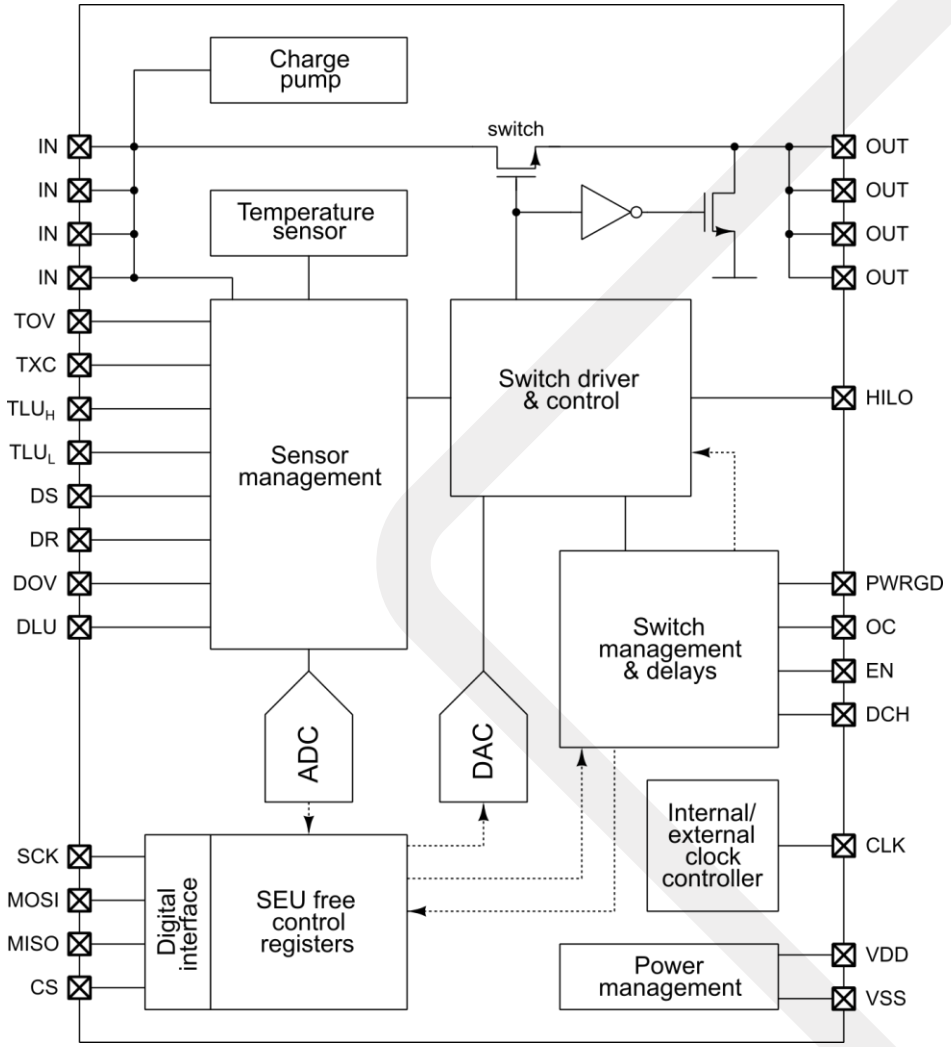
# LUCA principle and architecture

# Luca principle



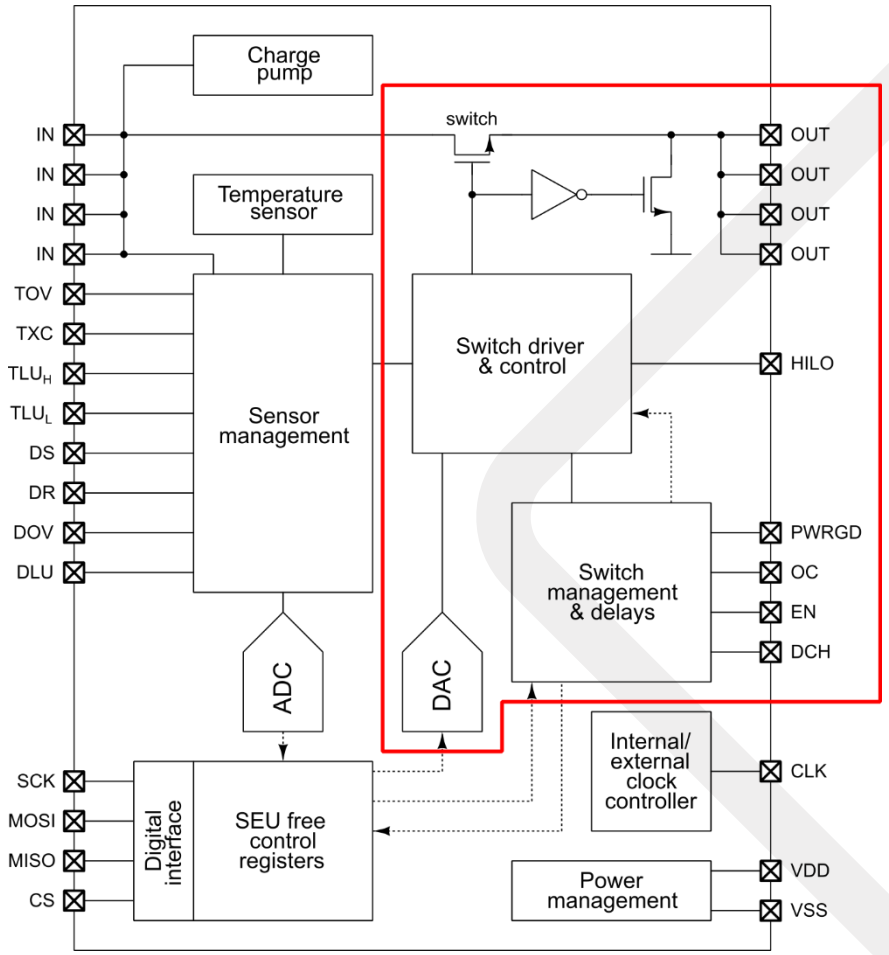
# Luca architecture

- More detailed



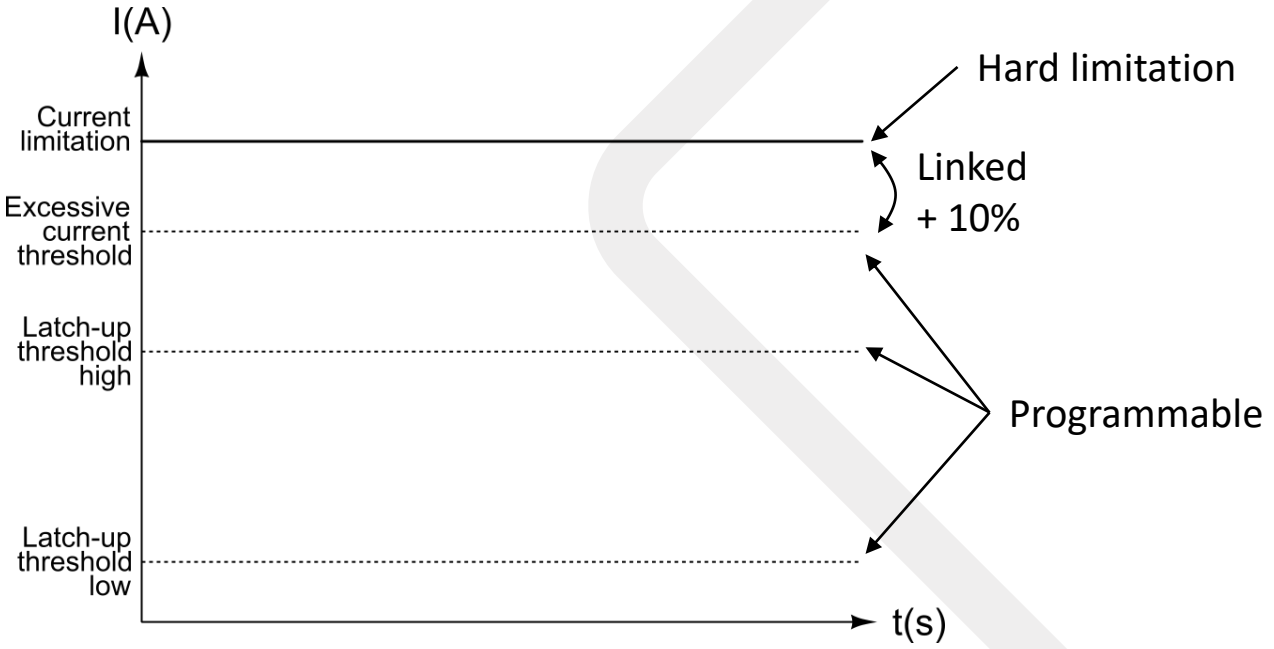
# Main switch and current control

# Main switch and current control



# Current thresholds

- LUCA has:
  - Three different programmable current thresholds
  - One current limitation threshold

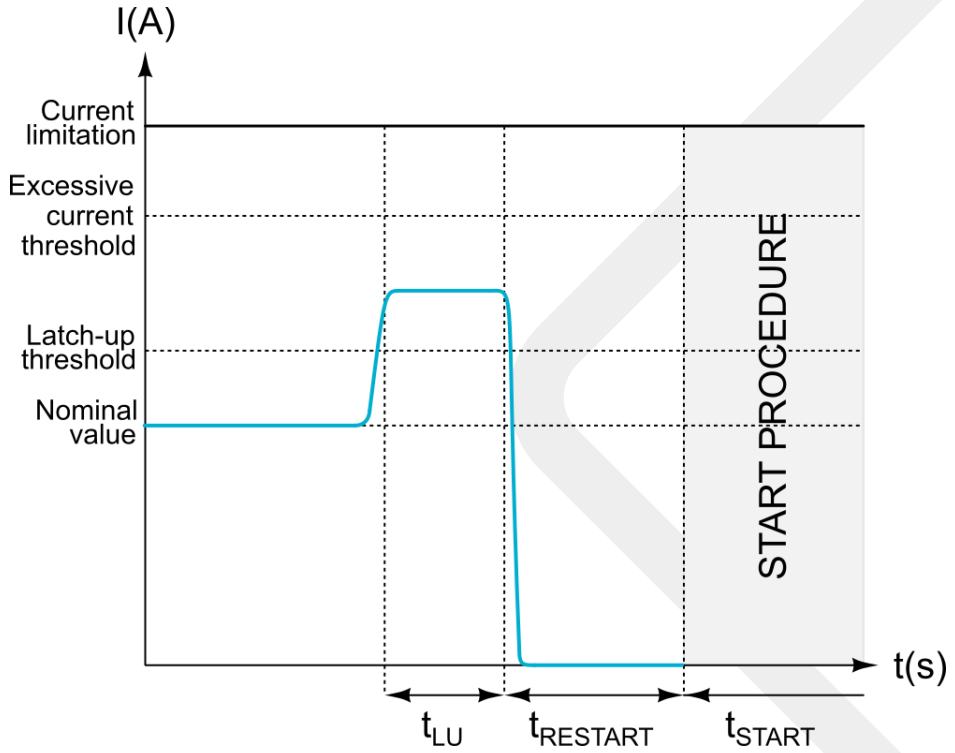


# Main switch operation modes

- OFF state: when the load is not powered
- Linear low voltage drop mode:
  - When the current is lower than current limitation threshold
  - Low dissipation of power (low Ron)
- Current limitation mode:
  - When the current limitation is reached
  - Main switch becomes more resistive!
- All these modes are:
  - Monitored
  - Controlled by a state machine

# Current limitation and protection during “showtime”

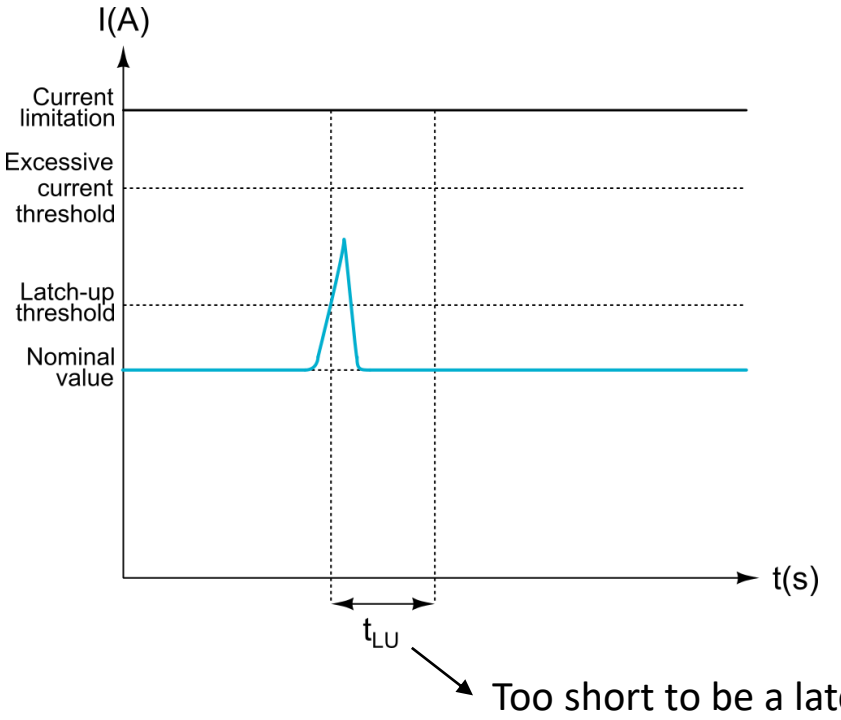
- Latch-up condition



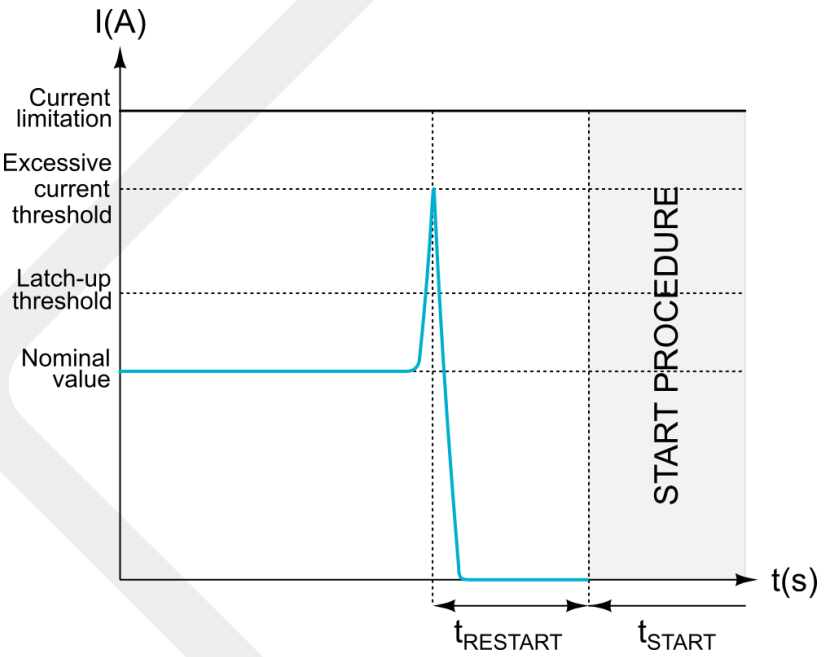

The load is shutdown after some (programmable) delay

# Current limitation and protection during “showtime”

- Short “glitch” condition



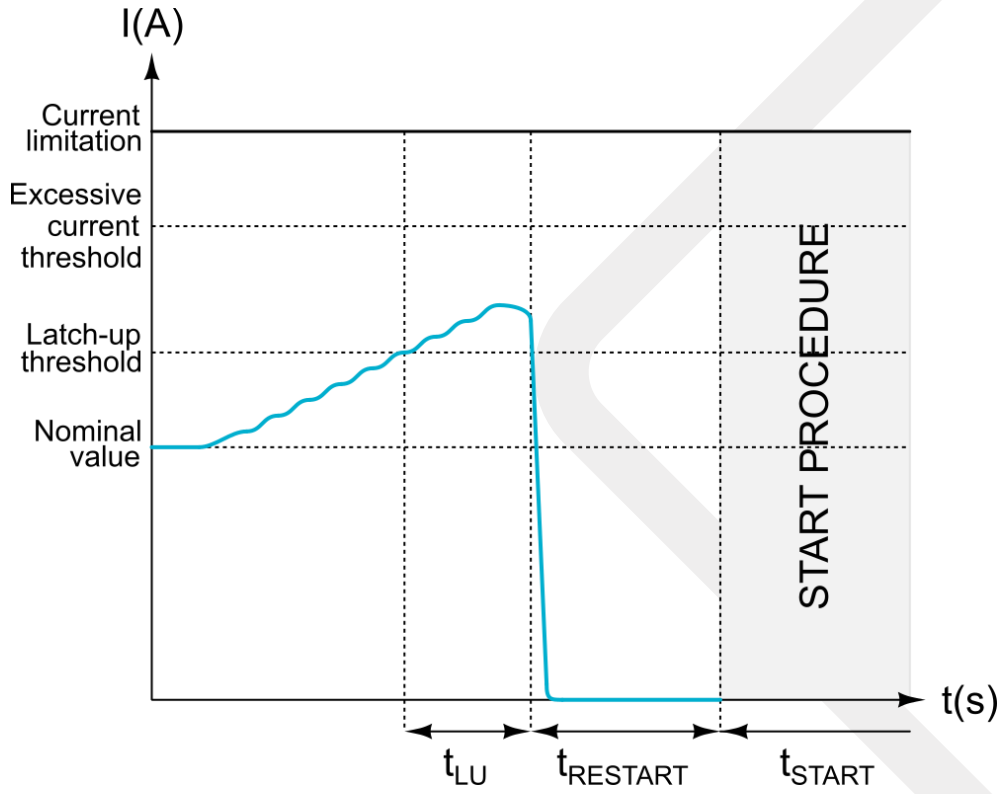

Noise in the supply is “filtered”



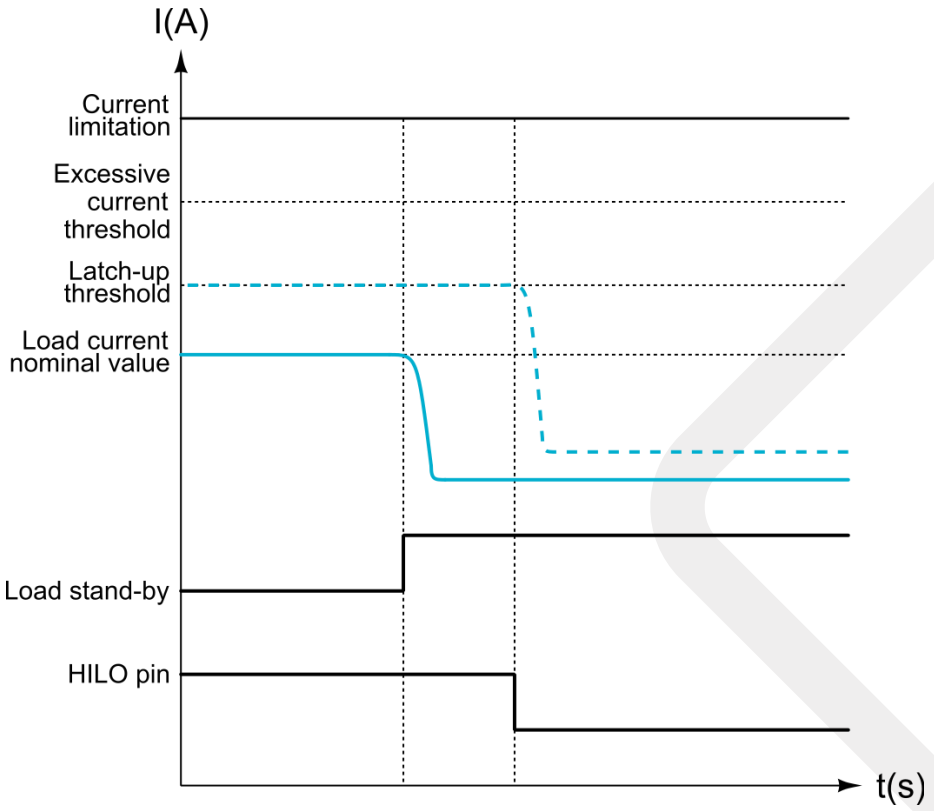

Current reaches high limit
→ Immediate shutdown

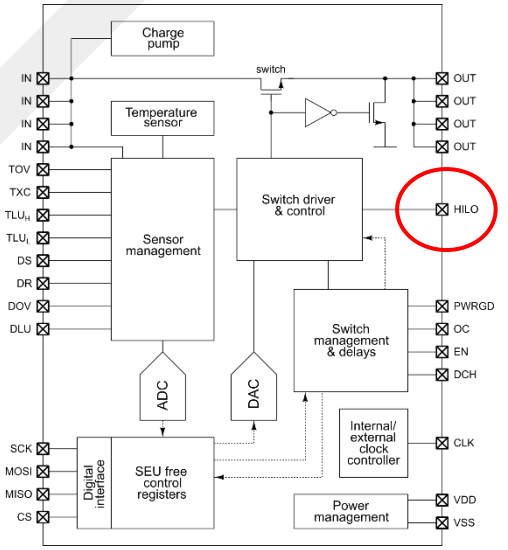
# Current limitation and protection during “showtime”

- Accumulating (micro latch-up) conditions



# High or low latch-up threshold




Switching between high and low latch-up current threshold is controlled by hardware (HILO pin)

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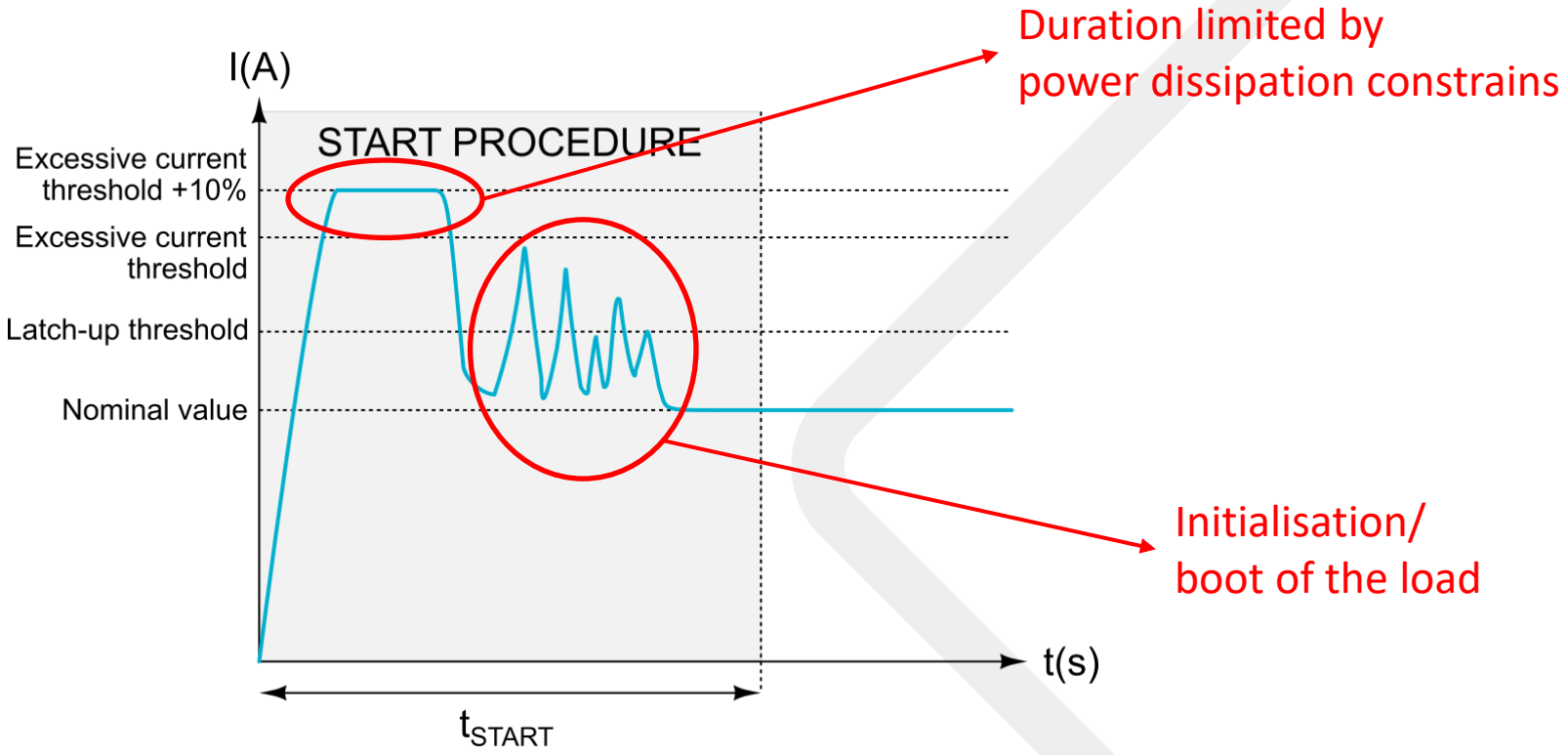
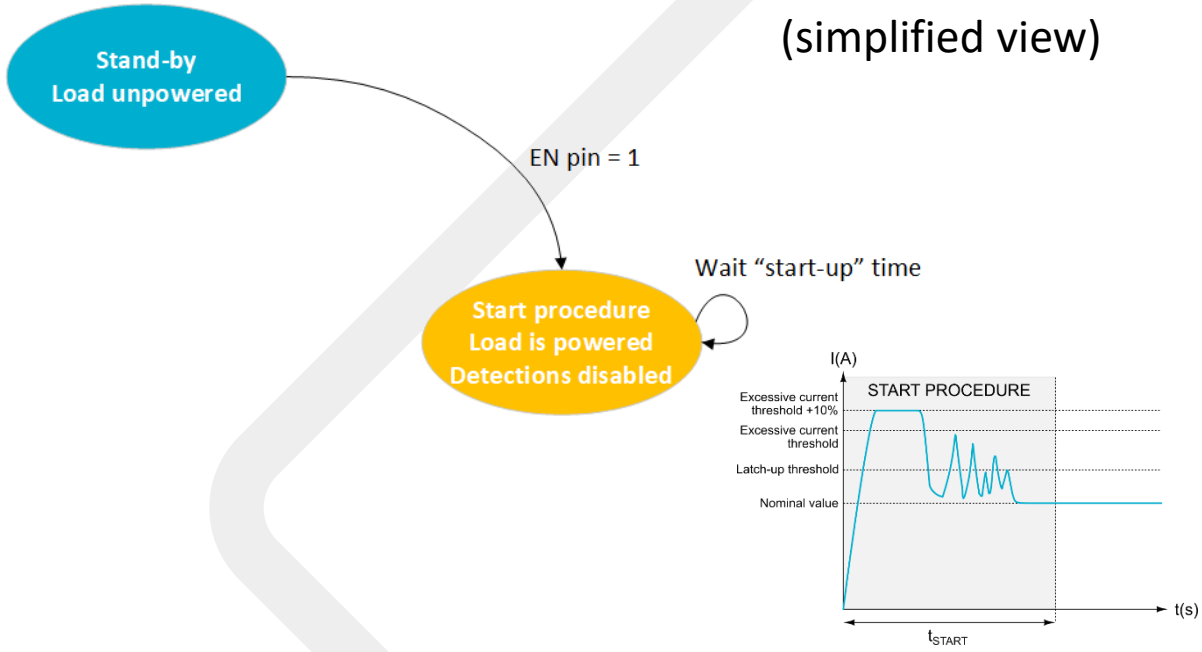
# Current detection and limitation during start-up




→ latch-up and excessive current detection is masked during the start procedure

# Protection controlled by a state machine

(simplified view)



# Protection controlled by a state machine

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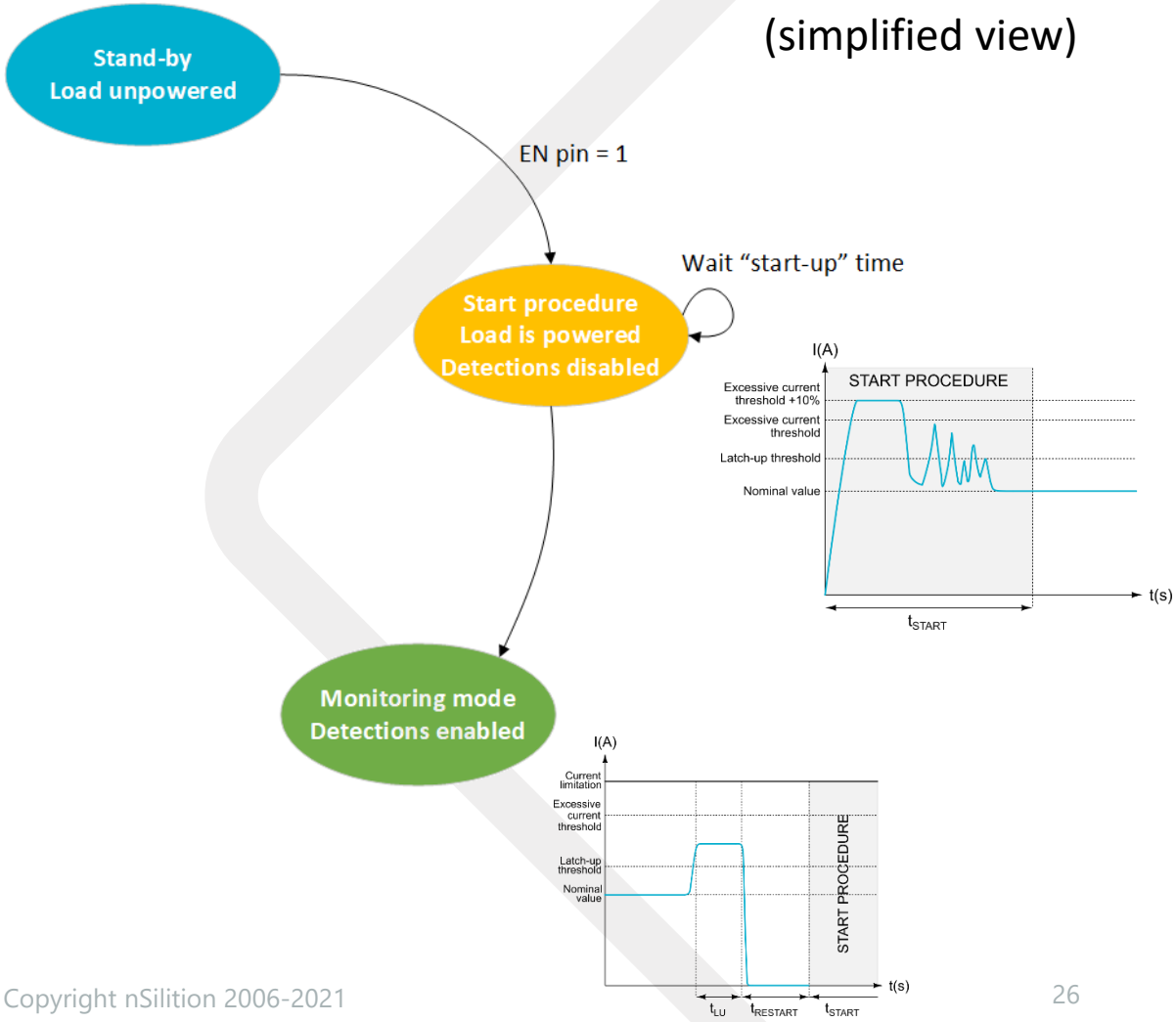


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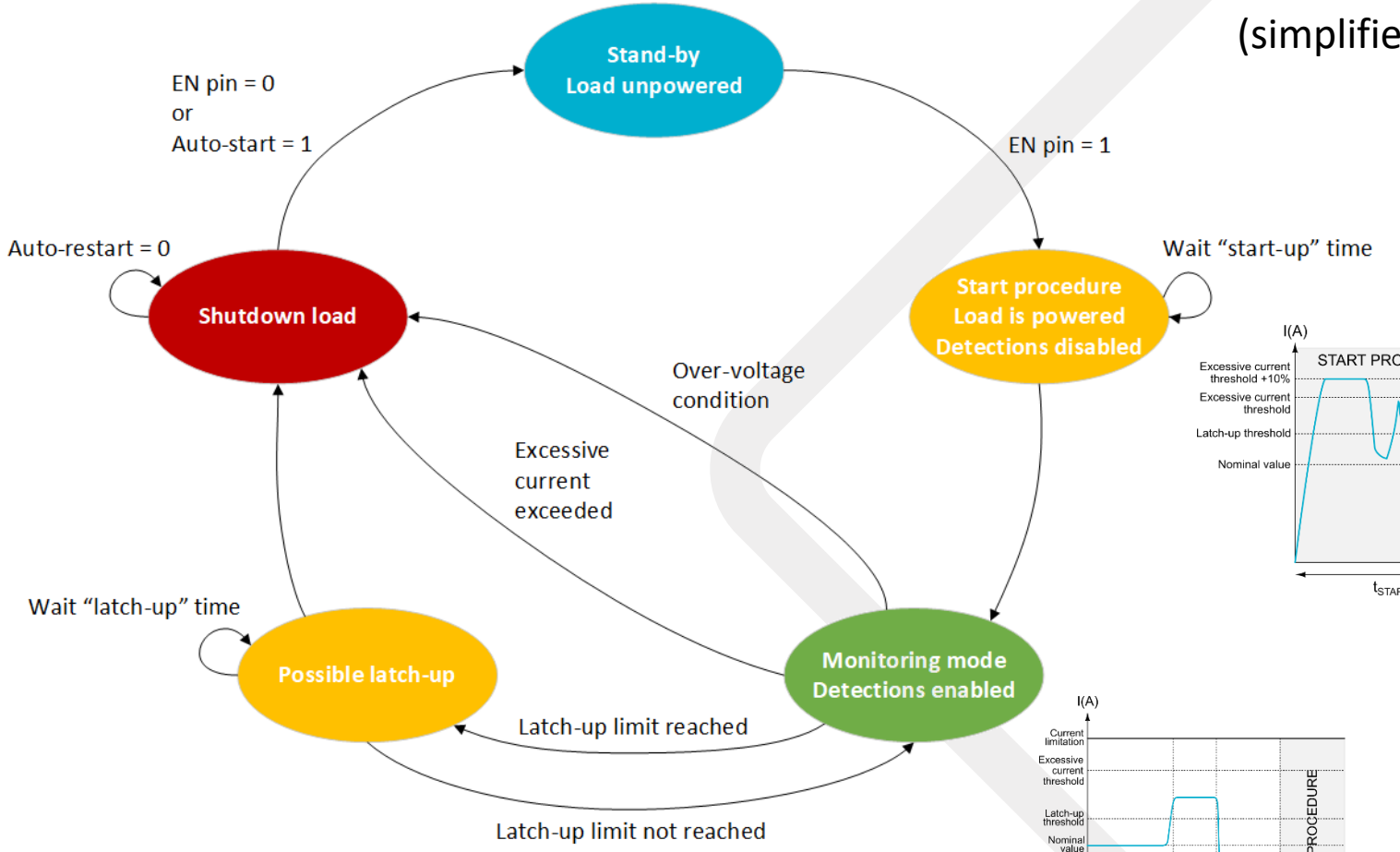
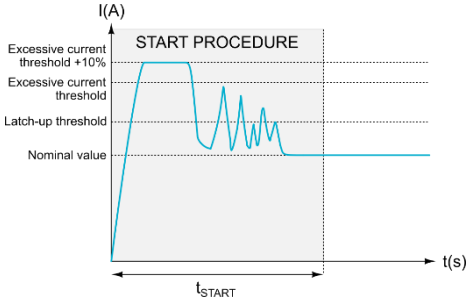
# Protection controlled by a state machine

(simplified view)







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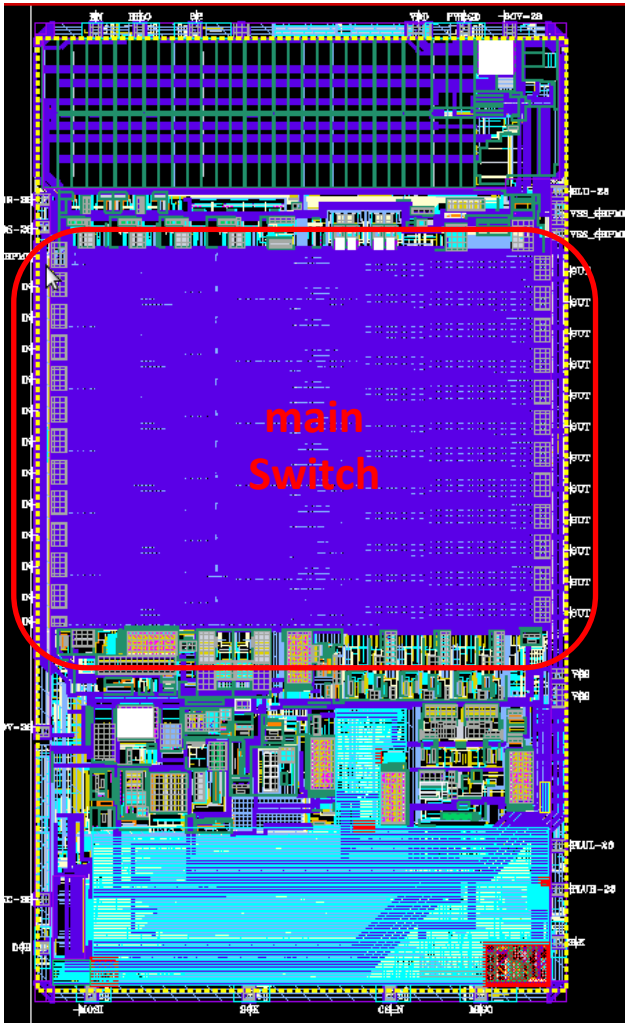
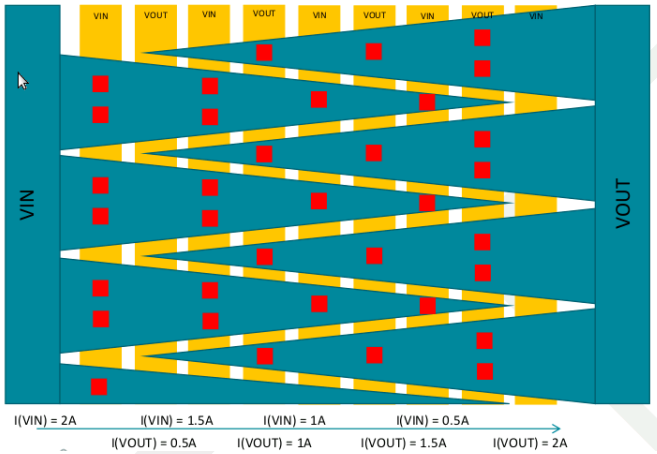
# Main switch and current control




The **Main Switch** is **layout**:

- to **equalize** power **dissipation** across silicon area
- to sustain **10V** voltage and **2A** current
- to **select** of the **Ron resistivity** (7Ω to 50mΩ)
- to **maintain voltage drop** in the specified range

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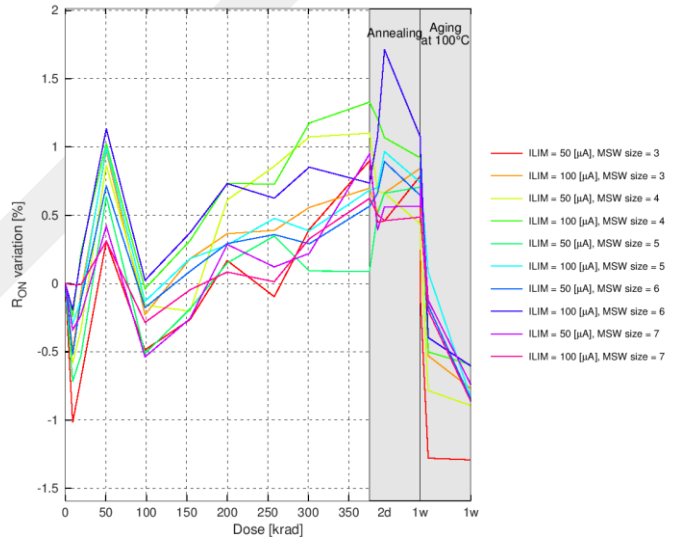
# Main switch and current control

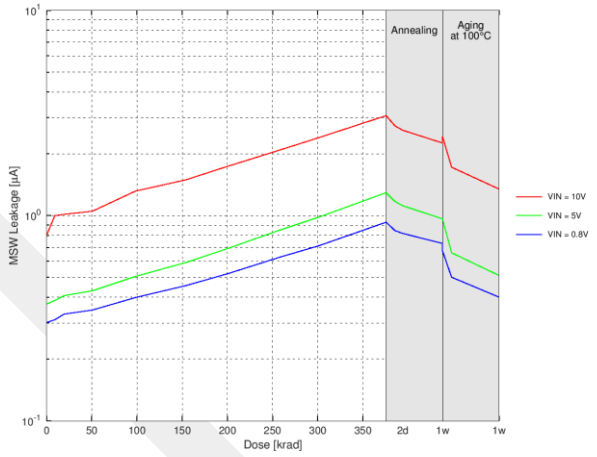
**Main Switch** radiation hardening and tolerance:

- Implemented using **10V NMOS device**
- **TID tolerance** tested on the **Luca Testchip**
- **$R_{on}$** and **current limitation** compensated
  - temperature variation
  - TID deviation

  by the **same regulation loop**

- Variation of $R_{on}$ over 300krad is < 2.5%
- In off state, the **leakage increase** over 300krad **stays limited**
- **Leakage current** is **sink** to **ground**, not to the load

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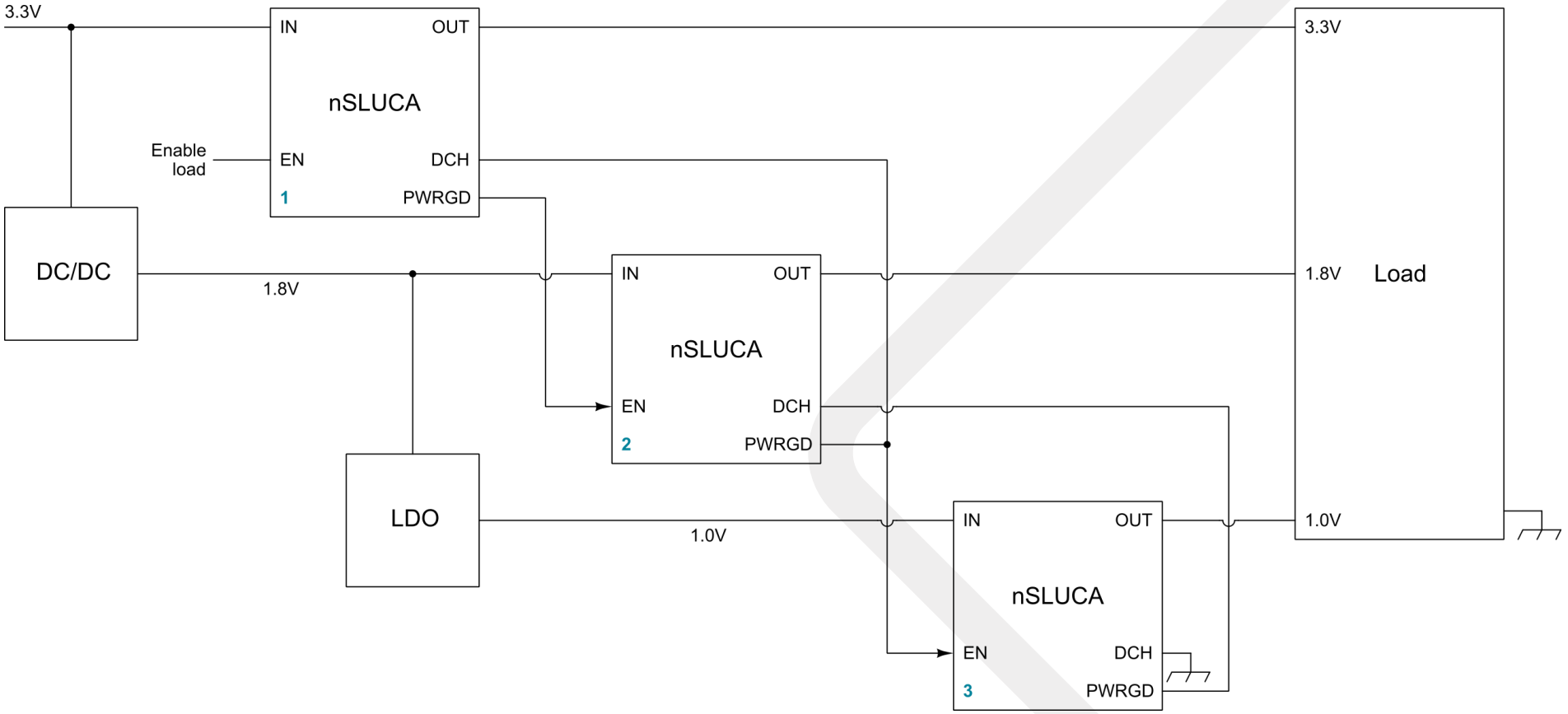
# Protecting dependent supply domains

# Daisy-chaining LUCAs: one example




Start-up sequence 1 → 2 → 3

PWRGD = 1 when the supply is stable

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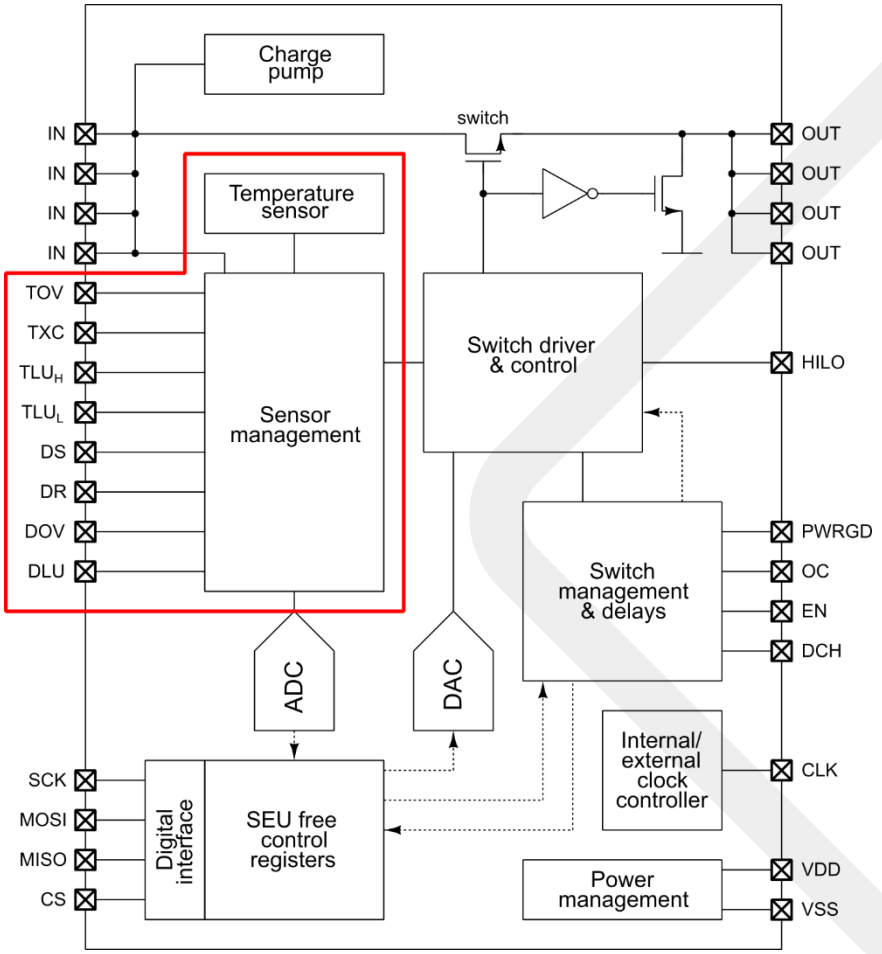
# Controlling thresholds

# Controlling thresholds: with/without OBC

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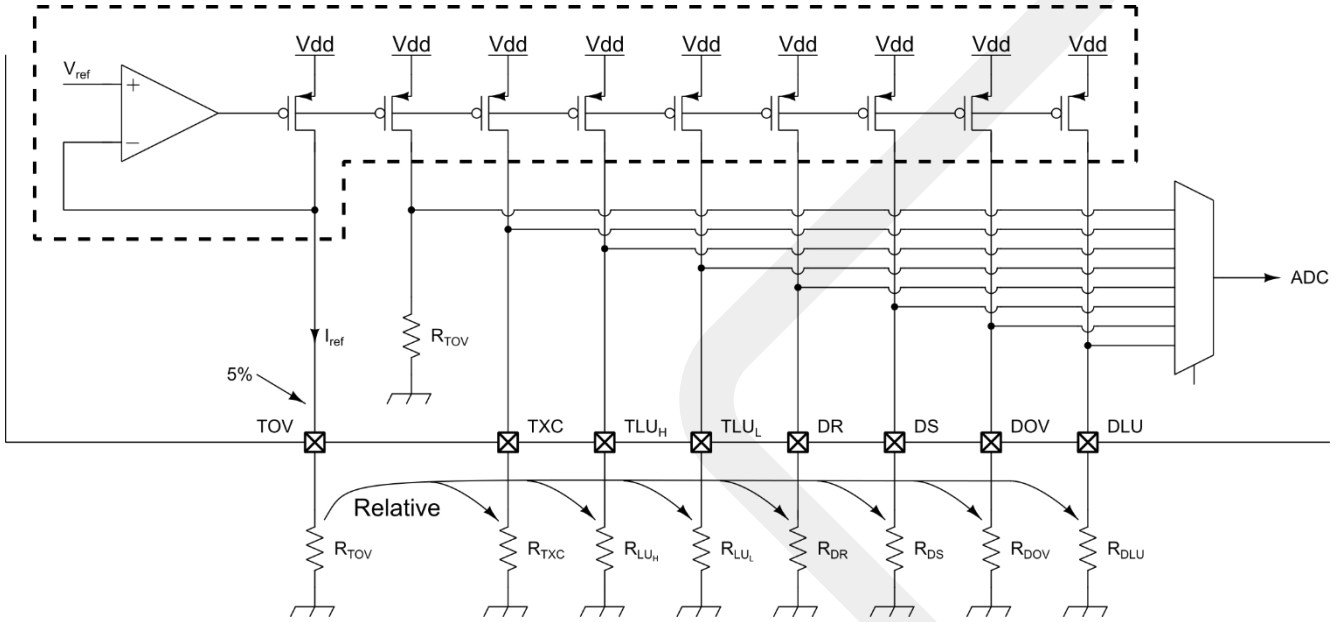
# Controlling thresholds: with/without OBC

- Principle schematic




- TOV: over-voltage (low precision). Relates to absolute value $R_{TOV}$
- TXC: excessive current threshold
- $TLU_H$: latch-up current threshold high
- $TLU_L$: latch-up current threshold low
- DR: delay restart
- DS: delay start procedure
- DOV: delay over-voltage
- DLU: delay latch-up

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# Controlling thresholds: with/without OBC

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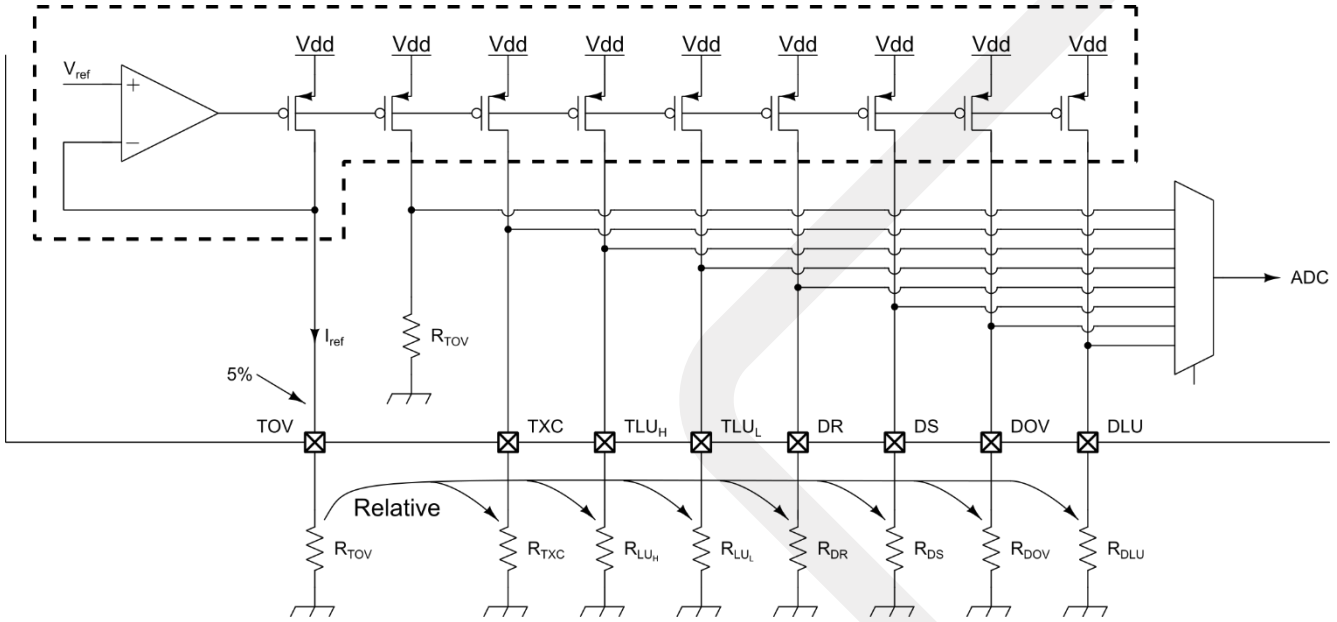


- TID tolerance by proper design of current sources
- SET tolerance by redundant measurements
- Precision on TOV is ± 5%
- Precision on other values is ± 1%

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# Controlling thresholds: with/without OBC

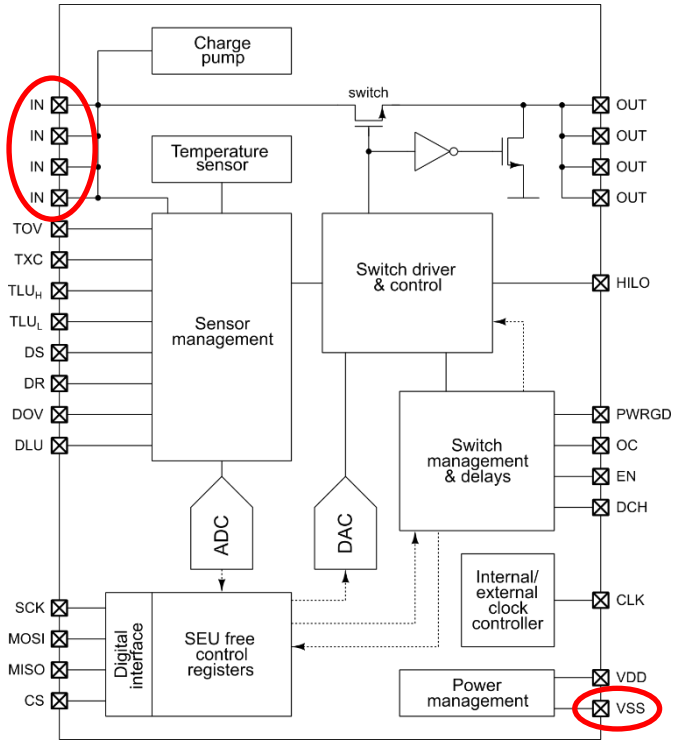
- LUCA does not need an OBC to be used and programmed
  - "Stand-alone" version → 28 pins
  - Can be still over-written by OBC
  - Resistor omitted → default value in register
  - Redundancy or "safe" mode if OBC is out-of-order

# Controlling thresholds: with/without OBC

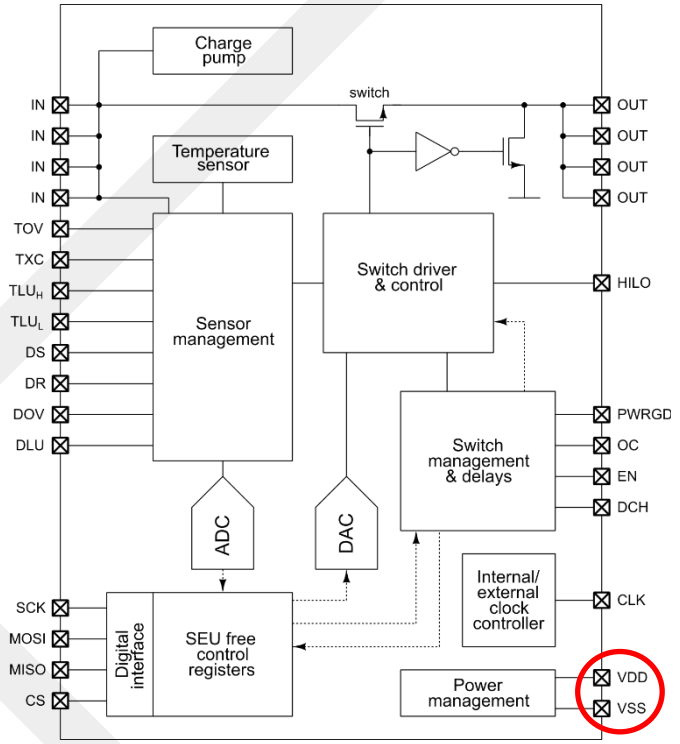
- In case control by OBC is performed
  - Do not equip the resistors (or use the 20 pins LUCA)
  - Power-up LUCA
  - Program the right threshold
  - Rise enable pin (EN)

# Power management of LUCA

# Power management allows two supply schemes




Supply by the IN pins if IN > 4V and VDD < 3V




Supply by the VDD pin HAS PRIORITY if VDD > 3V

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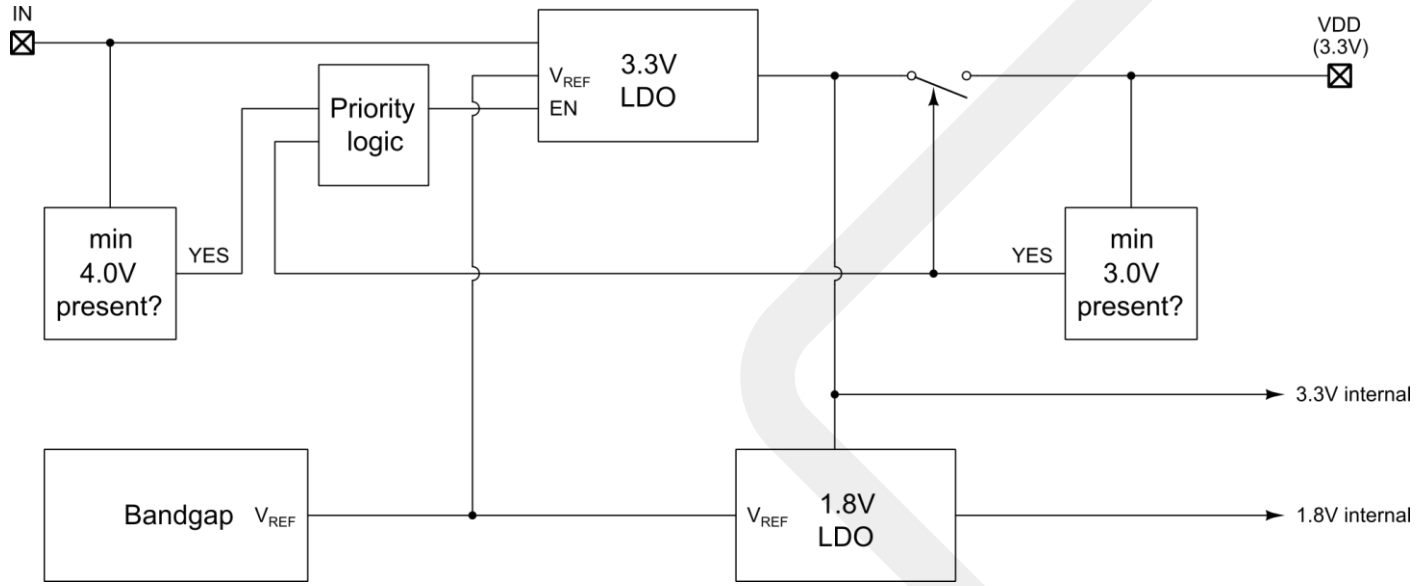
# Power management allows two supply schemes

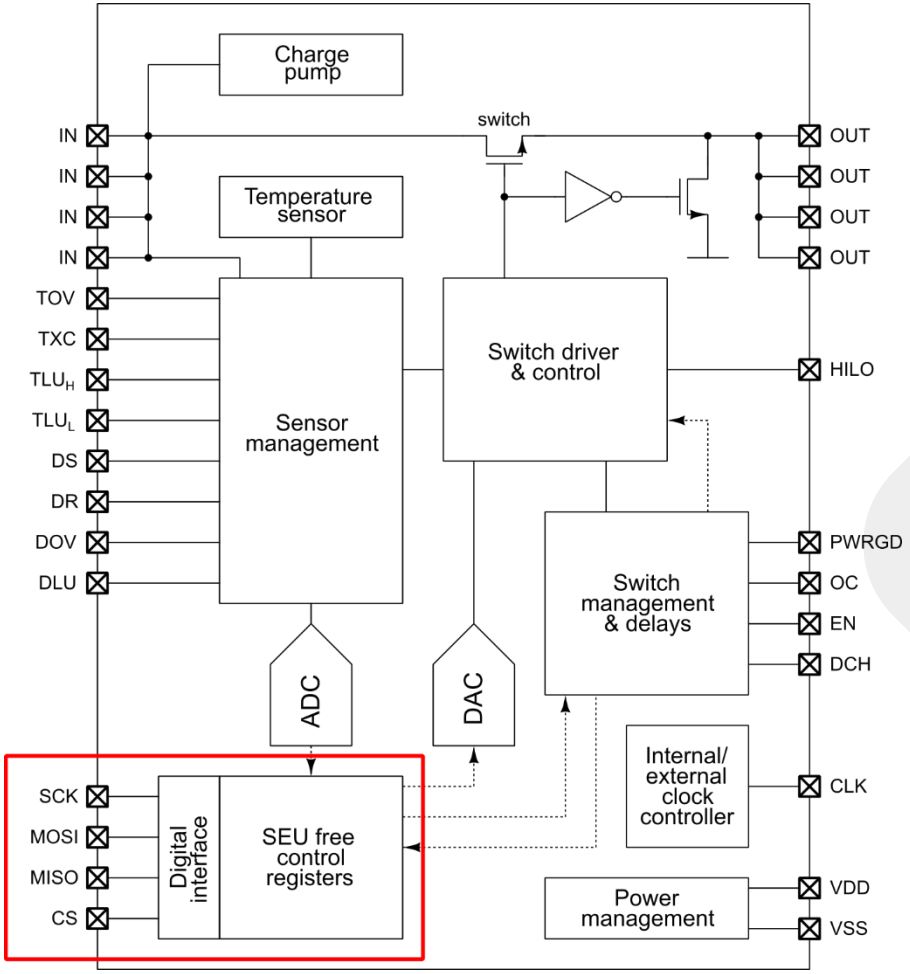
- Principle




- Bandgap is TID tolerant, LDO too
- SET tolerance by proper design

# Digital interface

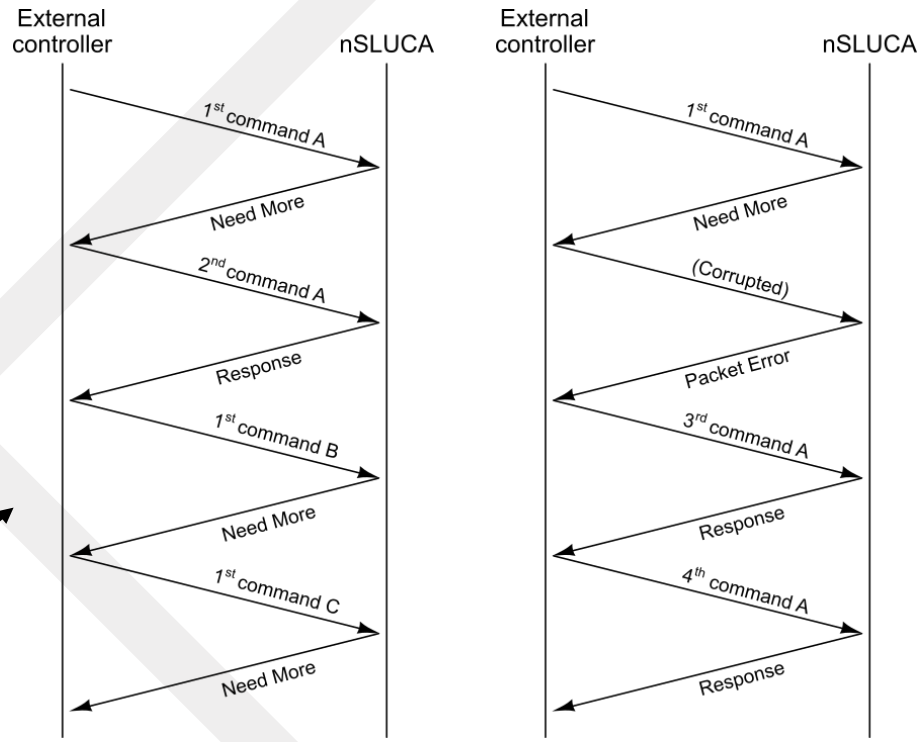
# SPI interface




- SET tolerant SPI interface and logic
- SEU free control registers
- Cold spare IOs → allow to leave unpowered LUCA connected to the SPI bus

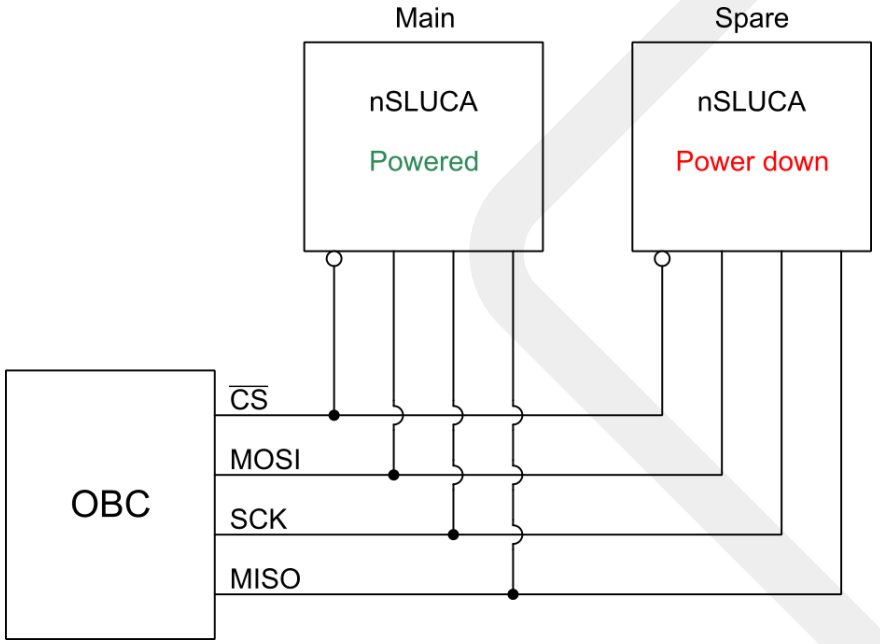
# SPI interface

- One command is 24b:
  - 8b address
  - 8b data
  - 8b CRC check
- SET tolerance of the SPI interface
  - Obtained by repetition of the message
  - “Redundant” signaling
  - CRC check



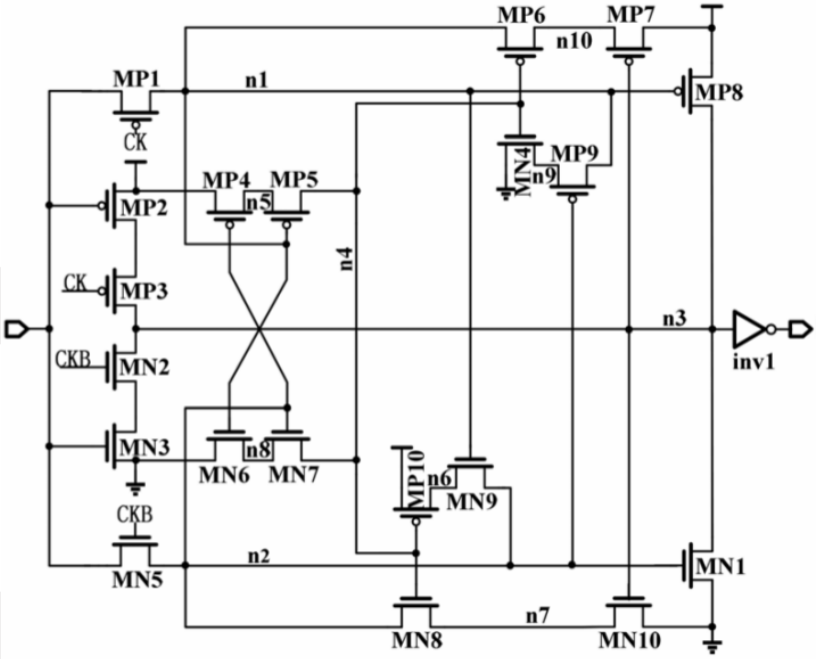
# SPI interface

- Cold spare IOs
  - Allow some redundant LUCAs in power down mode



# Digital library: SEU Resilient D-Flipflop

- Latches used to construct the master and slave parts of FFs are based on triple-interlocked latches
- Resilient to multiple simultaneous particle strikes
- Added SET/SEU resilient reset circuitry



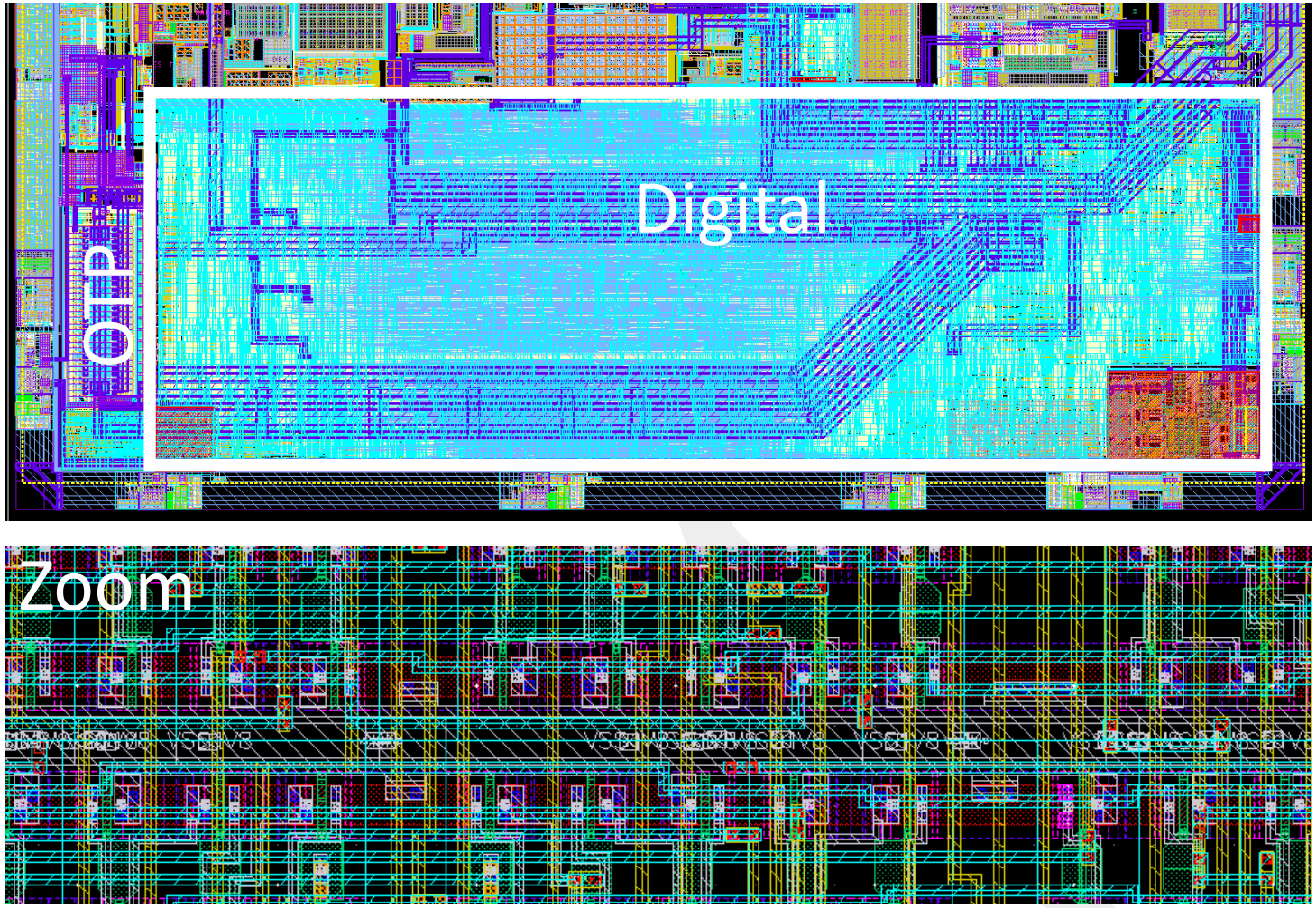

TIL-latch (1/2 of a FF)

Reference: T. Li, H. Yang, G. Cai, T. Zhi and Y Li, "A CMOS Triple Inter-Locked Latch for SEU Insensitivity Design," *IEEE Trans. Nucl. Science*, vol. 61, no. 6, Dec. 2014, pp. 3265-3273

# Digital library

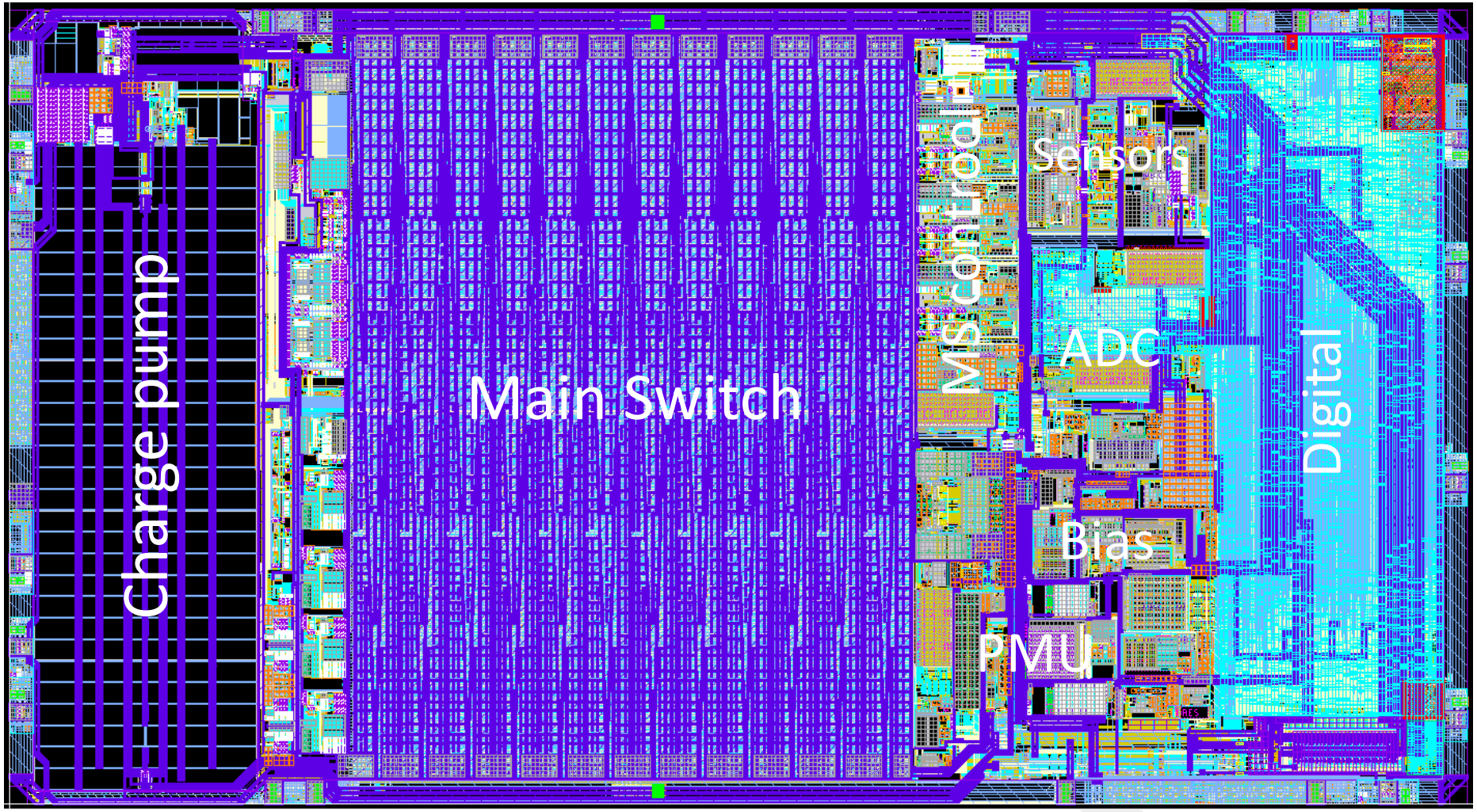
- Library has been made synthesizable
  - Automatic timing characterization
  - Description under the Liberty format available
  - Synthesis with various synthesis tools
- Library has been designed placeable and routable
  - LEF abstracts available
  - Placed and routed with Innovus

# Digital library



# LUCA layout

# LUCA top level layout



# Current status

# Current status

- Current status
  - First layout tape-out January 2020
  - /!\ First silicon dies received January 2021
  - Packaging first engineering samples done March 2021
  - Evaluation and characterization started
- Next steps
  - First characterized devices expected in September 2021
  - First engineering samples can be ordered by September 2021
  - Radiation tolerance characterized by end 2021

# Conclusion

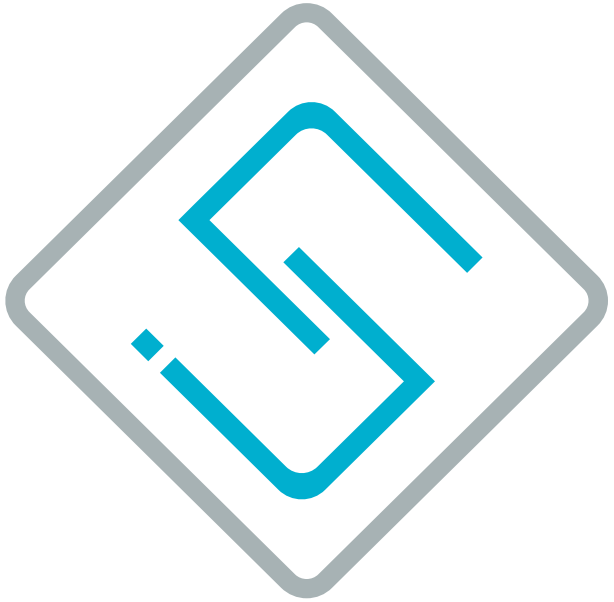
# Conclusion

- Test chip to assess radiation tolerance
  - of elementary devices
  - of analog blocks
  - of digital library
- Controlled and monitored current. Different phases
- Can be used with or without OBC
- Daisy chaining with priority scheme
- Two possible supply schemes
- SET resilient SPI interface and SEU free digital control

# Contributors

- Designed by nSilition AMS IC design team
  - Alessandro Michielin
  - Drahoslav Lím
  - Quentin Wala
  - Thierry Delmot
- Specified in collaboration with ESTEC
  - Giorgio Magistrati
  - Richard Jansen

Any questions?



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# Thank you!