ATMX150RHA Building Blocks – Block Presentation and Measurement Results

Julien Fleury[1*], Salleh Ahmad[1], Florent Perez[1], Valentin Brinster[1], Jean-Baptiste Cizel[1]

[1]Weeroc, 4 avenue de la Baltique, 91140 Villebon-sur-Yvette, France ;

Weeroc has designed several analogue and mixed signal IP blocks in Microchip ATMX150RHA technology with support of CNES. These IP blocks has been tested for electrical performances, temperature variation and irradiation up to 100krad.

The test vehicle is composed of:

- Two different kind of bandgap
- A 10-bit 10MHz SAR ADC
- A 500MHz-bandwidth switch

One bandgap is a low surface trimmable allowing to adjust the value based on process parameters and user requirement to have an optimized reference. The second bandgap is a large generic bandgap that is not trimmable but optimized for room temperature and minimizing dispersion over a -40°C to +125°C temperature span.
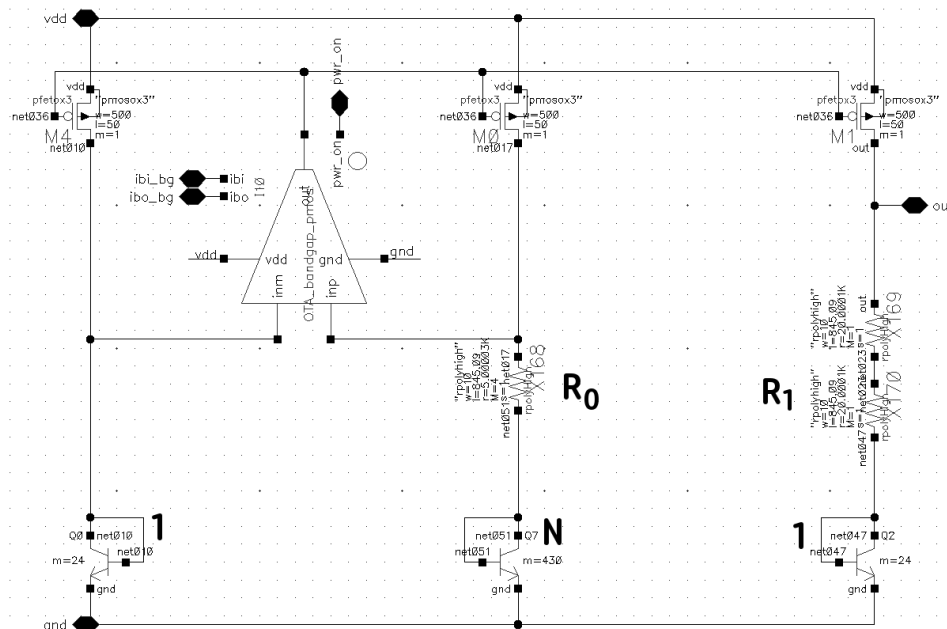

Figure 1 - Bandgap scheme

SAR ADC is using a capacitance ladder as a C-2C DAC, a fast low-offset comparator and an asynchronous state machine handling the approximation sequence. ADC requires a differential input and provides a 10-b parallel output. A conversion signal active on rising edge triggers the track and hold and the approximation state machine. A conversion done signal is asynchronously provided

when conversion is done and data are available. Data remains available on output until next conversion is started.
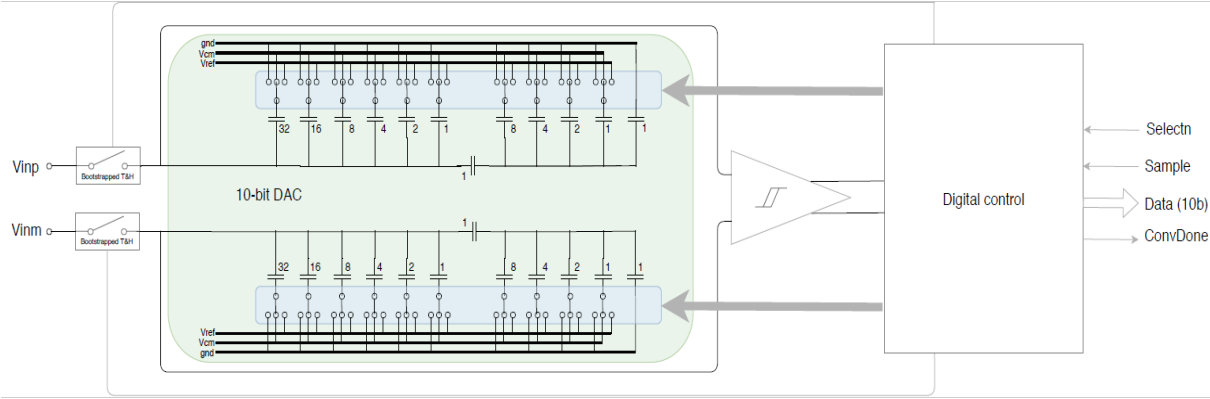

Figure 2 - SAR ADC block scheme

High Frequency switch is a 5V analogue I/Os 3.3V digital control switch with a RDSON lower than 20 Ohm and an isolation over 70dB at DC and in the 60dB range at 10MHz. That switch is embedded both in an 8-to-1 analogue multiplexer and in a quad switch component.

These blocks will be detailed and measurement results of electrical performances, temperature and irradiation hardness up to 100krad will be presented for each of these blocks.