IM485A Mixed-Signal Analog/Digital ASIC design Development& Qualification based on IDMOS rad-hard XH035 library

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Abstract

The needs for increasingly low cost, low space occupancy and reduced weight in the space industry have made mixed-signal ASIC integration mandatory.

The aim of the contract was to develop, qualify and deliver the flight models of the mixed Analog/Digital ASIC, named ACCORC7 or IM485A for the CODECHAMP Company. It is a high resolution optical encoder and polarimetric position sensor.

In a first contract, the CNES and ID MOS selected the mixed-signal XH035 LV technology to design a set of rad-tolerant Low Voltage ELT transistors, checked their robustness up to total ionizing dose of 100Krads and their immunity to the Single Event Latch-up under heavy ions.
The design of those transistors made it possible to reach the required radiation level and the characterization of these basic elements made it possible to have reliable simulation models in order to secure the result from the first Silicon run.

Once the prototypes were validated by CODECHAMP, ID MOS launched a production batch for the qualification and delivery of the flight models.

I. INTRODUCTION

The activity of ID MOS, a SERMA Group company, is the industrialization of integrated circuits. We take charge of activities which can go from the development, the characterization of libraries, the design of a digital, analog or mixed ASIC down to the qualification for fields such as: Automotive, Transport, Medical, Space, Avionics, ..including the radiation tests.
ID MOS performed all these tasks for the IM485A Analog/Digital ASIC. This circuit is a high-resolution angular sensor for a contactless spatial application using the optical technology of CODECHAMP Company.
It is based on the standard XFAB process: XH035 (350nm) and on the IDMOS Low Voltage RadHard Library fully characterized for the radiation environment including Digital and Analog cells.
The circuit has been fully qualified according to ESCC9000 and the flight models delivered.

The tasks performed in this contract are the following:

- Design of the Analogue blocks
- Design of the Digital blocks in VHDL language, including the CORDIC Algorithm provided by CODECHAMP.
- VHDL synthesis including automatic flip-flops triplication to minimize SEE effects
- Manufacturing , Probing, Assembly , Final test
- Radiation Tests (TID , SEE) according ESCC specifications
- Qualification according ESCC9000 specification
- Flight models delivery.

II. IM485A DESCRIPTION

The IM485A circuit is part of the ACCORCx family circuits defined by CODECHAMP. This ACCORC version 7 is a high resolution optical encoder dedicated to space applications. The circuit performs the calculation of an angular position based on the CORDIC algorithm developed by CODECHAMP. In an application point of vue the new coder must be fully compatible with the previous version but most of the Analogue functions, previously based on discrete components, are now integrated in the ASIC.

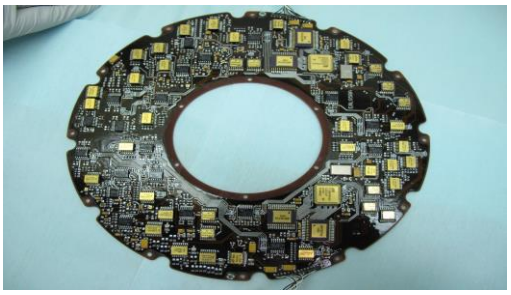


Figure 1: Previous Encoder version

A. Main Features :

- 22 Analogue structures (Differential or single) dedicated to receive data from Phototransistors only.
- 8 photo Amplifiers (Differential structures) dedicated to either Phototransistors or Photodiodes.
- 2 SAR ADC 12Bits (ID MOS IP) are used to process the photo amplifiers output
- Digital interfaces I2C / RS422 for programming or Data transfer
- Supply voltage range: 3.15 V to 3.45 V
- Operating temperature range: -40°C to +125°C
- Based on the IDMOS 0.35µm RadHard Library.

- Radiation requirements:
  - TID (Total Ionizing Dose): 100 krad(Si)
  - Single Events Effects: (SEL, SEFI, SEU, SET)
    - SEU, SET characterisation
    - No SEL, No SEFI up to a LET equal to 62.5 MeV.cm²/mg with a total fluence equal to $1E^{+7}$ ions.cm^{-2}

B. Architecture Description:

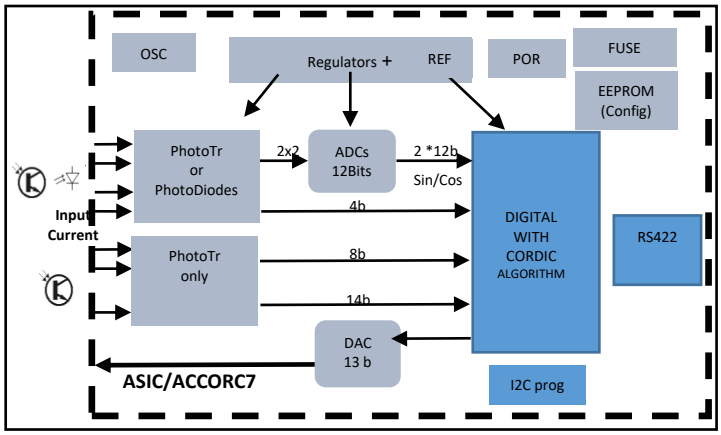


Figure 2: IM485 Bloc Diagram

This mixed analog/digital circuit receives, at the input, currents supplied either by phototransistors or by photodiodes corresponding to the Sine and Cosine of the angle.
Input data from phototransistor or photodiode arrays can be processed in 4 different ways with 4 different modules. After a current/voltage conversion, the information is digitized either by ADCs or comparators.
After digital conversions, the angle is calculated with the CORDIC algorithm and then transferred to the outside via the digital RS422 interface. (TIA/EIA-422-B standard)

Each analog module is a set of amplifier or comparator. The gain of the input amplifiers is fixed by a matrix of integrated resistors, programmable via the digital I2C interface.
Three regulators are designed to provide the supply for the Analogue, Digital and ADC blocks.
Voltage references (1.35 V, 2.7 V) are provided for the ADC.

The ASIC parameters defined by CODECHAMP are stored in an EEPROM memory to provide flexibility during validation. The content is written in a fuse matrix for the flight models.

Other functions:
- Quartz Oscillator 20MHz / POR / Bandgap
- ADC 12bits 1Msp/s
- DAC13bits 10 Ksp/s
- A digital function allows the communication between two ASICs for high precision application purpose.(Chain mode)

C. Advantages

Four main advantages:

1. ITAR Free and independent from the United States to supply of components
2. Reduction of the number of discrete components

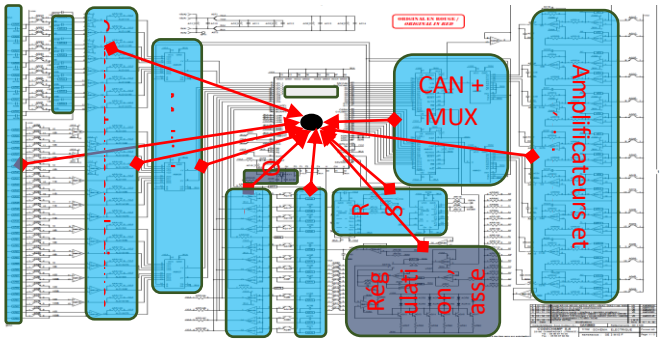


Figure 3: Functions integrated in the ASIC

3. Volume and weight reduction
4. Economic Competitiveness

III. XH035 RadHard Library

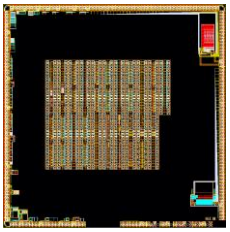
A. Description :

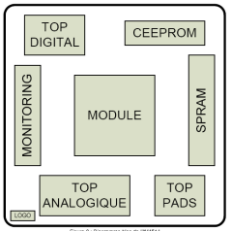
The development of the RadHard IDMOS library was presented at AMICSA2014. This library is based on the XH035 XFAB process. The objective was to obtain accurate models to guarantee the result during the first Silicon Run for the design of a Digital or Analog circuit for Space. The advantage is to significantly reduce the cost and delivery time of the flight models.

A test chip has been designed, manufactured, comprising analog, digital and memory blocks sufficiently representative of the functions of a mixed digital or analog ASIC, in particular for the IM485A.

We have integrated seven blocks including functions based on harden transistors (ELT) and standard transistors to compare their radiation levels:

- Digital : Basic digital cells & functions
- Monitoring : Basic devices with ESD protection
- Analogique : Basic analogue cells & functions
- Pads : Input/Output/Bidirectional
- Memories : Std XFAB SRAM/CEEPROM
- Module : Basic devices





B. Description & results of the radiation tests:

The total dose tests have been carried out with a Cobalt 60 source on 6 parts up to 100 krads at a low dose rate of 310 rad/h. An annealing of 24h/25°C plus 168 h/100°C has been performed.

TID tests have shown no functional or parametric drifts up to 100 krads on hardened structures.

The SEE tests were performed at UCL (Belgium) using Xenon ions with energy of 1217 MeV and a LET on die surface of 67.7 MeV.cm²/mg at a temperature of 125°C on IM485A devices.
No SEL was observed on the Rad-Tolerant cells up to 67.7 MeV.cm²/mg and with a total fluence equal to $1E^{+7}$ ions.cm^{-2}.
No SET and SEFI were observed during irradiation with a LET of 62.5MeV.cm^2/mg and with a total fluence equal to 1E+7 ions.cm^{-2}.
Some SEU and SET were observed with a LET of 32.4MeV.cm^2/mg (Krypton heavy ions) and with a total fluence equal to $1E^{+6}$ ions.cm^{-2}.

C. The Design Kit:

The ID MOS RadHard Design Kit is an extension of the official XH035 DK provided by XFAB. The advantages are multiple: maintenance, enhancement, no training, no time lost in using it.
It provides a database of models, primitive devices, digital cells, I/O cells, configuration scripts and tools needed to design Rad-Hard-by-Design mixed-signal Analogue/Digital Integrated circuits, according to ID MOS custom rules.

D. Project Design Flow

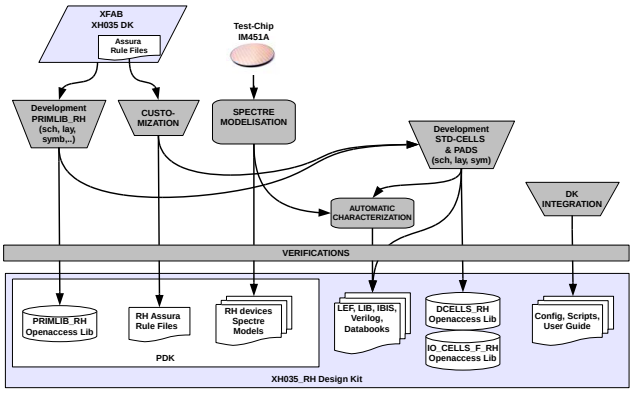


Figure 4: Project Design Flow

E. Process Design Kit (PDK)

The PDK is the core of the RadHard Design Kit. It includes all the low-levels Cadence libraries, configuration files and scripts to develop and simulates Rad-hard functions.

It consists of three main parts.

- *SPECTRE Models :*
- *ASSURA Tool Kit : LVS and DRC*
- *Library PRIMLIB: composed of a set of low voltage transistors hardened against radiation.*

F. STD-CELLS & I/O Libraries

It includes a library of digital standard cells (~40) and 3V digital/analogue standards pads (~15) suitable for logic synthesis and automatic P&R:

- ⇨ Schematics + Layouts + Abstracts + symbols
- ⇨ Liberty library
- ⇨ Verilog Library
- ⇨ LEF Library
- ⇨ Tutorial(s)
- ⇨ Detailed description of SEU-hardening procedure(s).
- ⇨ IBIS Models of Digital Pads
- ⇨ Library databook

1) Electrical Characterization conditions :

- Voltage : 1,8V up to 3,6V
- Temperature : -55°C ; 25°C ; 125°C
- Process : Slow/Fast
- With/without radiation

IV. IM485A Procurement/ Qualification :

The aim of the procurement specification is to explain ASIC characteristics and particular conditions for the purchasing and the qualification of a full custom ASIC.
It describes all tasks done at all quality levels: Prototypes, Qualification, Flight models.

A. Tests & Operations

1) Prototype Level :

- Wafer probe
- Assembly
- Final electrical Test
- Heavy Ions Single Event Effect Test

2) Qualification level :

- Wafer probe
- SEM
- Assembly in CQFP132 package:
  - Special In-Process Controls (Bond strength & Die shear)
  - Die Visual Inspection (Level A) – PRE-CAP
  - Sealing
- Final electrical Test
- Total Dose Radiation Testing (TID)
- Residual Gas Analysis (according MIL STD 883)
- X-Ray analysis
- Screening tests
- Qualification Tests

3) Flight Models level:

- Wafer probe
- Assembly :
    - Special In-Process Controls (Bond strength & Die shear)
    - Die Visual Inspection (Level A) – PRE-CAP
    - Sealing
- Final electrical Test
- X-Ray analysis
- Screening tests

B. Screening :

Screening tests are done on all packaged parts used afterward for qualification and on all Flight Models according ESCC9000 specification:

- Serialisation
- High Temperature Bake (24h – 150°C)
- Temperature cycling (10 cycles)
- Particle Impact Noise Detection (PIND test)
- Electrical measurement (25°C)
- Burn-in (240h- 125°C)
- Final Test at 3 temperatures
- Electrical measurement (25°C) (Drift calculation)
- Fine & Gross Leak
- External Visual Inspection
- Solderability

C. Qualification

The qualification follows strictly the ESCC9000.
Among the screened parts, 50 are used for the Qualification lot which is divided in 3 subgroups:

- Environmental / Mechanical Subgroup : 30 parts
- Endurance Subgroup : 15 parts
- Assembly Capability Subgroup : 5 parts

No failures are allowed in any of those tests. The qualification of ACCORC7 ASIC was successful.

V. CONCLUSION

The IM485A mixed analog/digital circuit has been fully validated with the first Silicon Run. Apart from a small error in the RESET signal release in one mode which was corrected at Metal level.
All the Analog cells have been validated on the first Silicon run. This validates the design and verification methodology implemented by ID MOS on their 0,35µm RadHard library: Modelling, Triplication, Simulation of SETs, all developed by ID MOS before Manufacturing.
The circuits have successfully passed all the screening and qualification tests.
This allowed the delivery of the flight models to CODECHAMP in time.

References

ESCC9000 INTEGRATED CIRCUITSESCC25100 Single event effects test method and guidelines
ESCC22900: Total Dose Steady-State Irradiation Test Method
ECSS-Q-ST-60-02C Space Product Assurance-ASIC and FPGA development
ESA-ESTEC- Space engineering, product assurance
ECSS-Q-HB-60-02A "Techniques for radiation effects mitigation in ASICs and FPGAs handbook"