A Cost and Size Optimized Motor Control Solution using Radiation Hardened AFE + Microcontroller Circuits

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INTRODUCTION

Traditionally, radiation hardened Permanent Magnet Synchronous Motor (PMSM)/ Brushless DC (BLDC) motor control uses the Field Oriented Control (FOC) method and is implemented using a Field Programmable Grid Array (FPGA) for the digital control portion and the drive and sense power/analog circuits are built using available rad-hard discrete or simple integrated circuits. This yields a relatively large size and mass electronic system but drive performance can also be very good (i.e. high speed and high accuracy of the control loop). A solution to optimize the cost and size is to use a highly integrated Analog Front End AFE (e.g. LX7720 spacecraft motor controller with position sensing) together with an FPGA. This solution lowers the size, mass and cost of the overall implementation and keeps the high-speed and high-accuracy performance. If, however, the very high loop speed is not necessary, it would be desirable to have a smaller, less complex solution. This paper describes what must be implemented to use a high-speed, rad-hard AFE together with a lower speed rad-hard microcontroller (MCU) for cost and size optimized PMSM drive electronics that runs a sensor-ed FOC control method implemented in software. The AFE + microcontroller solution was successfully prototyped, and measured data is presented.

INTERFACING WITH CURRENT SENSE DELTA SIGMA MODULATORS

When faced with the problem of reading data output of rad-hard, high-precision Delta Sigma Modulators (DSM) the classical approach is to use an FPGA and implement a form of low-pass decimation filter to convert the single-bit delta sigma digital stream to a lower bit rate, higher word length (e.g. 16-bit or more) parallel representation suitable for control, data acquisition or Digital Signal Processing (DSP) applications. Figure 1 shows a canonical implementation of a sinc^3 decimation filter that processes data from a second order DSM. Performance of this type of processing is well known in the literature. Additionally, for applications with frequent single event or other glitch-type disturbances, designers use a nonlinear filter to make the design more robust.

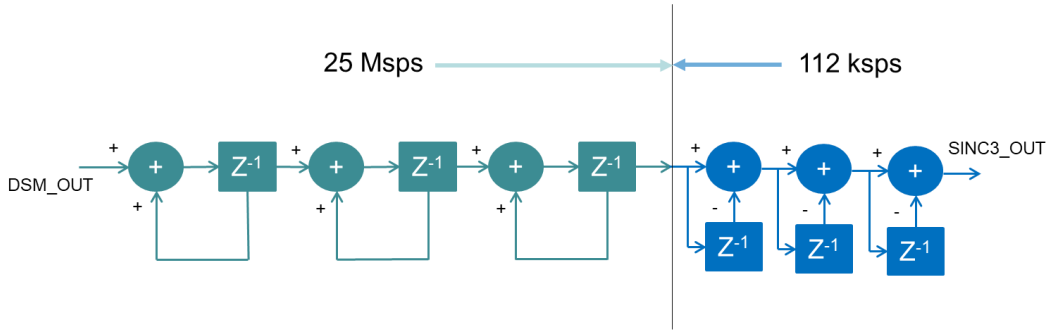

Figure 1. Canonical implementation of sinc^3 decimation filter

LOWER SPEED CONTROL SOLUTION FOR CURRENT SENSE

The traditional approach works well and can yield high frequency of operation but requires the use of an FPGA which could already be used for other aspects of the application. Particularly for motor/actuator control applications, where required speed is limited by the mechanical/inertial properties of the system, the usage of an FPGA could be wasteful. Additionally, software is more of a commodity than hardware/FPGA development so design cycle could be faster if using an MCU. Therefore, it is desirable from a cost-optimization perspective to use the current sense sigma delta modulators from a highly integrated AFE like the LX7720 together with an MCU like the SAMRH71. Because of the low speed/parallel nature of data input path in an MCU, the system needs to decimate the DSM data as quickly and as hardware-free as possible. One possible implementation is to build a two-stage decimation filter, the first stage could use a sinc^1 filter and have a simple counter as the first integrator stage. Then, the data is sampled via the counter's parallel output by the MCU at a low enough first decimation frequency. The second stages of filtering are done in software and executes at the first decimation frequency and, after a second higher order decimation filter, at the output decimation frequency. The single event filter can be inserted between the sinc^1 and second decimation filter (sinc^k) see Figure 2. In this example, the first counter uses a 4-bit up-down synchronous counter, followed by a decimation by 15 that lowers the data rate from 1-bit at 30 Msps to 4-bit at 2 Msps. If this is followed by a sinc^k decimation filter with a decimation by 128, it yields results of 16-bits at 15.6 ksps. Simulation results to showcase the resulting performance will be provided including Signal-to-Noise Ratio (SNR), latency and Single Event Upset (SEU) filter response.

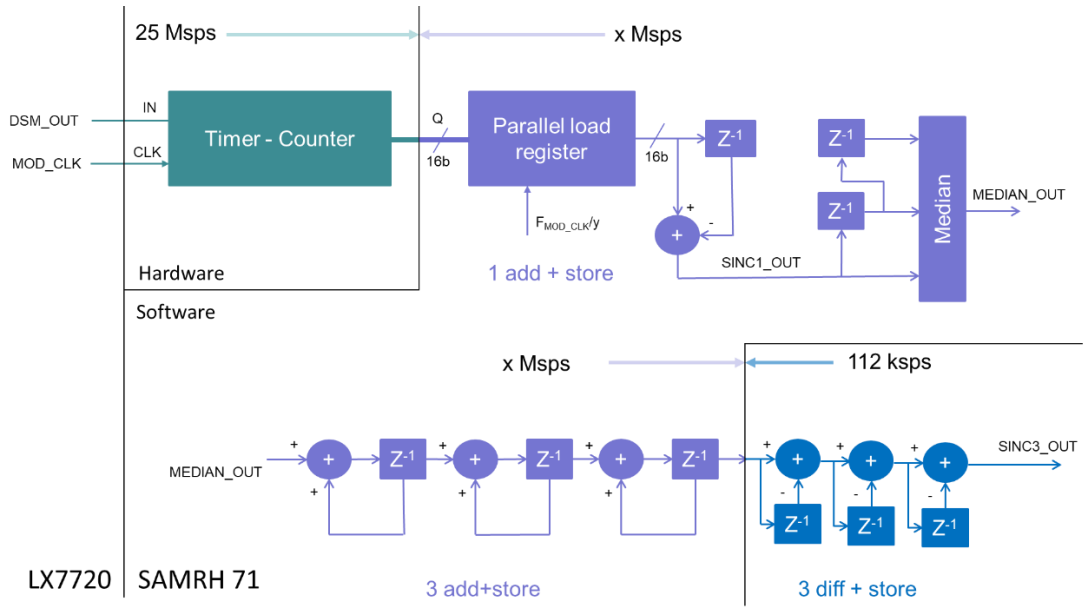

Figure 2. MCU-friendly decimation filter for LX7720 DSM outputs.

DETAILS OF THE MICROCONTROLLER INTERFACE

Luckily, the SAMRH71 MCU has the capability to implement the above-mentioned external function using an internal timer/counter channel so there is no need for an external counter IC—simply use a

counter/timer available on the microcontroller. Sampling for decimation is done using a periodic interrupt generated by another timer/counter channel. Figure 3 shows a block diagram of the motor control application of the LX7720 and SAMRH71.

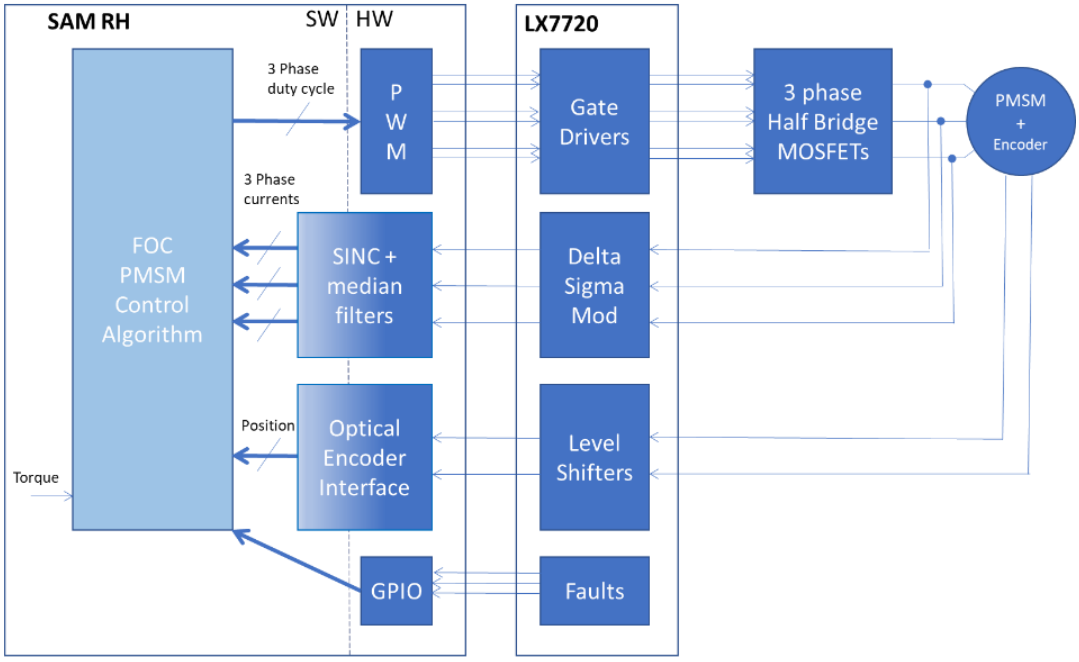

Figure 3. SAMRH71 and LX7720 motor control application block diagram

PROTOTYPING

A prototype was assembled using two evaluation boards for the two chips mentioned above. A traditional motor control software stack was adapted to the acquisition/DSP used for acquiring two/three current channel DSM outputs. Three SAMRH71 Pulse Width Modulation (PWM) resources are used to drive six LX7720 gate drivers. Three of the LX7720 level shifters are used to adapt the 5V position encoder outputs to the MCU IO voltage levels.

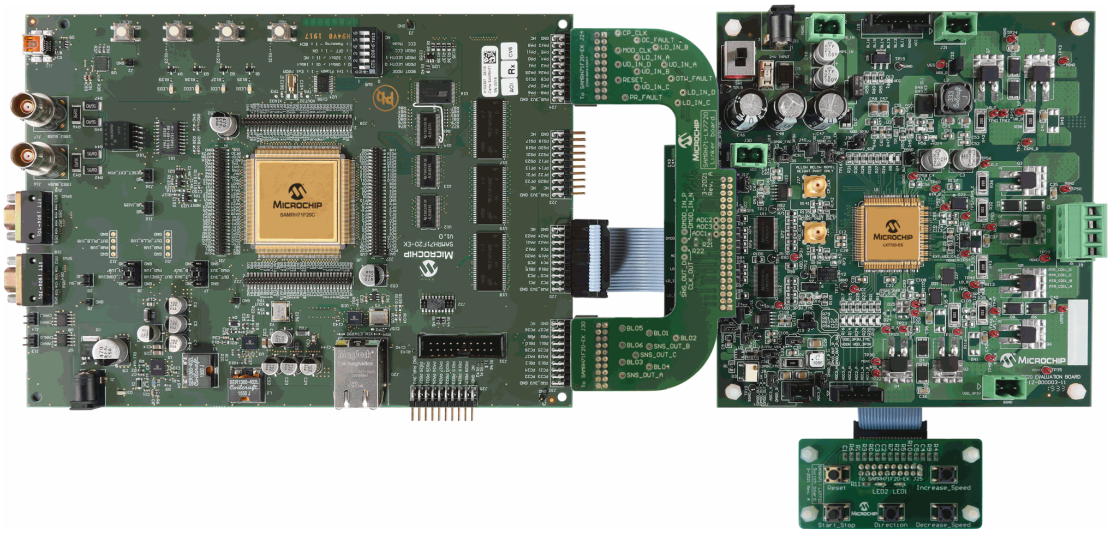

Figure 4. SAMRH71 and LX7720 motor control evaluation kit

RESULTS

First the implementation of the current sense was verified against oscilloscope captured waveform. These are compared to the data captured via SAMRH after SINC1 + SINC3 decimation in SW and the results match very well (see Fig. 5)

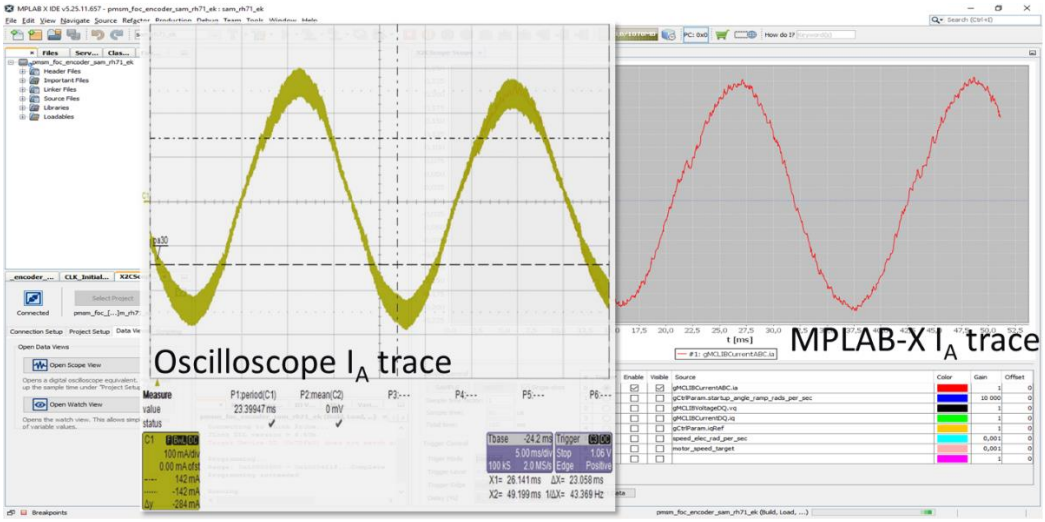

Figure 5. Oscilloscope v.s. average decimated current captured via LX7720+SAMRH71

Additionally the FOC algorithm was tested on light and heavier motor loads and loop response proves to be as expected. Figure 6 shows capture of control data during those transients. The ripple in the current is due to the asymmetrical load/torque.

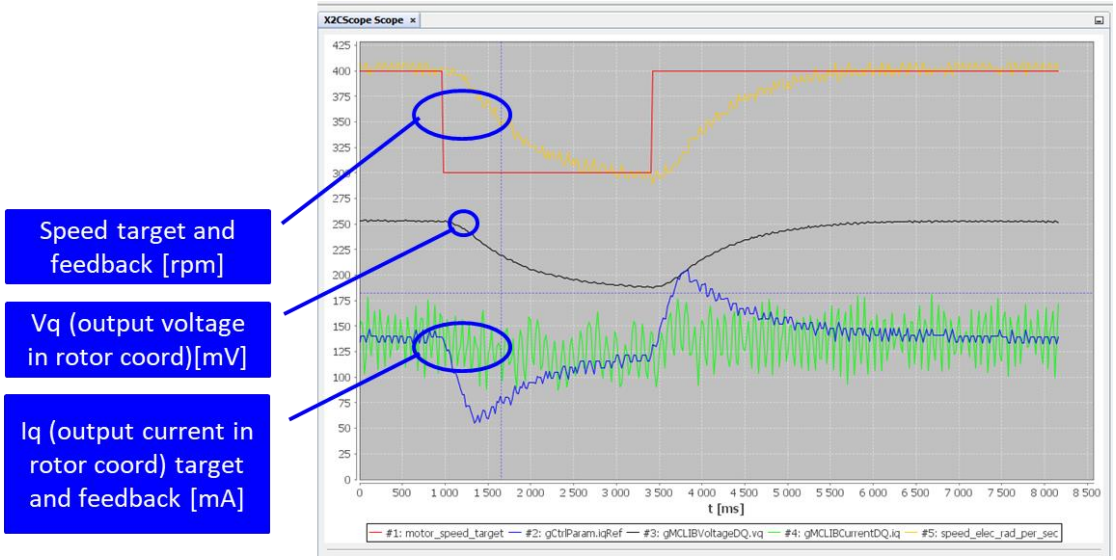

Figure 5. Light load: Loop response to transient torque target

CONCLUSIONS AND FUTURE WORK

A cost/performance optimized solution using AFE+MCU for radiation-hardened motor control will be successfully demonstrated. To further simplify the application, work could be done to integrate the application completely. Additionally, other filtering /decimation techniques could be even more microcontroller friendly.