Research on ADC Architectures Suitable for Space Applications and Technology Scaling

(Abstract)

I. CONTENT

The preliminary structure of the paper is described below:

- 1. Summary
- 2. Introduction
 - a. Research rationale
 - b. Technology
- 3. ADC features
 - a. Target performance
 - b. Architecture
 - c. Target applications
 - d. State of the Art
- 4. Radiation hardening
 - a. Hardening strategy
 - b. Analog core hardening
 - c. Digital core hardening
- 5. Project status
- 6. Conclusions
- 7. References

II. ABSTRACT

Analogue-to-Digital Converters (ADC) are one of the critical components that engineers seek when designing electronic hardware for space flight projects. Today there are very few suitable analogue-to-digital conversion solutions for space-qualified high-speed (from 10Msps onwards) and high-resolution (13 bits and above) applications such as video acquisition, precise motion control and telemetries requiring fast acquisition rate.

Most of the devices used in Europe belong to US companies and, in some cases, are subject to export restrictions. Some initiatives from European suppliers are ongoing, but the preliminary data shared to date show high power consumption levels, above 100mW. Due to the reduced number of flight qualified chip suppliers, there is a trend to use non-space-qualified products known as COTS (commercial-off-the-shelf) that need to be submitted to costly up-screening tests to validate their performance in space environment. Having a radiation hardened ADC with similar characteristics and reduced power consumption (below 100mW) would certainly enable new applications with higher performances. Additionally, it would guarantee European independence on critical space technologies and would reduce the dependence on COTS and associated screening cost and time.

The main goal of this research project is to investigate a solution for high-speed high-resolution analogue-to-digital signal conversion using European technologies, and the subsequent implementation of a radiation-hardened ADC chip for its use in the space environment. Thus, the main project result will be an ADC with a resolution over 13 bits at 10 to 15 MS/s conversion rate, with reduced power consumption (<100mW), implemented with fully European cutting-edge technologies belonging to the Leibniz Research Institute IHP from Frankfurt (Oder), and ready for formal qualification according to the European Space standards. An additional byproduct/objective is the generation of a rad-hard IP core from the ADC, which is a microelectronics functional block that can be integrated in systems-on-chip. The IP form of the ADC will contribute to expand the design platform of IHP's 130nm technology for space applications, and to reconfirm the promising evaluation results of the basic components in the previous radiation tests.

From the research point of view, this project will provide valuable results on the feasibility assessment of complex mixedsignal designs for space application where the conflicting requirements of high performance, low power consumption and radiation hardness are in place. Additionally, the use of a BiCMOS technology from IHP, where bipolar HBT transistors have at the same time very high performance and an excellent radiation response would contribute to the future European space technology roadmap. Another research result of the project will relate to the optimization of IHP's design flow for highperformance mixed-signal circuits for space applications such as the proposed ADC.

A digitally assisted cascaded MASH 1-1 Delta-Sigma architecture is selected for this purpose. From a space application point of view, the inherent oversampling of this kind of converters can be considered as a multi-vote spread in time that filters

SEE at the cost of increasing system noise. The design could take advantage of the fast HBT devices of BiCMOS technology from IHP, combined with new low-voltage and low-power design techniques. The multi-bit quantizer will be replaced by a time-to digital converter based on a high-speed comparator and a delay locked-loop; both components would be reusable in future designs based on the same technology. The modulator will be based in a MASH 1-1 structure. An ADC with such characteristics is especially demanded for signal conversion in applications involving video data acquisition or high-speed processing of data collected from earth observation satellites, scientific missions, etc.

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V. COMMENTS

No additional comments.