Research on ADC Architectures Suitable for Space Applications and Technology Scaling

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Abstract

For the time being, $\Delta\Sigma$ ADCs used in the space environment mainly target applications in the LF band. This paper presents a research project that explores a $\Delta\Sigma$ ADC architecture for operation in the MF/HF bands. The SG13RH technology, that offers characterization data under radiation and hardened devices, was selected to implement the test vehicles of this research. Additionally, the suitability of the proposed architecture for a future migration to ultra-deep submicron CMOS nodes is also considered.

I. INTRODUCTION

A. Research rationale

Analogue-to-Digital Converters are one of the critical components that engineers seek when designing electronic hardware for space flight projects. Today there are few suitable analogue-to-digital conversion solutions for space-qualified high-speed (from 10 Msps onwards) and high-resolution (13 bits and above) applications such as video acquisition, precise motion control and telemetries requiring fast acquisition rate.

Most of the devices used in Europe belong to US companies and, in some cases, are subject to export restrictions. Some initiatives from European suppliers are ongoing, but the preliminary data shared to date show high power consumption levels (above 100mW). Due to the reduced number of flight qualified chip suppliers, there is a trend to use non-space-qualified products known as COTS (commercial-off-the-shelf) that need to be submitted to costly up-screening tests to validate their performance in space environment. Having a radiation hardened ADC with similar characteristics and reduced power consumption (below 100mW) would certainly enable new applications with higher performances. Additionally, it would guarantee European independence on critical space technologies and would reduce the dependence on COTS and associated screening cost and time.

The main goal of this research project is to investigate a solution for high-speed high-resolution analogue-to-digital signal conversion using European technologies, and the subsequent implementation of a radiation-hardened ADC chip for its use in the space environment. Thus, the main project result will be an ADC with a resolution over 13 bits at 10 to 15 Msps conversion rate, with reduced power consumption (below 100mW), implemented with fully European cutting-edge technologies belonging to the Leibniz Research Institute IHP from Frankfurt (Oder), and ready for formal qualification according to the European Space standards. An additional by-product/objective is the generation of a rad-hard IP core from the ADC, which is a microelectronics functional block that can be integrated in systems-on-chip. The IP form of the ADC will contribute to expand the design platform of IHP's 130nm technology for space applications, and to reconfirm the promising evaluation results of the basic components in the previous radiation tests.

From the research point of view, this project will provide valuable results on the feasibility assessment of complex mixed-signal designs for space application where the conflicting requirements of high performance, low power consumption and radiation hardness are in place. Additionally, the use of a BiCMOS technology from IHP, where bipolar HBT transistors have at the same time very high performance and an excellent radiation response would contribute to the future European space technology roadmap. Another research result of the project will relate to the optimization of IHP's design flow for high-performance mixed-signal circuits for space applications such as the proposed ADC.

B. Technology

The selected SG13 technology is based on 130 nm bulk SiGe BiCMOS process with SiGe npn-HBTs (hetero-junction bipolar transistors) with f_T/fmax = 250/300 GHz. Particularly, the SG13RH design kit includes libraries of rad-hard devices obtained by applying RHBD techniques to the SG13S commercial process. The most relevant technological features are dual gate oxide, STI and n-doped buried layer for inter-device isolation, as well as parametric cells for 3.3V ELT devices. The rad-hard PDK also includes digital libraries with flip-flops that are SEL-free, SEU-tested and SEU-free up to

67 MeV-cm2/mg [1] depending on the selected flip-flop configuration.

It shall be noted that neither doping profiles nor base materials are modified for SG13RH; therefore, no RHBP techniques are involved in its use.

II. ADC FEATURES

A. Target performance

The main target performance for the ADC can be summarized with the following list of requirements:

- Nyquist sampling frequency: 15 MHz
- ENOB: 13
- Power consumption of the analogue core ≤ 7 mW
- Power consumption of the digital core ≤ 36 mW
- No degradation due to TID up to 500 krad(Si).
- No SEL below 67 meV-cm^2/mg.
- No SEU below 67 meV-cm^2/mg.
- No SET (seen at the output) below 20 meV-cm^2/mg.

B. Architecture

A digitally assisted MASH 1-1 $\Delta\Sigma$ ADC architecture was chosen considering its later use for space applications and its suitability for a future migration to smaller nodes. The inherent oversampling of $\Delta\Sigma$ data converters can be considered a multi-vote spread in time that filters SEE at the cost of occasionally increasing the system noise [2]. Additionally, the low order loops included in the architecture avoid possible system instability triggered by a SET [3].

The multi-bit quantizer employs a time-to digital conversion technique based on high-speed comparators and a delay locked-loop. Furthermore, the design takes advantage of the fast HBT devices to implement gm-C based integrators.
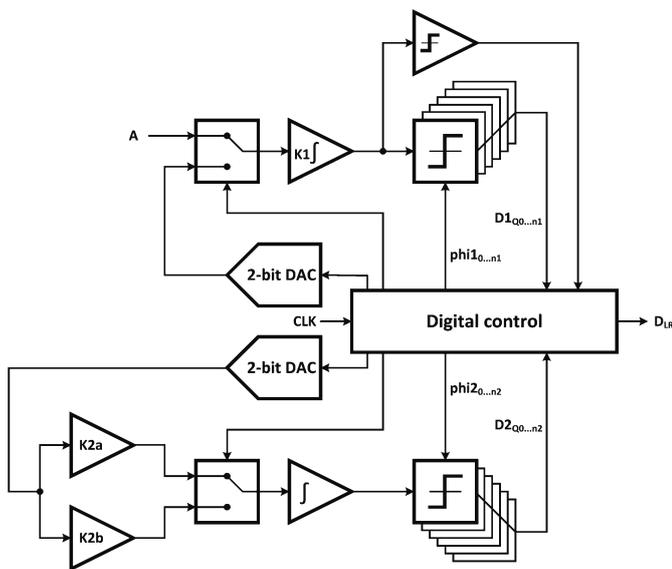
However, an alternative implementation of the integrators will be required for migrating the design to UDSM (ultra-deep submicron) technologies.

C. Applications

This ADC mainly targets TT&C (telemetry, tracking and control) applications. As IP-core the ADC could be integrated in a microcontroller or a more complex SoC (System on Chip).

D. State of the Art

Table 2 collects the performance data of several rad-hard ADCs that operate in the MF/HF bands [4]. As a summary of the analysis of Table 2, it can be said that the proposed design aims to compete in conversion speed with rad-hard pipeline ADCs consuming the same power as rad-hard SAR ADCs more than 10 times slower.

III. RADIATION HARDENING

A. Hardening strategy

The process of hardening the design against radiation effects comprises a maximum of two RHBD attempts and as many radiation tests campaigns; the flowchart depicted in Figure 2 summarizes this hardening strategy. TID and SEE characterization were planned for both test campaigns; however, the characterization under heavy ions was skipped in the first one (additional details of the project status are provided in section IV). Currently, the TID test results of the first test campaign are under analysis to tailor the final design.

B. Analogue core hardening

After a thorough analysis of previous works in the 130 nm bulk CMOS technology node [5][6][7][8], the following RHBD strategy for AMS circuit design has being adopted:

Figure 1: Simplified block diagram of the proposed $\Delta\Sigma$ modulator
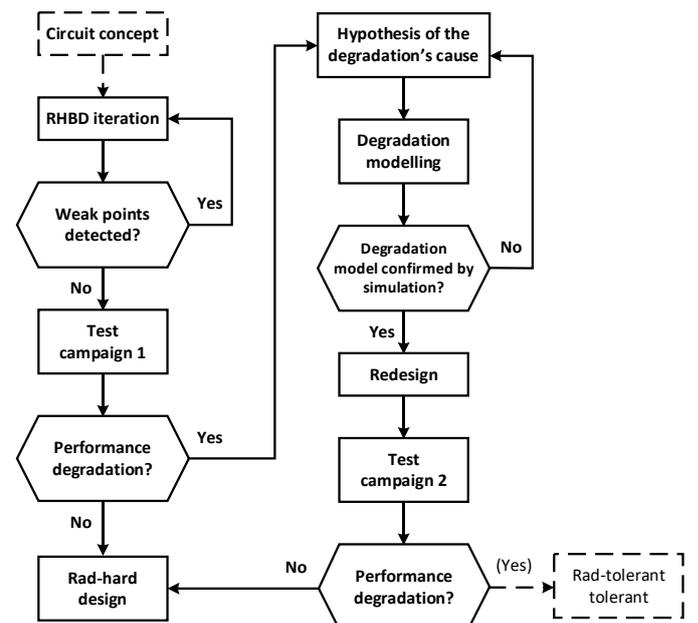

Figure 2: Simplified workflow of the hardening strategy

- Use high density well contacts, especially in isolated nMOS transistors.

- Isolate transistors located in the same well (but in different branches) with guard-bands. However, this recommendation could be skipped to take advantage of the pulse quenching effect.

- Interdigitate dummy drain contacts in multi-finger transistors operating close to their saturation drain-source voltage. Again, this recommendation could be skipped to take advantage of the pulse quenching effect.

- Avoid thick gate oxide transistors.

- Avoid nMOS transistors operating in weak inversion.

- Avoid nMOS transistors in high-performance switches.

- Avoid narrow nMOS transistors: $W_{NMOS} \geq 1$ µm. In case that narrow nMOS transistors could not be avoided, separate the STI from their channel at least 0.45 µm [9].

- Avoid deep n-wells below p-wells (whenever possible).

- Use deep n-wells below n-wells.

This generic strategy has been tailored for each AMS block of the design, depending on its functionality and particularities.

Sensitive nodes to SET in AMS bocks were identified by simulation using the classic approach of a double-exponential current injection in the surveyed node, where the charge collection depth (after an ionizing particle strike) was estimated with a safety margin. Table 1 collects the values used for that purpose.

LET (MeV-cm²/mg)	Q (fC)
5	100
10	200
20	400
30	600

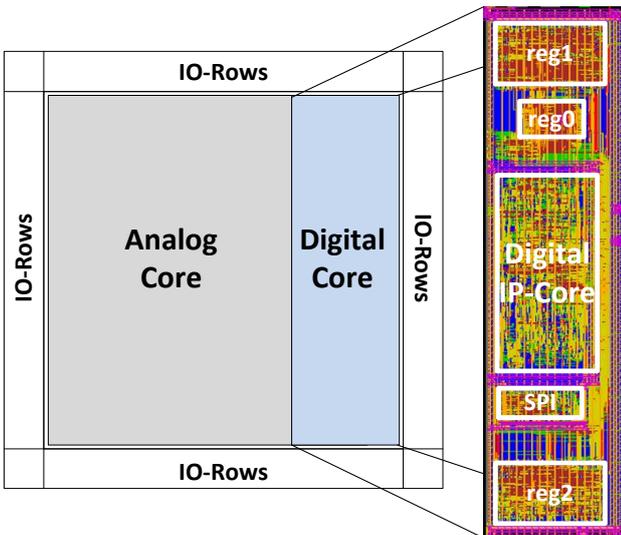Table 1: Simulated collected charge for different ionizing particle's LET.

Figure 3: Modular distribution of the digital core.

C. Digital core hardening

The implementation of the digital core is designed following the traditional RTL-to-GDS digital design flow with hardening measures taken at Gate-Level-Synthesis (GLS) and Place and Route (PnR) stage. An unhardened standard cell library and an additional set of robust flip-flops and transient filters are selected for functional implementation. First, the RHBD-TMR flip-flops are required to correct SEUs induced by high energetic particle strikes. These cells base on the initial concept of [10] and were implemented from unhardened standard cell components. They offer a common flip-flop interface, i.e., one data input pin, and a shared clock and asynchronous control pin comprise the TMR-flip-flop pin-out. The flip-flops are equipped with internal transient filter on the data path, to address SETs which might propagate to the data inputs. Moreover, similarly as published in [11], the layout of these ΔTMR flip-flops provides extra spacing between logically connected, sensitive regions to avoid multiple-bit upsets. In addition, we used special guard-gate buffer (GGB) cells with a delay-chain-guard-gate configuration [12] for SET mitigation of single critical signals.

The behaviour of the digital core is classically described in HDL without introducing any hardening by redundancy. The HDL design is translated to digital library cells during GLS. All behavioural memory cells are mapped to the RHBD-ΔTMR flip-flop counterparts. Critical signals such as asynchronous reset and clock are treated as ideal nets and are protected by GGB gates on input side. The GGB cells are also selected as drivers for sensitive signals crossings to the analogue domain. The physical implementation is performed in hierarchical manner. The modules SPI and the digital IP-core of the ADC-IP are implemented as separate partitions after an initial placement of all components. Figure 2 illustrates the placement of the modules. Moreover, test circuits (reg0-reg2) for future low-power applications are integrated in addition. A hierarchical design is necessary to simplify the derivation of the IP cores afterwards. Robust buffer trees are realized for critical nets and high fan-out nets. The clock trees are implemented with larger-sized, RHBD inverter gates with symmetrical rise and fall transition times.

Nevertheless, two conditions must be met to obtain a radiation-hardened design using the presented design methodology. First, the selected standard cells of the unhardened library must be robust against SEL individually. For a prototype chip, we additionally added a deep N-well which encapsulates the entire digital core. This improves the SEL robustness and the noise performance of the AMS IC in parallel. Second, even though RHBD-TMR flip-flops are selected, bit-faults would accumulate if the clock is inactive or gated for a certain amount of time. Consequently, a continuously running system clock is required to update the values of TMR registers.

IV. PROJECT STATUS

The project considers two manufacturing runs and as many test campaigns. Currently, the test results of the first manufactured IC (cf. its die microphotograph in Figure 4) are being interpreted in the benefit of the final design. Since not

all the functionality was included in the first IC, a full characterization of the ADC was not possible in the first test campaign. The characterization under heavy ions of the first IC was hence replaced by additional radiation simulations of the final design.
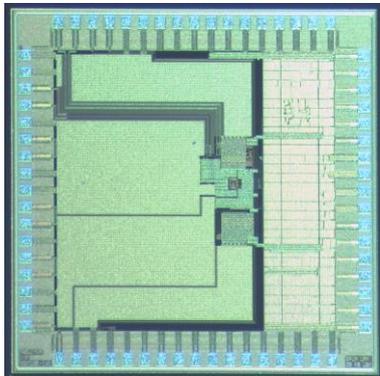

Figure 4: Die microphotograph of the ASIC prototype.

V. CONCLUSIONS

A novel ΔΣ ADC architecture for operation in the MF/HF bands and implemented in a 130 nm bulk SiGe BiCMOS technology was presented. This architecture considers its later use for space applications and its suitability for a future migration to smaller CMOS nodes. The proposed solution could be integrated in a microcontroller or a more complex SoC targeting TT&C applications.

VI. REFERENCES

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ADC	$f_{s,Nyquist}$ MHz	ENOB / res. bits	INL ±LSB	DNL ±LSB	Power mW	Supply V	Arch.	TID krad(Si)	SEL MeV-cm²/mg	SEU MeV-cm²/mg
RHFAD128	1	11.7 / 12	1.1	0.9	6	3.6	SAR	300	125	32
ADC128S102 QML-SP	1	11.7 / 12	0.6	0.5	2.3	3	SAR	100	121.8	5.8
ISL7314SEH	1	13.3 / 14	0.5	0.2	60	5	SAR	75	86	86
UT14AD03	3	12.9 / 14	2	1	100	5	pipeline	300	111	-
9240LP	10	12.2 / 14	2.5	0.7	230	5	pipeline	100	> 120	-
VASP	12	< 12 / 14	2	0.5	275	3.3	pipeline	100	67.7	-
This work (specifications)	15	13 / 14	1	0.5	43	1.2	ΔΣ	500	> 67	> 67

Table 2: Performance comparison of rad-hard ADCs for operation in the MF/HF bands.