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Research on ADC Architectures Suitable for Space Applications and Technology Scaling

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(AMICSA 2021)

Wednesday 26 May 2021

15:25 – 15:45

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- Our continuous activity in R&D&i allows us to create solutions and innovative products based on our technologies for highly demanding sectors where we operate.

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Operations
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SPACE

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AERONAUTICS

SCIENCE

Other project participants:

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Research rationale

- Analogue-to-Digital Converters are key components in space applications.
- Limited number of alternatives within the same frequency range.
- Explore the suitability of ΔΣ ADC architectures in the MF/HF bands.
- Consider an ΔΣ ADC architecture suitable for its migration to ultra-deep submicron technologies.
- Implementation in a Europe-based foundry (IHP).

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Technology

- SG13 technology family:
  - 130 nm bulk SiGe BiCMOS process
  - SiGe npn-HBTs with f_T/f_{max} = 250/300 GHz
- Relevant technological features:
  - dual gate oxide
  - Inter-device isolation: STI and n-buried layer
  - no RHBP
- SG13RH design kit:
  - Libraries of rad-hard devices
  - RHBD techniques to the SG13S commercial process
- Relevant PDK features:
  - parametric cells for 3.3V ELT
  - flip-flops that are SEL-free, SEU-tested and SEU-free up to 67 MeV·cm^2/mg

Reference:
[1] M. Krstic, J. Schmidt, A. Breitenreiter, F. Teply und R. Sorge, Evaluierung einer strahlungsharten Bibliothek in 0.13µm BiCMOS, DLR Bauteilekonferenz 2018.

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Target performance and applications

Target performance:

- Nyquist sampling frequency: 15 MHz
- ENOB: 13
- Power consumption of the analogue core ≤ 7 mW
- Power consumption of the digital core ≤ 36 mW
- No degradation due to TID up to 500 krad(Si).
- No SEL below 67 MeV·cm^2/mg.
- No SEU below 67 MeV·cm^2/mg.
- No SET (seen at the output) below 20 MeV·cm^2/mg.

Applications:

- Telemetry, tracking and control (TT&C).
- IP-core to be integrated in a:
  - Microcontroller
  - System on Chip (SoC)

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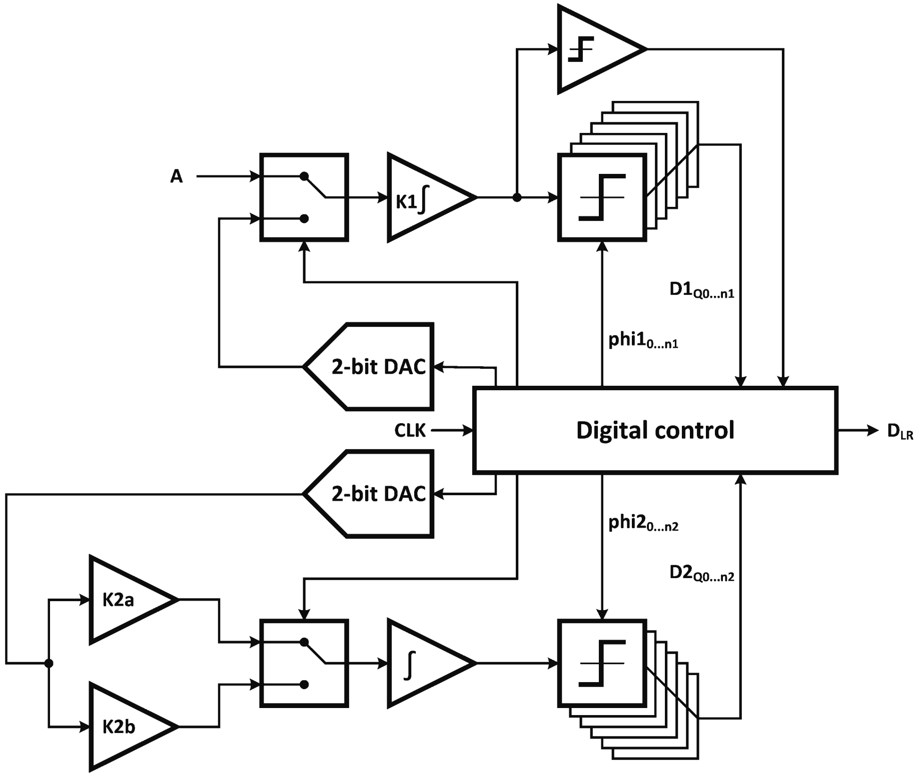
Architecture

- Digitally assisted MASH 1-1 ΔΣ ADC, considering:
  - Its later use in space applications
  - Future migration to smaller nodes
- Selection rationale:
  - Oversampling as a multi-vote spread in time [2].
  - Low order loops to avoid instability triggered by a SET [3].
- Design details:
  - Time-to-digital conversion technique based on DLL.
  - gm-C based integrators taking advantage of the fast HBT.



References:

[2] L. Anghel, D. Alexandrescu, and M. Nicolaidis. Evaluation of a soft error tolerance technique based on time and/or space redundancy. In Proceedings - 13th Symposium on Integrated Circuits and Systems Design, 2000.
[3] Daniel Malagon Perianez, José Manuel de la Rosa, Rocío del Río, and Gildas Leger. Single Event Transients trigger instability in Sigma-Delta Modulators. DCIS), Madrid (Spain), Nov. 2014.

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State of the art

ADC	$f_{s,Nyquist}$ MHz	ENOB / res. Bits	INL ±LSB	DNL ±LSB	Power mW	Supply V	Arch.	TID krad(Si)	SEL MeV·cm²/mg	SEU MeV·cm²/mg
RHFAD128	1	11.7 / 12	1.1	0.9	6	3.6	SAR	300	125	32
ADC128S102 QML-SP	1	11.7 / 12	0.6	0.5	2.3	3	SAR	100	121.8	5.8
ISL7314SEH	1	13.3 / 14	0.5	0.2	60	5	SAR	75	86	86
UT14AD03	3	12.9 / 14	2	1	100	5	pipeline	300	111	-
9240LP	10	12.2 / 14	2.5	0.7	230	5	pipeline	100	> 120	-
VASP	12	< 12 / 14	2	0.5	275	3.3	pipeline	100	67.7	-
This work (specifications)	15	13 / 14	1	0.5	43	1.2	ΔΣ	500	> 67	> 67

References:
[4] E. Pun-García, M. López-Vallejo. A Survey of Analog-to-Digital Converters for Operation under Radiation Environments. MDPI Electronics 2020, 9(10), 1694; 15 October 2020. DOI: 10.3390/electronics9101694

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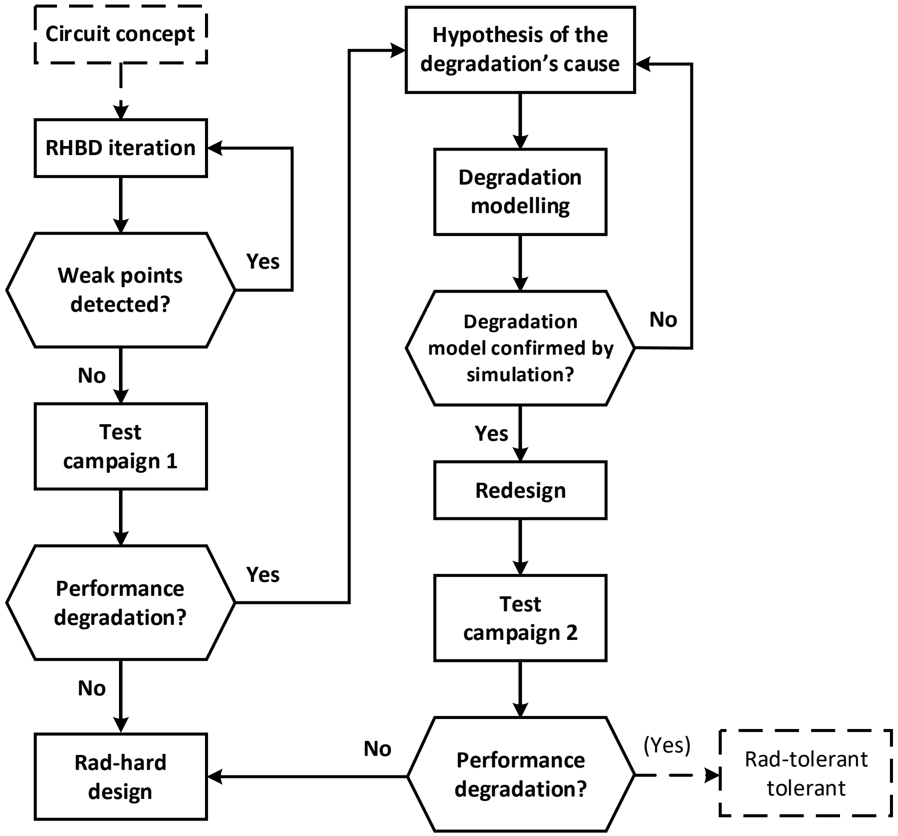
Hardening strategy

- 2 RHBD attempts (1 accomplished, 1 ongoing).
- 2 test campaigns:
  - Test campaign 1 (accomplished):
    - Temperature range [-40, 125] °C
    - TID up to 500 krad(Si).
  - Test campaign 2 (planned):
    - Temperature range [-55, 125] °C
    - TID up to 500 krad(Si)
    - Heavy ions up to LET 67 MeV·cm^2/mg (at least).



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Analog core hardening (1/2)

- RHBD strategy for AMS circuit design [5-9]:
  - Use high density well contacts, especially in isolated nMOS transistors.
  - Isolate transistors located in the same well (but in different branches) with guard-bands. However, this recommendation could be skipped to take advantage of the pulse quenching effect.
  - Interdigitate dummy drain contacts in multi-finger transistors operating close to their saturation drain-source voltage. Again, this recommendation could be skipped to take advantage of the pulse quenching effect.
  - Avoid thick gate oxide transistors.
  - Avoid nMOS transistors operating in weak inversion.
  - Avoid nMOS transistors in high-performance switches.
  - Avoid narrow nMOS transistors: WNMOS ≥ 1 µm. In case that narrow nMOS transistors could not be avoided, separate the STI from their channel at least 0.45 µm.
  - Avoid deep n-wells below p-wells (whenever possible).
  - Use deep n-wells below n-wells.

References:

[5] P. Roche, J. L. Autran, G. Gasiot, and D. Munteanu. Technology downscaling worsening radiation effects in bulk: SOI to the rescue. In Technical Digest - International Electron Devices Meeting, IEDM, 2013.
[6] Oluwole A., *et al.*. Charge collection and charge sharing in a 130 nm CMOS technology. In IEEE Transactions on Nuclear Science, volume 53, pages 3253-3258, dec 2006.
[7] David G. Mavis and Paul H. Eaton. SEU and set modeling and mitigation in deep submicron technologies. In Annual Proceedings - Reliability Physics (Symposium), pages 293-305, 2007.
[8] Balaji Narasimham, *et al.*. Characterization of digital single event transient pulse-widths in 130-nm and 90-nm CMOS technologies. In IEEE Transactions on Nuclear Science, volume 54, pages 2506-2511, Dec 2007.
[9] R. Sorge, *et al.*. JICG CMOS transistors for reduction of total ionizing dose and single event effects in a 130 nm bulk SiGe BiCMOS technology. Nuclear Instruments and Methods in Physics Research, Jan 2021.

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Analog core hardening (2/2)

- Previous strategy tailored for each AMS block.
- Sensitive nodes to SET identified by simulation
  - Classic approach of a double-exponential current injection in the surveyed node
  - Charge collection depth (after an ionizing particle strike) estimated with a safety margin (cf. table).

Simulated collected charge for different ionizing particle's LET

LET (MeV·cm^2/mg)	Q (fC)
5	100
10	200
20	400
30	600

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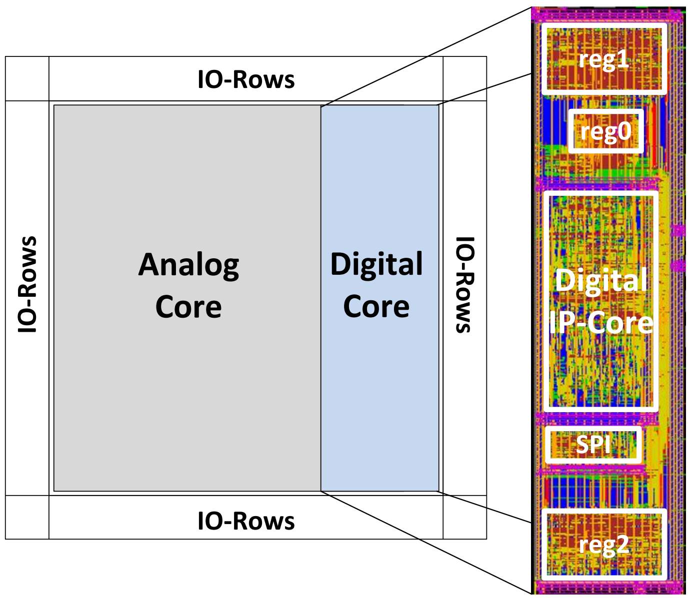
Digital core hardening

- Traditional RTL-to-GDS digital design flow + hardening measures:
  - At Gate-Level-Synthesis using:
    - Unhardened standard cell library
    - Robust RHBD-TMR flip-flops [10]
    - Transient filters (guard-gate buffer cells with a delay-chain-guard-gate configuration)
  - At Place and Route
- No hardening by redundancy at HDL level.
- Additional test vehicles (reg0-reg2) for future low-power applications.

Digital core's modular distribution



References:

[10] V. Petrovic, M. Krstic, "Design Flow for Rad-Hard TMR Flip-Flops," In Proc. IEEE International Symposium on Digital Design of Electronic Circuits and Systems (DDECS), 2015.
[11] Schrape, O.; Andjelkovic, M.; Breitenreiter, A.; Balashov, A. & Krstic, M. Design Concept for Radiation-Hardening of Triple Modular Redundancy TSPC Flip-Flops. In DSD, 2020.
[12] Naseer, R., Draper, J. The DF-dice storage element for immunity to soft errors, 48th Midwest Symposium on Circuits and Systems, 2005.

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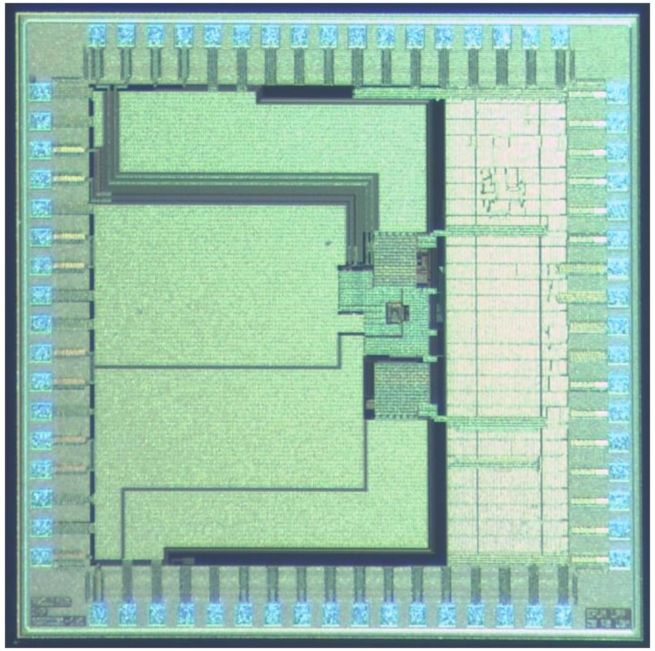
Project status

- 1 manufacturing run accomplished (2 in total).

- 1 test campaign (temperature+TID) accomplished (2 in total):
  - No degradation observed up to 500 krad(Si).
  - Expected behavior at room temperature and 125°C.
  - The second test campaign will include characterization under heavy ions at least up to 67 MeV·cm^2/mg.
  - Heavy ions tests of the prototype were replaced with additional charge injection simulations.

Prototype's die microphotograph



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Conclusions

- Novel ΔΣ ADC architecture for operation in the MF/HF bands is presented:
  - Implemented in a commercial 130 nm bulk SiGe BiCMOS technology
  - Targeting TT&C applications
- Suitable for:
  - Integration in a microcontroller or a more complex SoC (reduced dimensions: ~1.2 x ~1.2 mm^2)
  - Future migration to smaller nodes (time-to-digital conversion approach)

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Thank you for your attention!

Any questions?

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