Update on the Development of the Rad-Hard TM/TC MS-ASIC

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Abstract

This work presents the status of the TM/TC MS-ASIC development (telemetry and telecommand mixed-signal application specific integrated circuit) and describes its final implemented features and target applications. Its usage in RIU/RTU and ICU satellite subsystems will entail weight, volume, and price reduction, in line with the market trend of reduced-size satellite fleets.

I. Introduction

A. *Development rationale*

TM/TC MS-ASIC integrates in a single chip solution the functionality of many electrical and electronic components used on spacecraft subsystems. Its main goal is to replace these components, and hence to reduce area and weight of the PCBs (printed circuit boards) implementing these subsystems. Some examples of units located in the spacecraft platform that could benefit from this replacement are RTU/RIU (remote terminal and remote interface units, respectively); additionally, ICU (instrument control unit) used in the instruments of the payload can also profit from this approach. Consequently, the overall spacecraft can be cheaper, lighter, and more compact, which is aligned with the emerging trend in the space industry towards reduced-size satellite fleets.

B. *Technology*

The TM/TC MS-ASIC is implemented with UMC L180 MM/RF 1.8/3.3V 1P6M p-sub/twin-well CMOS technology, taking advantage of the DARE180U libraries. In fact, the available catalog of DARE180U IO cells was enlarged in the frame of the project (and in the benefit of the DARE users' community) to cover the cold-spare functionality of the digital communication interface. To reduce risks and development time, the IP-core of a ΔΣ modulator with suitable performance was reused in this development; additionally, other available IP-cores were tailored with additional functionalities (low-dropout regulators with over-voltage and over-current protections) or enhanced performances (internal voltage reference). The design has been hardened against radiation effects applying validated techniques in previous projects. Moreover, the analog channels have been designed to allow cold-spare operation.

II. System Description

A. *Main features*

1) *Communications and configurations*

Due to its reliability and simplicity, a redundant SPI is the selected interface to communicate with the TM/TC MS-ASIC. Its implementation allows multiple devices sharing the same bus and a clock frequency in the [10; 20] MHz range. The TM/TC MS-ASIC configuration and information extraction (internal status and telemetries measurements) are performed through this interface.

Configurations that are both readable and writable have different addresses for each access mode to avoid possible software errors. Furthermore, some configurations can be consulted redundantly accessing indirectly to a particular ad hoc address.

Some specific registers can be written at the same time in several TM/TC MS-ASIC instances (software reset functionalities in 'broadcast mode'). This functionality allows synchronizing the telemetries and telecommands of multiple TM/TC MS-ASICs within the same system.

2) *Telemetries*

TM/TC MS-ASIC can acquire up to 27/54 differential/single-ended analog telemetries (limited in band up to 50 kHz, with at least 11 ENOB) that are converted to the digital domain. The acquisition sequence of the telemetries is configured on-chip through the SPI. Acquired telemetries are stored in a double depth table that collects first and current acquisition that can be consulted through the SPI. Fifty-four IO ports are reserved as inputs of the telemetry channels.

Telemetry channels are grouped by pairs to handle one differential or two single-ended signals. Single-ended channels can be biased by means of an on-chip programmable current source.

Telemetries can be acquired with a maximum absolute error of 1% for the whole [-55; 125] ºC operational temperature range. This 1% accuracy is independent of the

resultant manufacturing process. All the acquisitions can be configured for thermistor acquisition enhancing the usability of the device.

Switching among channels is the default acquisition mode. In this mode, the fastest acquisition rate is one telemetry acquisition each 10 µs. However, the TM/TC MS-ASIC can be configured to acquire continuously a single channel.

3) Telecommands

The TM/TC MS-ASIC allows generating up to four separate telecommands at once, each being configurable independently as bi-level, single pulse, or PWM. For synchronization purposes, pulse and PWM options allow configuring their time reference. Four IO ports (one per telecommand) are reserved for this functionality.

The TM/TC MS-ASIC can autonomously execute some preconfigured telecommands depending on the acquired analog measurements. This monitoring functionality is applicable to the three operating modes of the telecommand (bi-level, pulse, and PWM) and can be configured with the following degrees of freedom: monitored telemetry channel, active polarity (high or low), conditional levels (upper and lower limits of the monitored channel). When the monitoring condition is configured through SPI (and the monitoring functionality enabled), the telecommand is not activated until the monitored telemetry channel fulfils its monitoring condition. In fact, when the monitoring condition is asserted, the respective telecommand behaves as it was activated through the equivalent SPI command. On the other hand, when the monitoring condition is unasserted, the respective telecommand behaves as it was deactivated through the equivalent SPI command.

4) Status

The TM/TC MS-ASIC can interpret analog acquisitions binarily comparing them with pre-configured threshold values. Up to two threshold levels can be configured to allow hysteretic monitoring. Each telemetry has a corresponding single-bit register distributed in four 16-bit APB registers.

B. Other on-chip solutions

1) Calibration

The gain and offset errors of the analog signal path can be compensated using two analogue channels. This calibration is optional (disabled by default) and needs to be enabled through SPI. Once enabled, all the acquisitions will be gain- and offset-compensated. If the conversion range is exceeded after compensation, the acquisition is saturated to the corresponding conversion limit. Furthermore, the internal voltage reference can be calibrated through SPI to achieve a ±0.5% precision with respect to its 1.25V nominal value.

2) Signal ranges above maximum ratings

Signal ranges at system level exceed the absolute maximum rating of the DARE180U IO cells used [3]: [-0.3; 3.63] V. Single-ended signals at system level can be within the [0; 10] V range. Differential signals up to the [-10; 10] V range with a common-mode in the [-1; 1] V range. Differential measurements are optimized by means of an on-chip a common-mode control loop (see Figure 1).

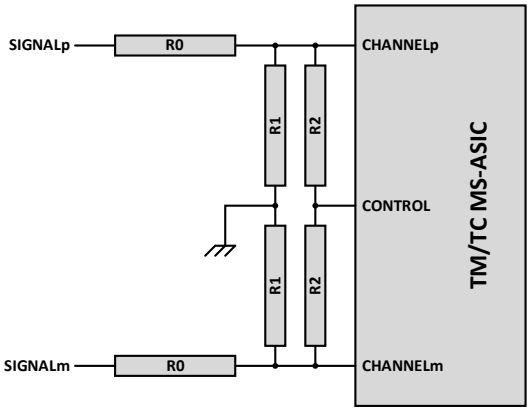

Figure 1: Differential measurement concept

3) Over-current alarms

Internal LDO regulators include an over-current alarm functionality to prevent from destructive SEL (single event latch-up). If the current through the pass element transistor exceeds a pre-defined current (~3 times the expected current consumption in worst-case conditions), the corresponding 1.8V core power supply is cycled several times until the over-current is no longer detected. In case of a permanent over-current, the 1.8 V core supply is cut indefinitely; this permanent state can be overridden with a power-cycle of the 3.3V input voltage of the LDO regulator.

4) Configurable latency

The different nature of the possible telemetries (single-ended/differential, biased or not, different voltage ranges, etc.) entails a stabilization period after channel switching. The worst-case settling time of the analog channels can be configured to warrantee a trustworthy telemetry acquisition minimizing the telemetry latency.

The digital filter at the end of the acquisition data path is highly configurable. It allows configuring its number of stages (to trade effective resolution of the acquisition for a smaller latency) and the decimation factor (to keep a constant signal bandwidth for the different clock frequency options).

5) Testability

Including testability in a new development is highly recommended to optimize the development time of a successful design. Observability of key internal nets and registers is extremely recommendable for debugging and/or confirming the expected design behaviour. For this purposes, TM/TC MS-ASIC includes an analogue test bus (ATB) and four digital scan chains (DSC).

ATB brings access to differential signal path nets, voltage references, bias voltages, and regulated supplies. Its simplified block diagram is depicted in Figure 2. ATB can work in single-ended or differential mode, depending on the nature of the internal net required to be monitored. In single-ended mode, ATB allows monitoring two different single-ended nets at once (useful to identify crosstalk or net dependency). ATB has two access options by sharing four IO

ports with telemetry channels. This implementation allows testing all the telemetry channels without sacrificing any during ATB usage. ATB allows disabling and bypassing the analogue voltage buffer at its output, which gives direct access to the selected internal net(s). ATB is configured through SPI.

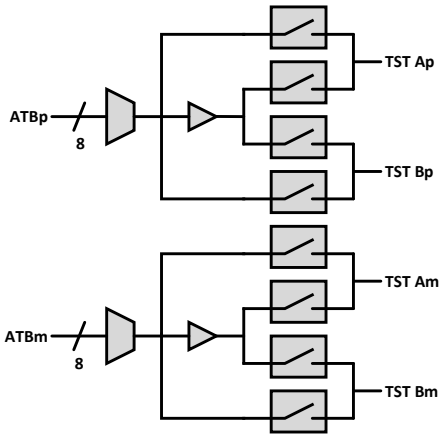

Figure 2: Block diagram of the analogue test bus

6) Reduced number of IO ports

A compromise to minimize the occupied area in the system board was reached with a 100-pin package, considering the amount of telemetry channel inputs, telecommands, communications ports, analogue references, and power supplies. It was hence decided to assemble the dice in a custom CQFP-100. Testability ports (for ATB and DSC) are shared with the functional ports. However, analog and digital core supply ports were included to provide additional decoupling to the internal LDO regulators. Particularly, several 3.3V power supply pads were double bonded.

C. Block Diagram

The layout of the TM/TC MS-ASIC is presented in Figure 3 and its block diagram in Figure 4. Each block is briefly explained below:

- B1 – LDO ANA block generates the 1.8V analogue core supply from the 3.3V external supply. It includes an over-current alarm.
- B3 – LDO DIG block generates the 1.8V digital core supply from the 3.3V external supply. It includes an over-current alarm.
- B4 – SENSOR BIASING block provides the bias capability of the telemetry channels.
- B6.1 – MUX block selects the telemetry channels to be acquired. Its implementation allows cold-spare operation.
- B6.2 – SIGNAL CONDITIONNING block fits the signal coming from the telemetry channels for the ΔΣ modulator input.
- B6.3 – LSSB MODULATOR block (ΔΣ modulator) is the first stage of the digital conversion of the acquired telemetry.
- B6.4 – DIGITAL FILTER block filters and decimates the 1-bit output of the ΔΣ modulator to obtain the final resolution.
- B6.5 – OUTPUT DATA BUFFER block records the acquired telemetries
- B7 – STATUS COMPARATOR compares the acquired telemetries with a registered threshold level.
- B8.1 – V REF block generates the internal voltage references for the ΔΣ modulator.
- B8.2 – I REF block generates the internal current references for the rest of the analogue core blocks.
- B9.1 – MAIN REF provides a stable voltage reference for other blocks of the analogue core. This reference can be provided either by the internal bandgap reference or externally.
- B9.2 – INT REF block generates the bias voltage for external attenuators based on resistive networks.
- B10 – V SUPERVISOR block is a window comparator (acquired telemetry versus registered threshold levels) implemented digitally.
- B11 – RESET MANAGEMENT block generates the internal reset signal for TM/TC MS-ASIC.
- B12 – REFERENCE REG block is a register bank. It records the threshold levels.
- B13 – PWM GEN block implement the PWM functionality of telecommands.
- B14 – STA REG block is a register bank. It stores the status of TM/TC MS-ASIC.
- B15 – ADC REG block is a register bank. It stores the configurations for the digital conversions of the telemetries.
- B16 – ADC TIMING CONTROLLER block manages the timing configurations of the digital conversions of the telemetries.
- B17 – MISC REG block is a register bank. It stores additional registers not considered in the other register banks.
- B18 – SPI/SSB block implements the communication interfaces.
- B19 – COMMAND block drives the telecommands using the information stored in other blocks.

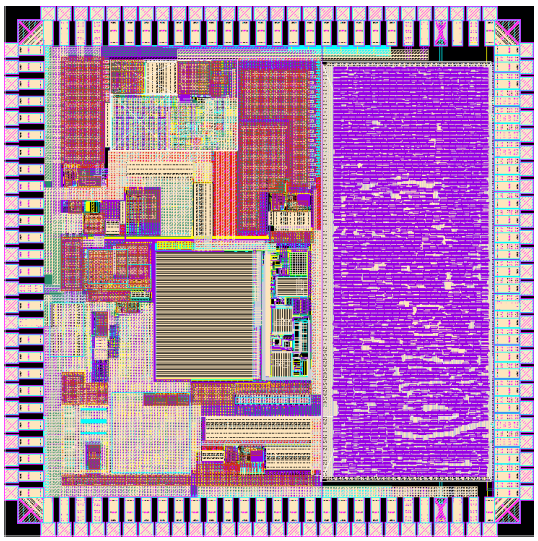

Figure 3: Layout of the TM/TC MS-ASIC

III. Target Applications

This device is intended to be used by Remote Interface/Terminal Units (RIUs & RTUs) and Instrument control Units (ICUs) for telemetry acquisition.

RIU/RTU units are, together with the OBC (On-Board Computer), a core element of the Data Handling Subsystem on all Satellites Platforms. The mission of the RIUs / RTUs is to provide support to the OBC in the control of the rest of the platform subsystem, among others, the AOCS (Altitude and Orbit Control System), the propulsion and the thermal control. This support includes on one hand the drivers of all actuators: Valves, Pyros, Heaters, MTQ (magnetorquer) and a wide range of platform specific devices, and, on the other hand, collect and process the platform Telemetries to be dispatched to ground via the OBC.

This functionality implies a very wide number of Input/Output Interfaces (I/Os) which represent a high number of electronic components defining the size and the recurring cost of the units. Typically, a single discrete board of Standard I/Os has around 2,500 EEE part and a RIU can include up to 4+4 I/O Boards. This important fact is the origin for the high cost of such type of units.

In similar way to the RIU/RTU, the ICU is one of the key elements of the satellite's instrument in charge of performing tasks of data processing and command and control of the downstream elements of the instrument. In this role, one of the main functions of the ICU is the Interface Module which generates commands and acquires and monitors logic statuses and analog telemetries. Depending on the instrument needs, one ICU could require up to 2+2 boards of this type.

This ASIC will allow to encompass a relevant number of I/O interfaces, as well as other ancillary elements reducing drastically the number of discrete parts on the boards and therefore reducing consequently the surface and the price of the unit.

IV. Project Status

The validation of the design obtained in the first manufacturing run is about to begin. The imminent test campaign aims an electrical characterization of all the presented functionalities in the [-55; 125] ºC temperature range, up to 150 krad(Si) of TID and up to 75 MeV-cm^2/mg heavy ions' LET. No performance degradation is expected in this temperature range and below 50 krad(Si) of TID. Furthermore, no SEL is expected under heavy ions at least up to 75 MeV-cm^2/mg and no SEU, SEB, SEFI, or SEGR at least up to 37 MeV-cm^2/mg.

V. Conclusions

This paper presents the status of development of the TM/TC MS-ASIC and the main features of this device. A brief description of the target applications has also been provided. Its usage in RIU/RTU and ICU will entail weight, volume, and price reduction of this satellite subsystems, in line with the market trend of reduced-size satellite fleets.

VI. Acknowledgments

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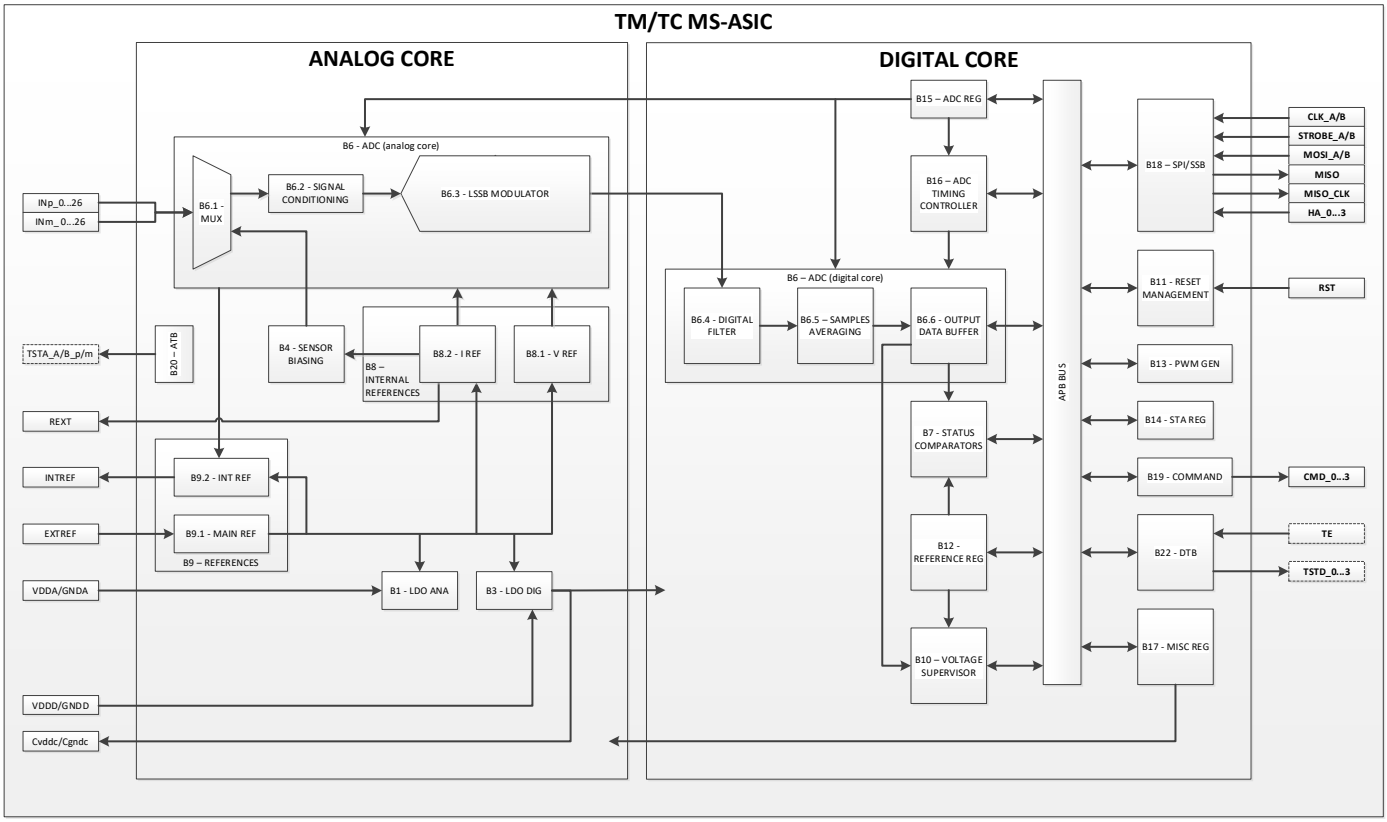

Figure 4: Block diagram of TM/TC MSA