Update on the Development of the Rad-Hard TM/TC MS-ASIC

8th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications
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17:20 – 17:40
About our company: ARQUIMEA

We believe in technology as a driver for social development and progress.

Our continuous activity in R&D&i allows us to create solutions and innovative products based on our technologies for highly demanding sectors where we operate.

ARQUIMEA is a cross-sectoral international technology company

Turnover
71 M€

Professionals
380+

Operations
25+

Countries
About our company: ARQUIMEA AEROSPACE & DEFENCE

Other project participants:

- AIRBUS Crisa
- ESA European Space Agency
- imec
Development rationale

• Single chip solution that integrates many electrical and electronic components used on spacecraft subsystems (such as RTU/RIU or ICU).

• Area and weight reduction of the PCBs implementing spacecraft sub-systems.

• Cheaper, lighter, and more compact spacecrafts (as required in reduced-size satellite fleets).
Technology

• Process: UMC L180 MM/RF 1.8/3.3V 1P6M p-sub/twin-well CMOS

• DARE180U libraries v5.7
  • Enhanced with 10 additional cells (OUT3VTRCS4/8/12/16/24 and OUT3VTRCSRCS4/8/12/16/24) in the frame of the project.

• IP-cores:
  • ΔΣ modulator designed from MF Cosmic Vision ESA Project (4000101556/10/NL/AF).
  • Other IP-cores (bandgap reference and LDO regulators, from the same ESA project) were enhanced.
Main features

- Communication and configurations:
  - Redundant SPI [10; 20] MHz
  - Different addresses for readable & writable configurations
  - Broadcast mode

- Telemetries:
  - Up to 27/54 differential/single-ended telemetries converted to the digital domain
  - Configurable acquisition sequence / continuous mode
  - Current bias capability (for single-ended telemetries): 10 µA / 100 µA / 1 mA
  - Signal bandwidth: 50 kHz
  - 11 ENOB (worst case with high-resolution configuration)

- Cold-spare operation

- Telecommands:
  - Up to 4 simultaneous telecommands
  - Bi-level, Pulse and PWM operating modes
  - Configurable time references (phase shift)
  - Possibility of autonomous operation:
    - Configurable associated telemetry
    - Two threshold levels for hysteretic monitoring
    - Configurable active polarity

- Status:
  - One status bit per telemetry
  - Two threshold levels for hysteretic monitoring
Other on-chip features

- **Calibration:**
  - Gain and offset of the *analog signal path* using two channels (disabled by default).
  - Temperature dependent gain and offset of the *internal voltage reference*.

- **High-voltage signal range:**
  - On-chip common-mode control (CMC)
  - Single-ended: [-1; 11] V
  - Differential: [-10; 10] V_{dpp} / [-1; 1] V_{CM}

- **Over-current alarms:**
  - In LDO regulators (for core supply).
  - Cyclic / Permanent.

- **Configurable latency:**
  - Discarded modulator samples after a channel switch.
  - Number of stages used in the digital filter.

- **DFT:**
  - Scan chains x4
  - Redundant analog test bus

- **Reduced number of IO ports:**
  - Custom CQFP-100
  - Test ports shared with functional ports
  - Double bonding for 3.3V supply ports
Block diagram

Conclusions

TM/TC MSA layout
Block diagram

Analogue Core blocks:

B1 – LDO ANA generates the 1.8V analogue core supply from the 3.3V external supply.
B3 – LDO DIG generates the 1.8V digital core supply from the 3.3V external supply.
B4 – SENSOR BIASING provides the bias capability of the telemetry channels.
B6.1 – MUX selects the telemetry channels to be acquired.
B6.2 – SIGNAL CONDITIONNING fits the signal coming from the telemetry channels for the ΔΣ modulator input.
B6.3 – LSSB (ΔΣ modulator) is the first stage of the digital conversion of the acquired telemetry.
B8.1 – V REF generates the internal voltage references for the ΔΣ modulator.
B8.2 – I REF generates the internal current references for the rest of the analogue core blocks.
B9.1 – MAIN REF provides a stable voltage reference for other blocks of the analogue core. This reference can be provided either by the internal bandgap reference or externally.
B9.2 – INT REF generates the bias voltage for external attenuators based on resistive networks.
B20 – ATB collects critical signals from the analog core for external monitoring.

Digital Core blocks:

B6.4 – DIGITAL FILTER filters and decimates the 1-bit output of the ΔΣ modulator to obtain the final resolution.
B6.5 – SAMPLES AVERAGING
B6.6 – OUTPUT DATA BUFFER records the acquired telemetries
B7 – STATUS COMPARATOR compares the acquired telemetries with a registered threshold level.
B10 – V SUPERVISOR is a window comparator (acquired telemetry versus registered threshold levels) implemented digitally.
B11 – RESET MANAGEMENT generates the internal reset signal for TM/TC MS-ASIC.
B12 – REFERENCE REG is a register bank. It records the threshold levels.
B13 – PWM GEN implement the PWM functionality of telecommands.
B14 – STA REG is a register bank. It stores the status of TM/TC MS-ASIC.
B15 – ADC REG is a register bank. It stores the configurations for the digital conversions of the telemetries.
B16 – ADC TIMING CONTROLLER manages the timing configurations of the digital conversions of the telemetries.
B17 – MISC REG is a register bank. It stores additional registers not considered in the other register banks.
B18 – SPI/SSB implements the communication interfaces.
B19 – COMMAND drives the telecommands using the information stored in other blocks.
B22 – DTB is the digital test bus.
**Target Applications**

**Satellite Spacecraft**

- **AOCS**: Altitude and Orbital Control System
- **CDMU**: Command and Data Management Unit
- **OBC**: On-Board Computer
- **PCDU/PCU**: Power Control (and Distribution) Unit
- **P/L**: Payload
- **P/F**: Peripheral
- **SMU**: System Management Unit
- **TTC**: Telemetry Traffic Control
- **X/Ka TX**: X or Ka band Transceiver

Reference:
Target Applications

AS1000 RIU

Modular-RTU

M-RTU Analogue Housekeeping Modules

M-RTU Digital IO Modules

Reference:
Project status

ESA project (GSTP) to achieve a TRL5 design.

A preliminary validation of 30 EM chips with a standard CQFP-100 package is about to begin:

- **Temperature range:** [-55; 125] °C  ➔ **Expected:** No performance degradation in the full range.
- **TID:** up to 150 krad(Si)  ➔ **Expected:** No performance degradation at least up to 50 krad(Si).
- **LET:** up to 75 MeV·cm²/mg  ➔ **Expected:** No SEL up to 75 MeV·cm²/mg, No SEU, SEFI, SEB or SEGR up to 37 MeV·cm²/mg.
Conclusions

- Final features of the TM/TC MS-ASIC:
  - Custom CQFP-100
  - SPI
  - Telemetries
  - Telecommands
  - Status
  - Calibration
  - High-voltage signal range
  - Over-current alarms
  - Configurable latency
  - DFT
  - Reduced number of IO ports

- Target applications:
  - RIU/RTU
  - ICU

- Usage benefits:
  - Weight, volume and price reduction.
  - Suitable for reduced-size satellite fleets.
Thank you for your attention!

Any questions?

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