# ROADMAP

# Future very integrated avionic for satellite platform base on hi-rel component NanoXplore NG-Ultra and Dahlia SoC

## DSO/TB/ET, DSO/TB/LV, DSO/AVI/AV, DSO/AVI/VS CNES

(Presenter: L. CLARAC DSO/AVI/AV)



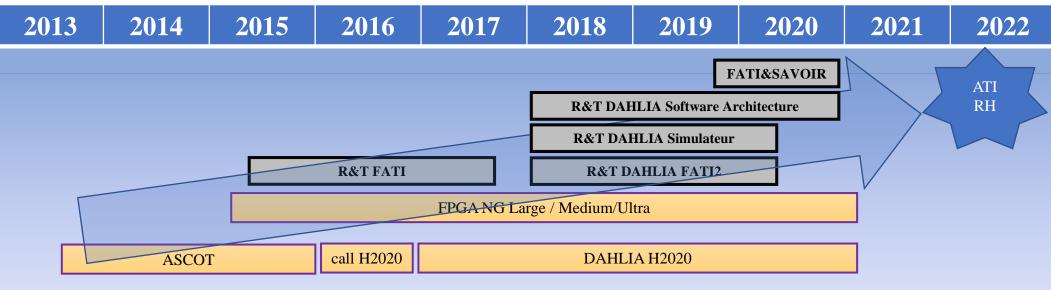
ADCSS 14/11/2019



### Context

# □ Initiative for Hi-Rel solutions for avionic & space applications

- Preparation of the next generation of de System-On-Chip in the frame 2020-2025
- ✓ ASCOT (Arm Spacecraft Controller On 65nm Technology) and FATI ("Future Avionic Très Intégrée")
- ✓ Assessment of the impacts of more compact on-board avionics systems
- ✓ Development of competitive FPGA products by European company NanoXplore



□ CNES Research & Technologies Plan and the Projet H2020 DAHLIA

## **Context: Projet DAHLIA H2020**

DAHLIA is an answer to the H2020 topic "COMPET-1-2016: Critical Space Technologies for European Strategic Non-Dependence" http://dahlia-h2020.eu

DAHLIA solution is an ARM-based System on Chip implemented in 28nm FDSOI technology designed to boost competitiveness and ensure strategic non dependence of future European Space

# H2020 project organization



Consortium: 7 partners – 4 countries

- ST France, coordinator
- Airbus D&S Germany& France
- Thales Alenia Space Italy& France
- ISD Greece& NanoXplore France



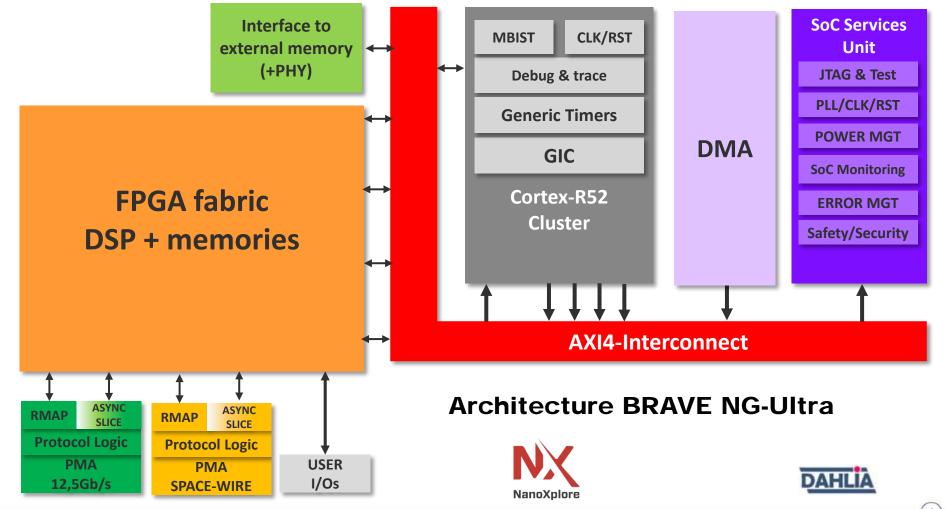






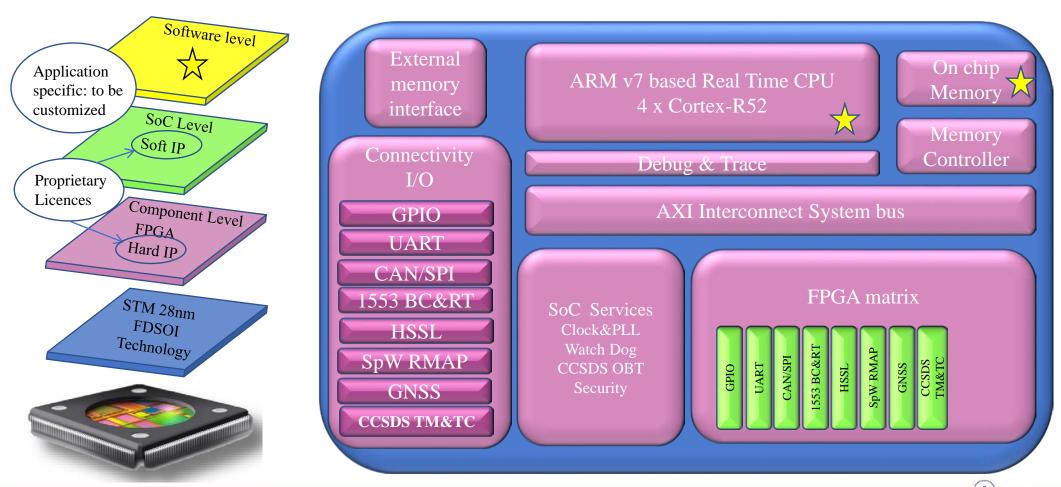
Very Integrated Avionic Architecture Roadmap for space application based on Hi-rel component NanoXplore NG-Ultra / Dahlia



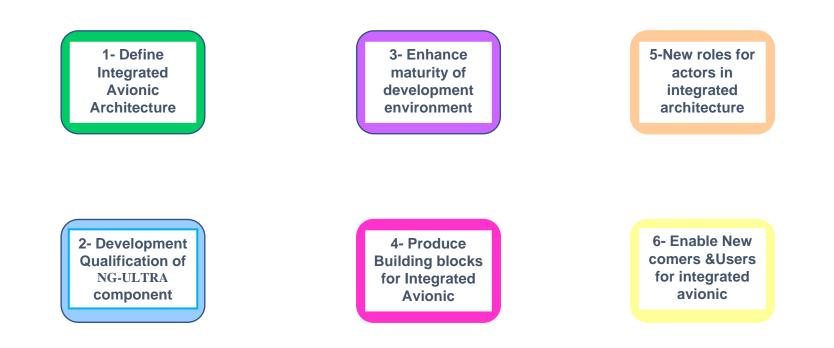




## **Context: Multi Processor SoC defined in H2020 DAHLIA project**









# **1- Define integrated Avionic Architecture**

- **1.1 Integration level definition: HW/SW partining integration choice**
- ✓ Choice of centralises or de-centralize architecture
- ✓ Choice of functions to integrate with impact on functions and equipment design

### **1.2 Integration of new functions**

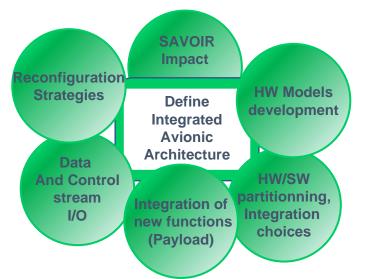
Impact on architecture of payload function integration

### 1.3 Data and control stream analysis

Choice of the interfaces and buses

## **1.4 Reconfiguration and redundancy strategy**

- ✓ Failure modes and reset tree, Reliability Analysis
- ✓ Use of DTC and eTM
- **1.5 Identification of impact on SAVOIR**
- **1.6 HW models development**
- ✓ EBB or EM OBC module for a proof of concept of integrated architecture





# 2. Development and qualification of NanoXplore NG-ULTRA component

#### 2.1 Development of the multi-processor SoC solution

Definition and development of SoC in H2020 DAHLIA project + NG-ULTRA component

#### 2.2 Space qualification of the component and the packaging

- ✓ Technology 28nm FDSOI qualification
- ✓ NG-ULTRA component and packaging qualification

#### 2.3 Commercial offer for NG-ULTRA product

- ✓ NG-ULTRA is part of the NanoXplore product line
  - Development environment for hardware design: NanoXmap solution
  - Starter Kit and evaluation board
  - Hardware and Software libraries





# 3. Enhance maturity of development environment

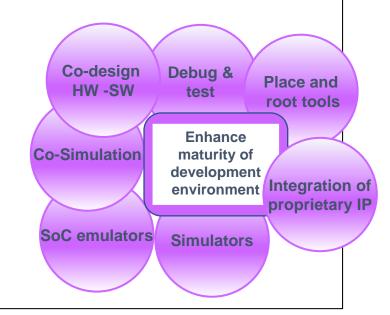
#### 3.1 Simulation environment for application and system with NG-Ultra

- Co-design d'IPs HW/SW
- o Co-simulation RTL for complex IP
- o Proprietary IP integration

### 3.2 SoC Emulator & NG-Ultra virtual platform

### 3.3. Simulators

- Software development environment for early Flight SW
- o System simulator for operations
- o System simulator for AIT





# 4- Produce Building blocks for integrated avionic

#### 4.1 Software

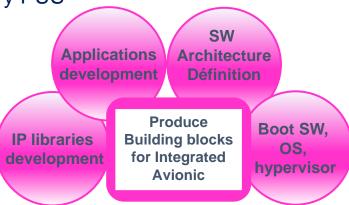
- Software architecture definition
- Development and qualification of OS, Hypervisor, Library PUS
- Development of applications
- ✓ IP libraries

#### 4.2 Hardware IP librairies (in the FPGA matrix)

- ✓ SoC services and specific
- Avionic functions
- Specific application

#### **4.3 Intellectual Property and licences**

- Ensure acceptable licences condition for tools and libraries
- Equipment provider need to develop proprietary IPs (and new hardware) for integration in the architecture





# 5- New roles for actors in integrated architecture

- 5.1 List Equipments and impacted suppliers
- Avionic candidates functions for integration are numerous: SCAO, Star tracker, GNSS, TM/TC...
- ✓ Only numerical functions will be executed on the System-on-Chip
- 5.2 New products Portfolios for the equipment providers
- ✓ New product development
- ✓ IP of the integrated function to be integrated in the SoC
- 5.3 Support « HW to IP » transition





Access to IP

portfolios

Access to

**Development** 

environment

**Enable New** 

comers &Users

for integrated avionic

# 6- Enable New comers &Users for integrated avionic architecture

#### 6.1 Objectives

Future areas of work

- ✓ Identify key IPs for space applications and enable their development for NG-ULTRA
- Ensure that all the documentation and tools are available to new comers to use the SoC
  - Lab for scientific missions
  - Small companies
  - Equipment suppliers

#### 6.2 What is needed ?

- ✓ NG-ULTRA product with development tools available by NanoXplore
- Simulations tools for IP development (before the availability of the component)
- Availability of building blocks (component with development board, simulators, IP library)
- ✓ Initiate strategic IPs development with affordable licences conditions for new comers





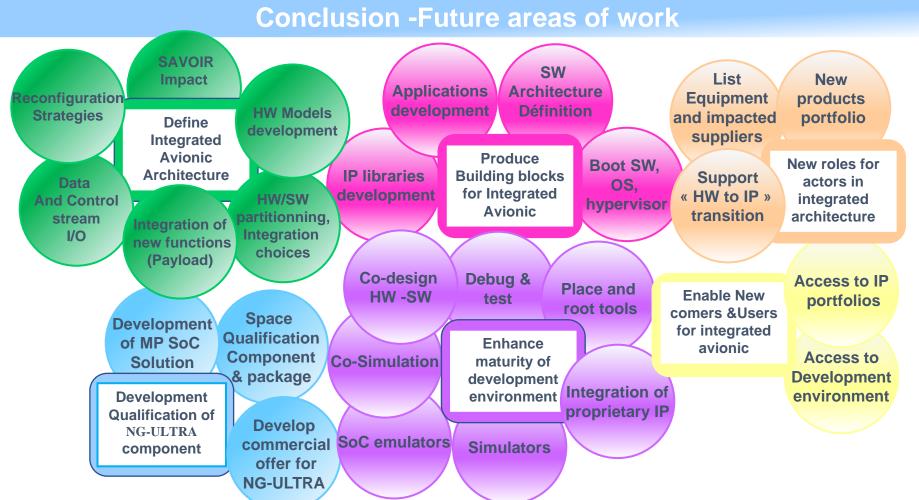
# CONCLUSION

- Building block for very integrated avionic core need to be available in 2020-2021
  - NG-ULTRA prototypes
  - OBC architectures
  - IP portfolios
  - Software architecture
  - Simulations tools

□ Need to enable the use of the technology by new comers: scientific community, small companies: Documentation, licences, test benches

□ Prepare evolutions of SAVOIR specifications with ESA and industry to take into account specificities of very integrated avionic





# End of the presentation Thank you

