Future Highly Integrated Avionics Architectures

ADCSS 2019

DEFENCE AND SPACE

AIRBUS

Agenda

1. Future DHS architecture
2. Equipment modular architecture
3. On-Board SW architecture
4. Keys trade-offs – FATI2
5. Baseline RU
6. Essential TC
7. Essential TM
8. Airbus workplan for Oscar-Ultra

NG core avionics architecture trends

Multi-core ARM processor module (NG Ultra)

Time & Space partitioning OS

New generation middleware and application layer technology with low missionisation cost. Application SW sees a standard interface whatever the underlying hardware. Service oriented

Centralised AOCS sensor processing.

Embedded / adaptable security. (from civilian grade to military).

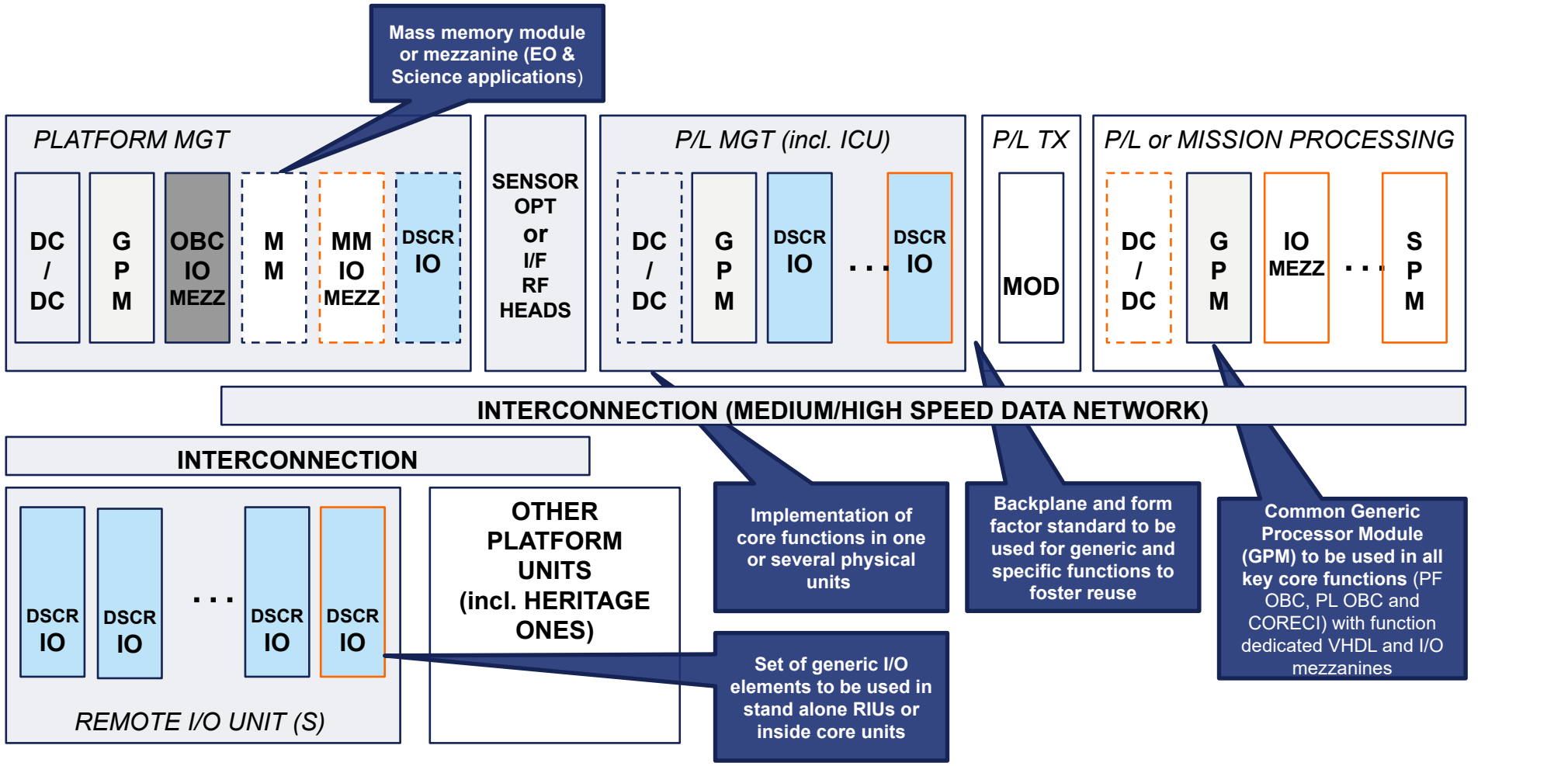
Physical centralisation in a modular architecture. Hardware and basic SW commonalization across digital units (e.g. same processing core customized via mezzanines).

Interface to other units

- **Minimisation of discrete I/Os**
- **Multi-protocol data concentrator compatible of various data link types to accommodate large set of sensors. Connectors doesn't fit well with small units.**
- **Local bus (to be selected) for IO decentralisation.**
- **Network to accommodate new intelligent equipment (esp. P/L) (intra modular unit and between them). (Space Fiber is a candidate)**

Growth potential to accommodate advanced specific processing. Partial routing of FPGA.

Future DHS architecture (Functional)



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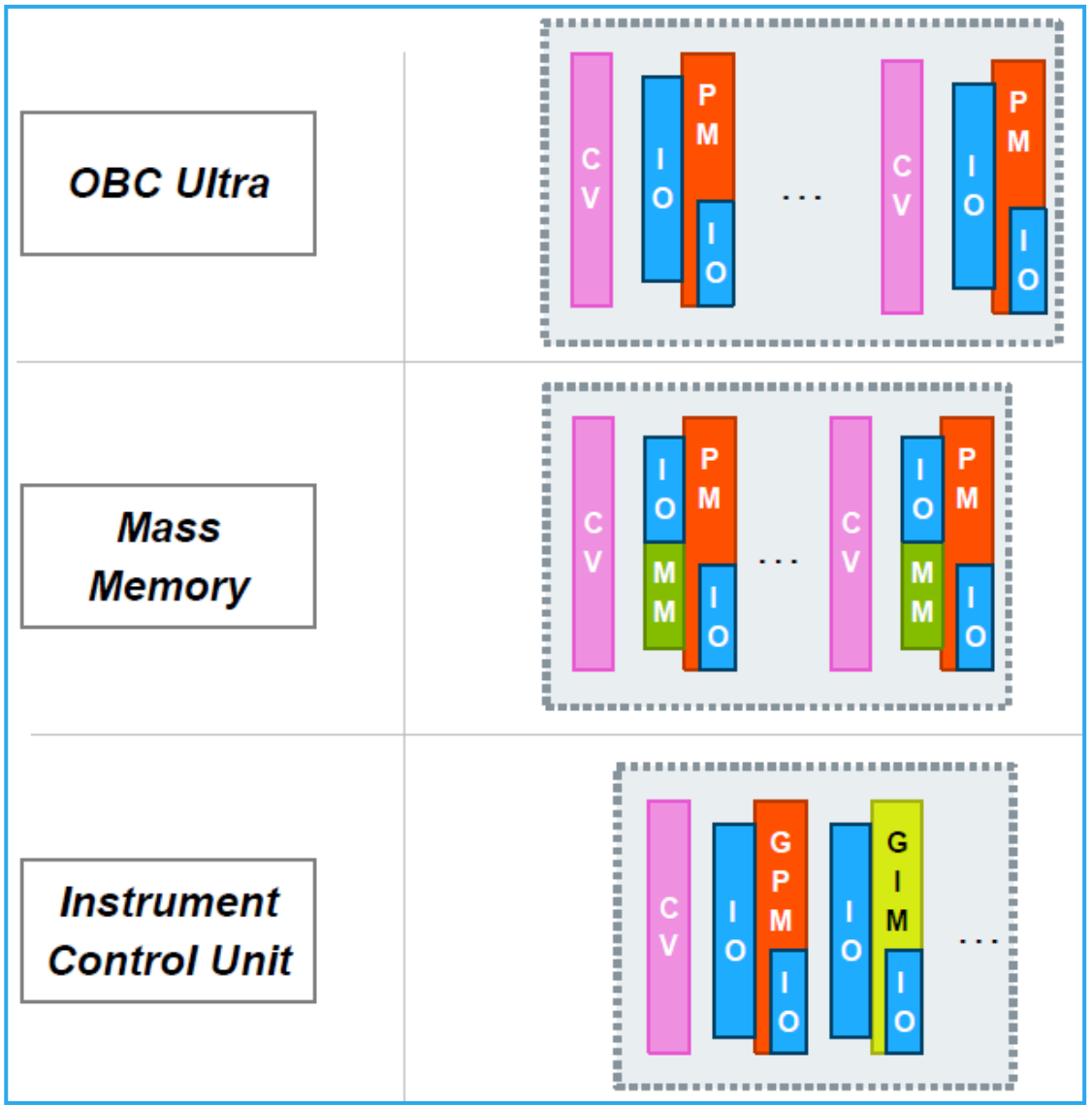
Equipment modular architecture

- Modular architecture concept:
  - Generic boards
  - Custom mezzanines
  - Adaptable number of boards

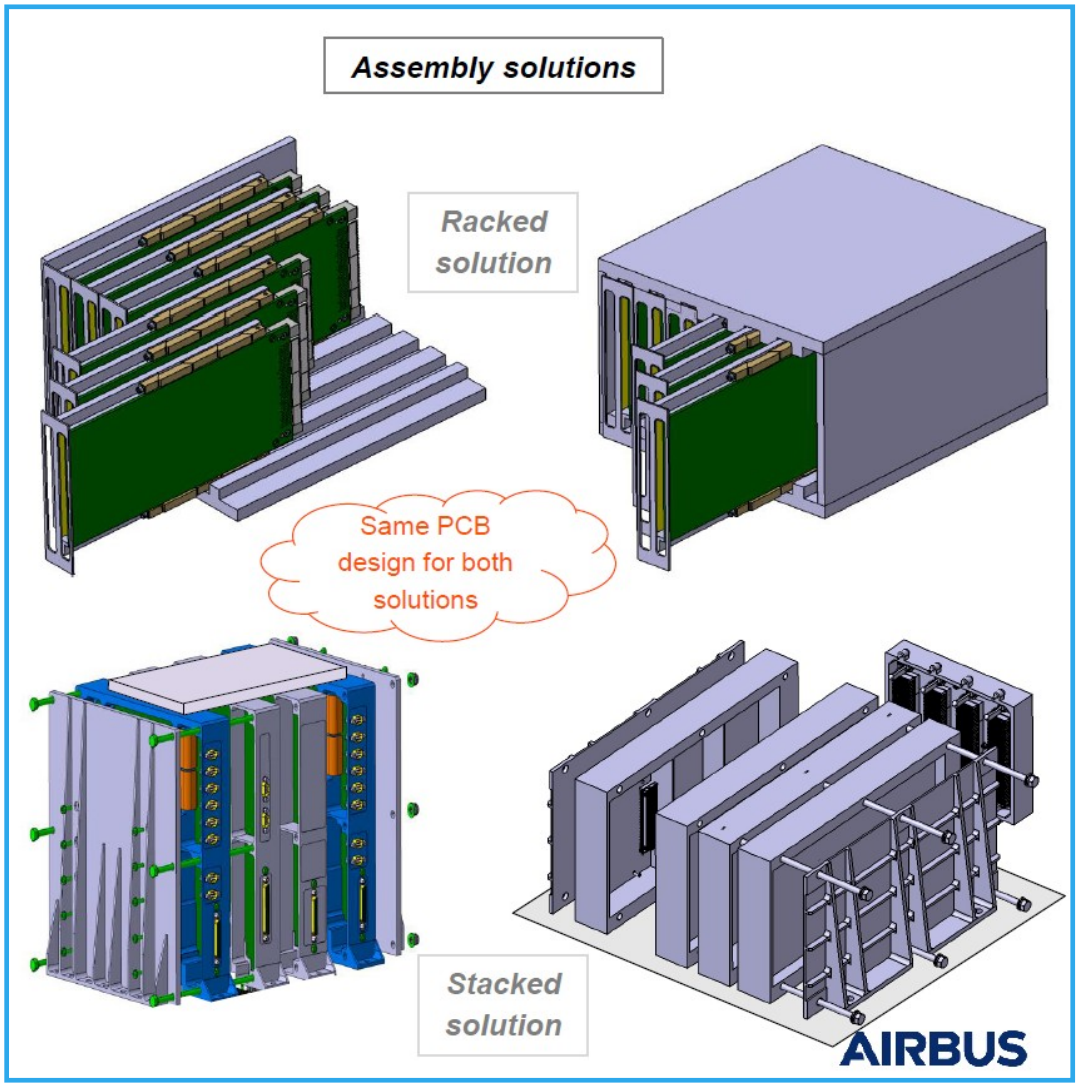
- Customized to the mission
  - OBC features
  - DHS functionalities distribution



Equipment modular assembly

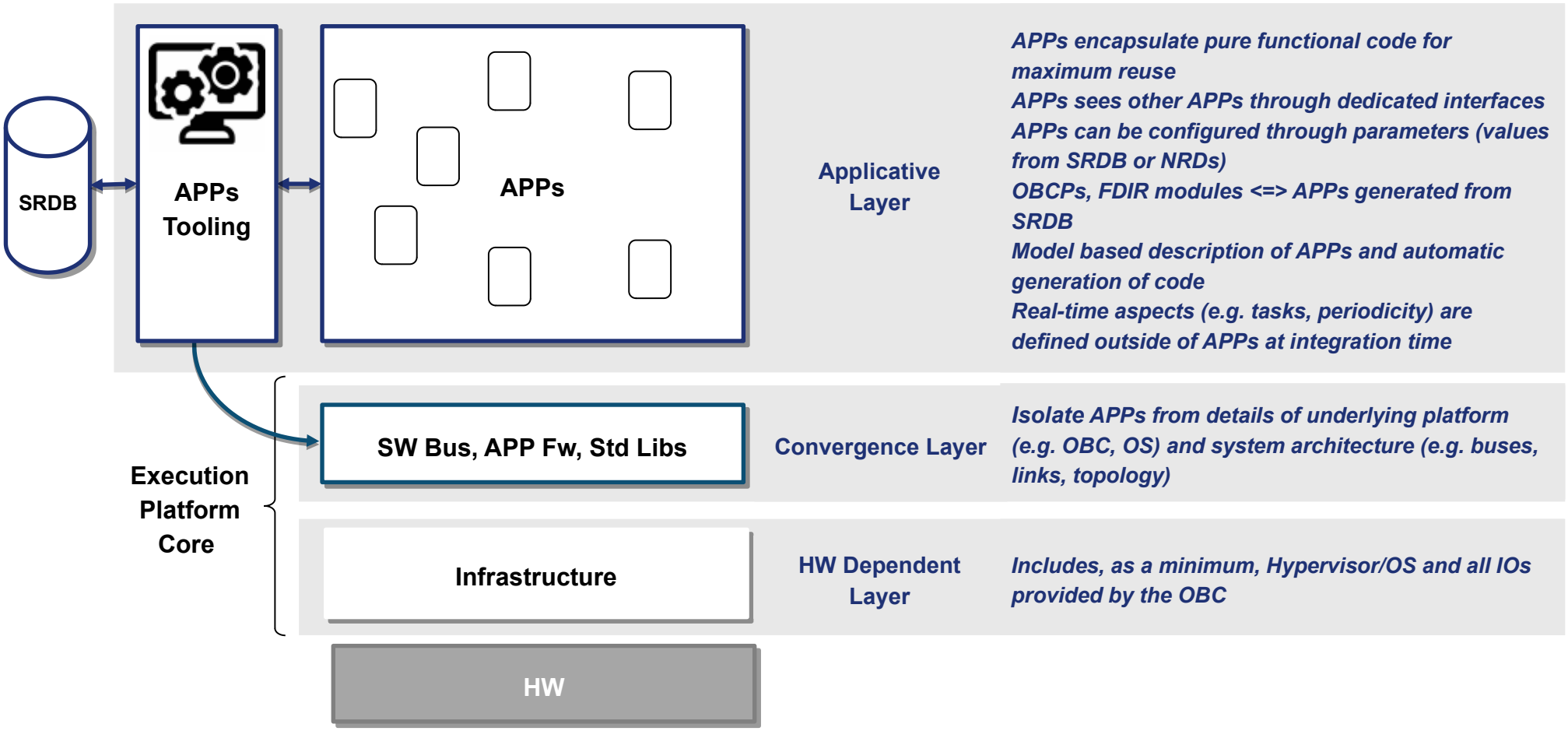
- Two assembly solutions :
  - Racked
  - Stacked

Up to what extent shoud we fly the standard?
Are the physical constraints worth the gains?



On-Board SW Architecture

Target Architecture



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Key trade-offs – FATI_2

- FATI1 (Futures Architectures Très Intégrées) study, under CNES contract, has highlighted some structuring topics for the OBC architecture
  - Where should the Reconfiguration Unit be implemented , basically inside or outside NG-Ultra ? considering that NG-Ultra FPGA is RAM based
  - How to design efficient Essential TM and Essential TC functions in the scope of an integrated architecture ?
- FATI2, as a follow-up to FATI1, aims to answer these points.

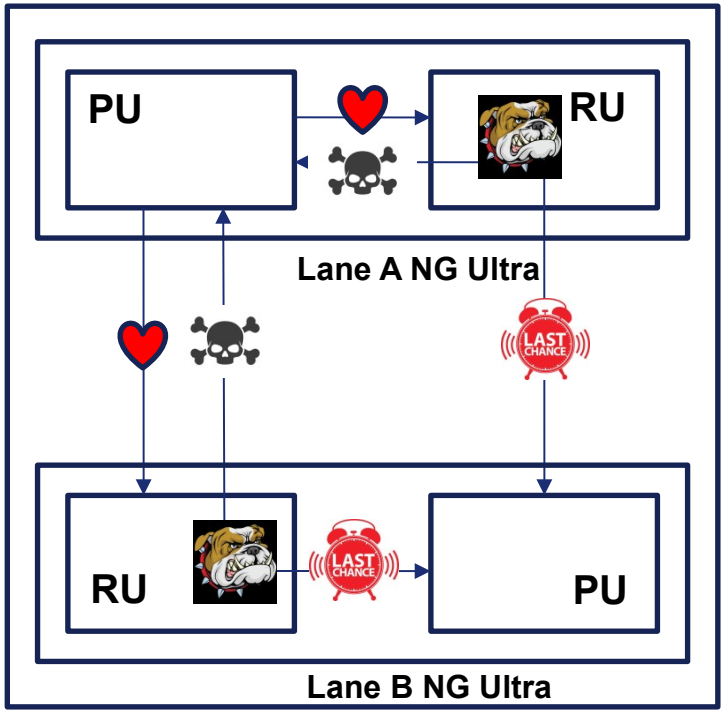
Reconfiguration Unit for Oscar-Ultra

- Same architecture as the Airbus SCOC3 based OSCAR family
  - using One PU (Processing Unit) and one RU (reconfiguration Unit) in same NG Ultra
  - One PU active, one PU 'frozen', two hot redundant RU

- Overall approach
  - No PU failure shall be missed
  - False alarms are acceptable given a low probability

- Specific points related to NG Ultra (TBC)
  - Good SEU behavior of the fabric
  - Good integrity of the configuration (CMIC)

OSCAR Ultra : Reconfiguration Baseline



Oscar Ultra

Heart Beat signal (WD reset)

Inhibit signal

Start signal

Per design:
-One single processor running
-RU in hot redundant configuration

Could lead to an erroneous reconfiguration if one RU is faulty.
-Triplicate design (RU internal)
-Insure FPGA configuration remains unaltered.
-Scrubbing (CMIC)
-Technology 28nm quite unsensitive

OBC monitoring and reconfiguration principle
Lane A active (symmetrical for lane B)

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Essential TC

- Direct TC shall allow receiving back the telemetry due to:
  - Failure of PM
  - Failure of TRSP
  - Failure of TFG

- TC necessary:
  - Reset PMA/PMB
  - Switch off/on PMA/PMB
  - Select PMA/PMB master
  - Select software image
  - Change TM coupler
  - Switch off/on TRSP A/B
  - Disable/enable RU (for avoiding loop configurations)

- As per Generic OIRD, Direct TC shall allow recovering control of the spacecraft without software:

  If no valid software is available that requirement asks for the capability to reload some software on board without using the CPU(s)…

  Strictly speaking, it means using a pure hardware automaton…

Essential TM

- The direct telemetry shall allow to regain observability of the spacecraft
- Missing TM packets originate in failure of the Processor Module or of the TFG
- Primary need is to check the acceptance and execution of TC to PM or TFG
  - TC decoder status
    - Authentication active/inactive
    - CLCW (included in each frame)
    - Frame acceptance report
    - CPDU status report
  - PM configuration
    - On/Off
    - Master/Slave
  - TFG coupler configuration
    - Selected/Unselected
  - CSW report
    - Image selected for the boot
    - Autotest results,
    - Boot report