ADCSS

12/11/2019

BRAVE LARGE PROCESSING BOARD

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Agenda

- **Context**
- **Constraints**
- **SpaceVPX**
- **FPGA NG Large**
- **Processing Board**
- **Conclusion**

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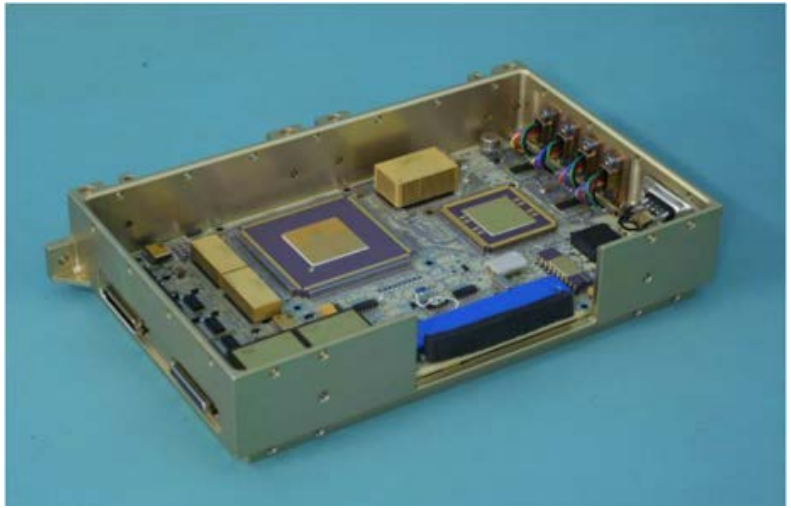
CONTEXT

- **CPU GEN : a high performance processor module, based on radiation hardened components and designed for space applications**
- **Developped with EREMS**
- **Features :**
  - Core : GR712 at 48/64/80MHz
  - FPGA : ATF (ATMEL) dedicated to mission pre-processing
  - ROM : 2Mbytes with secured Dual Boot
  - RAM : 256Mbytes
  - Interface Links :
    - 4 Spacewire at 160MHz
    - 2 redundant 1553 RT or BC
    - 2 UART
    - 16 GPIO signals
    - Debug



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CONSTRAINTS

- **The CPUGEN is designed with the classic constraints of most of projects**
- **Main Features:**
  - Components : ECSS Class 2 (Hirel QML-Q, QPL, 833B)
  - Components : standard space packages (FlatPack, Ceramic…)
  - Exportation: ITAR free
  - Radiation : Hardened design, SEFI/SEU/Latch-up protected
  - Total dose : 25krad

  ➔ No need of expensive radiation tests

  ➔ No need of expensive package & soldering qualification
- **Will flight on SVOM**

CONSTRAINTS

- **Custom Backplane & Custom Form-factor ➔ Need for standardization : Space VPX**
- **Limited FPGA (ressources and frequency) / Obsolete FPGA ➔ Select a new fpga or SoC : NG Large**
- **Obsoletes Memories ➔ Select new Memories : DDR3**

➔ **Need a substantial upgrade**

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SPACE VPX

- **Use of Space VPX Standard :**

  Approved ANSI Standard

  ANSI/VITA 78.00-2015

  SpaceVPX System

Abstract

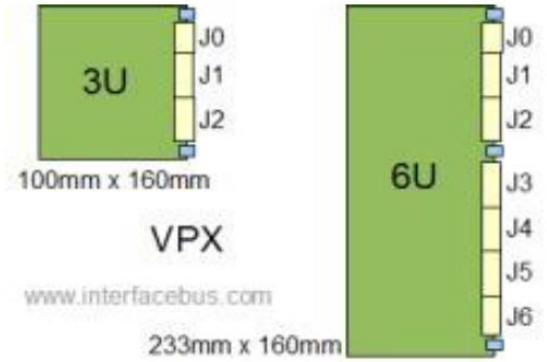
This document describes an open standard for creating high performance fault tolerant interoperable backplanes and modules to assemble electronic systems for spacecraft and other high availability applications. Such systems will support a wide variety of use cases across the aerospace community. This standard leverages the OpenVPX standards family and the commercial infrastructure that supports these standards.

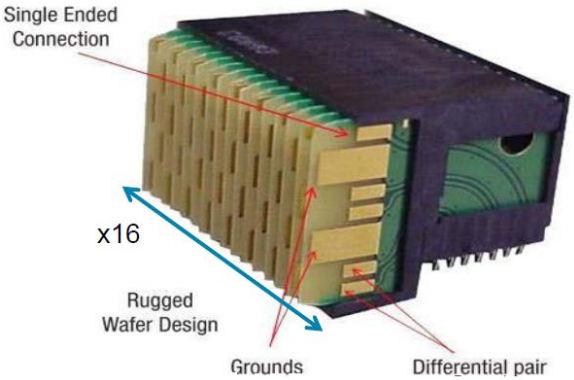
- **Form factor : 3U (100 x 160 mm) or 6U (233 x 160 mm) boards**

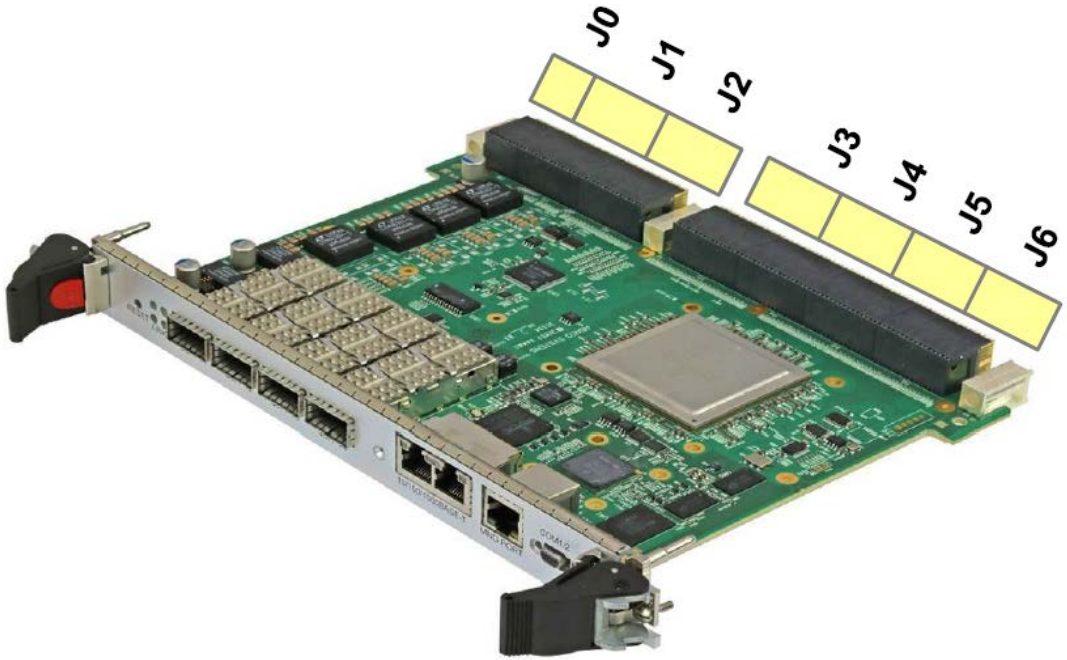
SPACE VPX Features

- **SpaceVPX created to bridge the VPX standards to the space market**
- **OpenVPX backplane standard use as the base for the SpaceVPX standardization**
- **SpaceVPX enhances the OpenVPX standard by adding spacecraft interfaces and balances fault tolerance with features required by space applications**
  - Single-point failure tolerance,
  - Spacecraft interfaces,
  - Redundancy management
- **SpaceVPX Backplane :**
  - Ethernet (for ground test)
  - Serial RapidIO (SRIO) (use of SpaceFibre)
  - Spacewire
  - Differential Pairs & Single Ended Signals
  - Power

VPX BACKPLANE CONNECTOR







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FPGA NG Large

- **NG Large (FPGA + Arm-Cortex R5) : 65nm RHBD FPGA**

ASIC Gates	**1 900 000**
Register	129 024
LUT-4	137 088
Embedded RAM	9,9Mb
Embedded DSP	384
SERDES (6,25 Gbps)	24
Packages – User I/Os LF1752 & CF1752 FF1752	 45*45 mm / 684 I/O 42,5*42,5mm / 684 I/O
Reprogrammable FPGA (SPI Configuration Memory)	
Nxmap Tools (Based on Python)	

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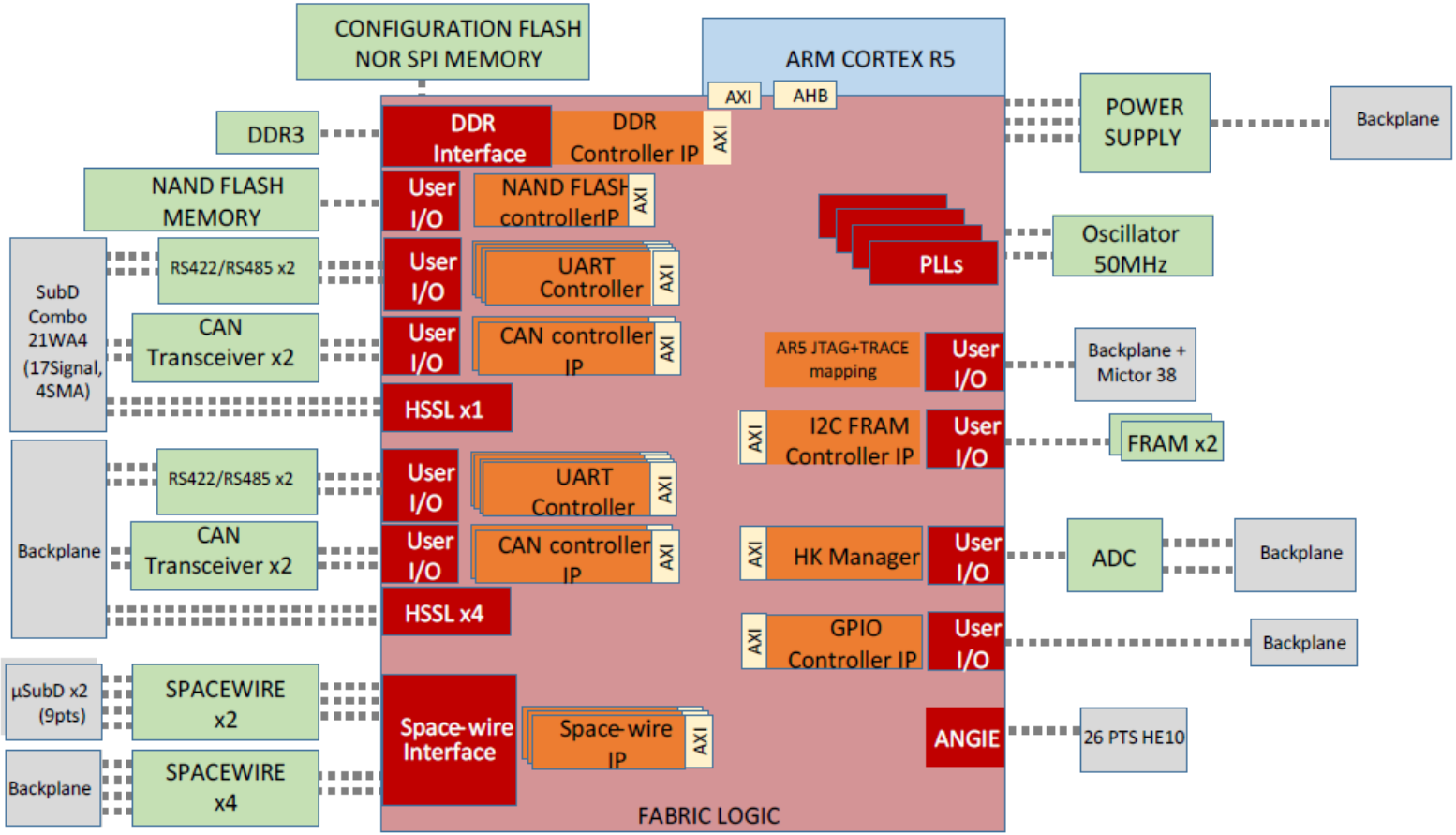
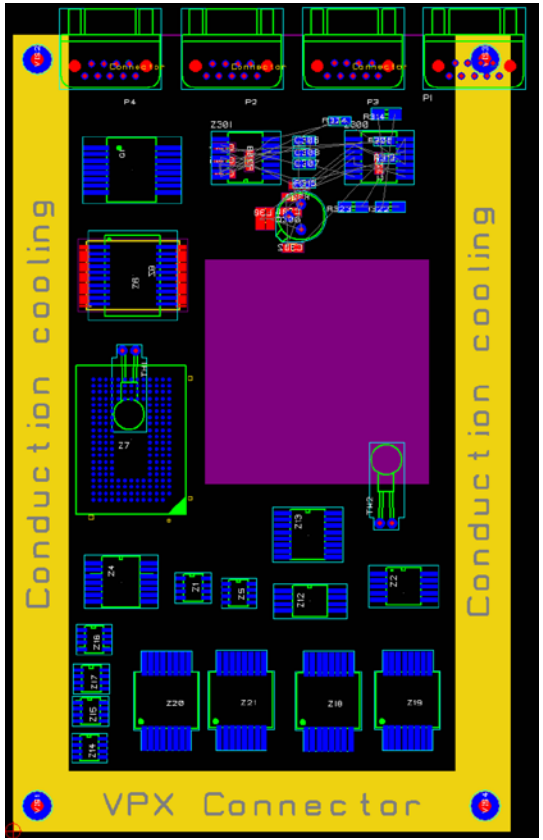
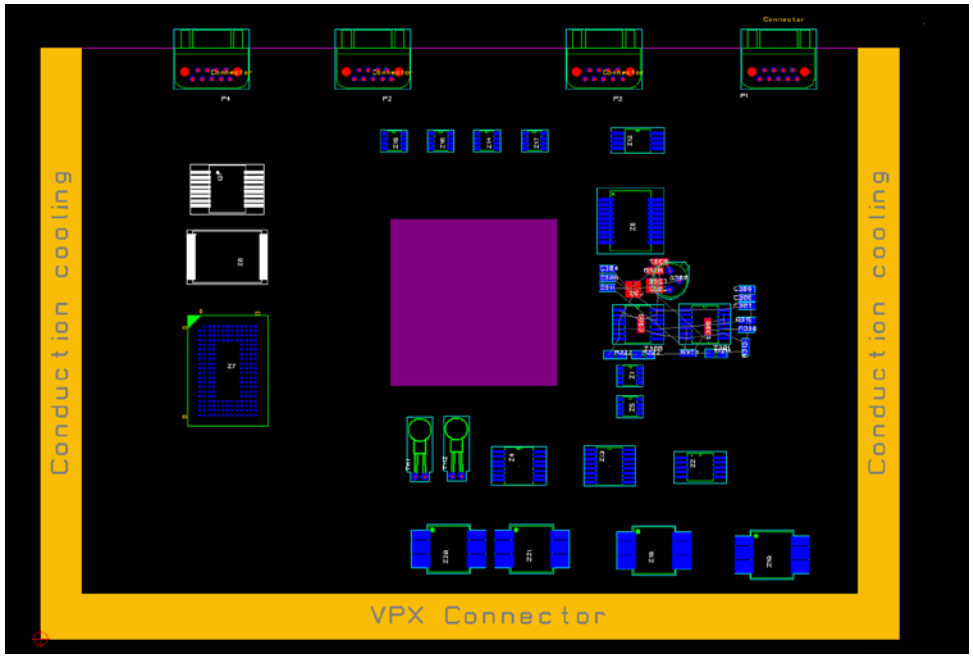
Board Architecture



Board Form Factor



3U



6U

Board Features

- **Exportation : ITAR FREE**
- **Radiation : Hardened design, SEFI/SEU/Latch-up protected**
- **SpaceVPX Form Factor (6U)**
- **FMC connector for Mezzanine Card**

- **Planning :**
  - Schematic finalized
  - Placement & Route in progress
  - Board could be available mid-2020 (engineering model)

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CONCLUSION

- **New processing board based on NG Large**
- **Standardization use for modularity approach**
- **Developpment still in progress**
  - Dvpt of FPGA IP
  - Dvpt SW of ARM Cortex-R5
  - Thermal dissipation to discuss
  - Power comsumption
  - Board qualification

Thank You