iSAFT Test Tool for deterministic on-board Ethernet Networks

(ESTEC GSTP De-Risk Activity)

ADCSS - November 2019

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Presentation Contents

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iSAFT – Interface Boards, Software, Integrated Testers/Recorders

SpaceWire

SpaceFibre

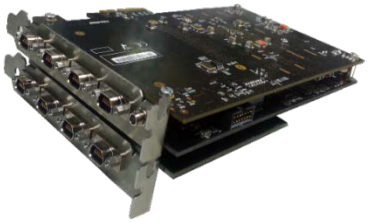
CAN

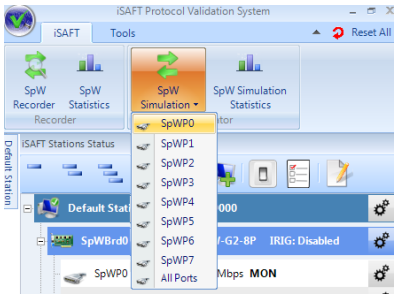
CANopen

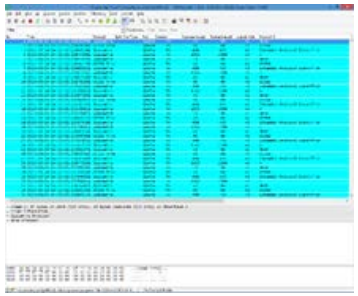
MIL-STD-1553

TTEthernet

UART, SPI, I2C, other







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Extend iSAFT with Time Triggered Ethernet interface

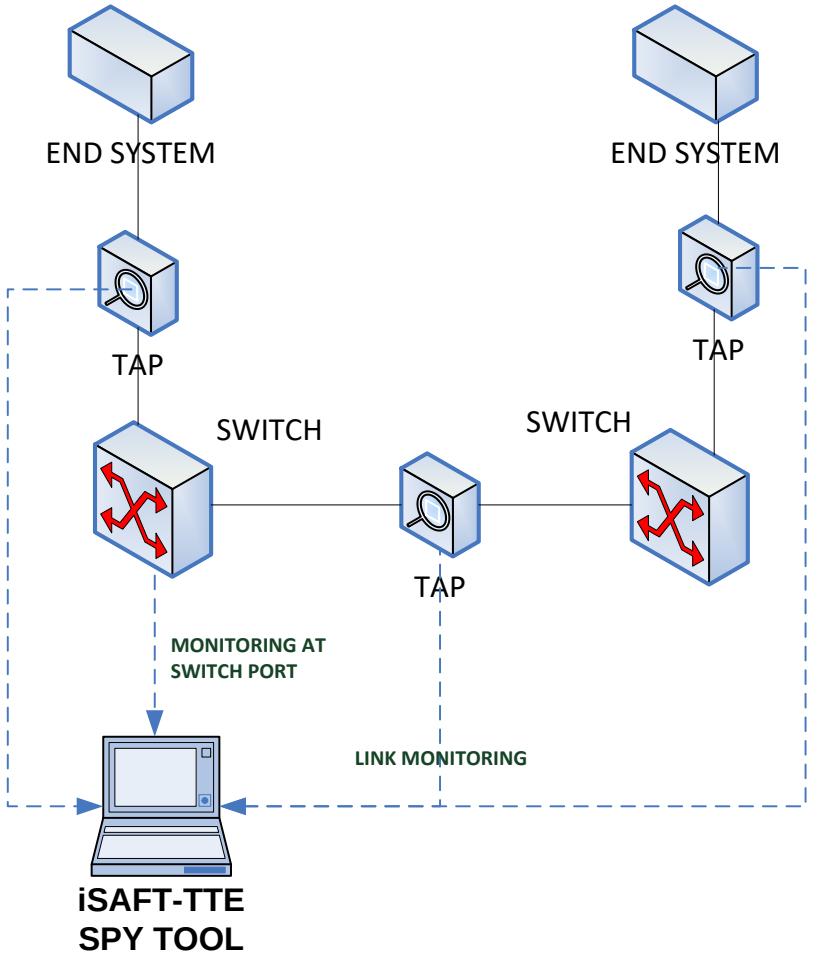
Main contractor: Teletel

Sub-contractors: Ariane Space, AIRBUS Defense & Space

- Phase 1 (project completed in 2018)
  - Task 1: Implementation of a TTEthernet VERIFICATION/SPY Tool
  - Task 2: Assessment for the implementation of a TTEthernet End System IP Core based on open TTEthernet standards
- Phase 2 (not started – on-hold):
  - Full Implementation of a TTEthernet End System IP Core
  - iSAFT PVS Tool extension: Implementation of TTEthernet ES simulation and traffic generation + fault injection tool (based on FPGA boards using the IP Core)

iSAFT TTE Verification/SPY Tool features

- TTE Network Monitoring
  - Direct physical traffic acquisition via Switch port or TAP
  - Full data recording with configurable filtering of received traffic
  - Traffic files in Wireshark format with Dissectors for all protocols
  - Traffic analysis and verification during monitoring
  - Analytical display & logging of statistics
  - Open interfaces for input configuration/output results data exchange with 3rd party tools
  - Using COTS Ethernet boards for monitoring (with accurate time-stamping)
  - Not based on existing TTEthernet HW/SW implementations



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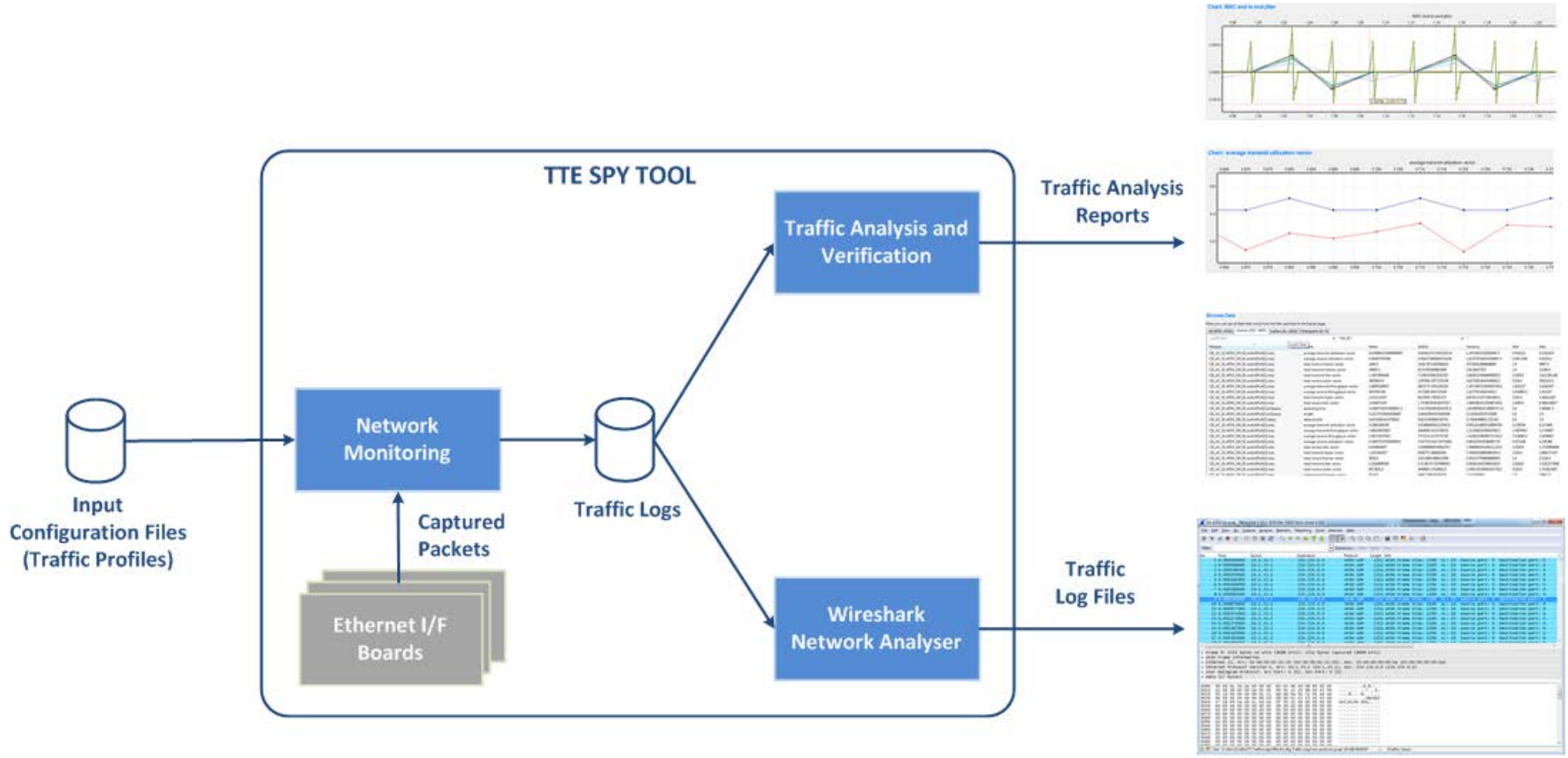
iSAFT TTE Verification/SPY Tool features



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- But in the meantime …..
- A new promising player has appeared in the space domain -> TSN
- Before proceeding to develop a TTE IP Core and the subsequent test tool, TELETEL wants to secure further developments.

- Decision to execute a Phase-1 project (de-risk)
  - *analyse, evaluate and compare TTE with TSN, mainly for network verification*
  - *identification of possibly common TTE/TSN building blocks,*
  - *prototyping in VHDL/FPGA technology and demonstration in a typical TTE/TSN testbed.*
  - *Use the existing iSAFT TTE Verification/SPY tool to verify the developments*

Participants and Main Roles

- **TELETEL S.A. (Greece) - prime-contractor**
  - Analysis of TTE/TSN commonalities
  - Development of VHDL IP blocks
  - Setup of a TSN testbed
  - Verification and demonstration
  - Definition of the roadmap for a fully fledged TTE/TSN Test Tool

- **AIRBUS Defense & Space (Toulouse) - subcontractor**
  - Requirements for the use of TSN in future missions
  - Identification of mandatory & optional TSN standards
  - Roadmap for the Bring system level requirements from existing and future missions, assuring the wider and more complete requirements definition, consolidation and review.

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PHASE-1 (De-Risk activity) Main Work Areas (1/2)

- Analyze the TSN / IEEE related standards and define the required blocks for a TSN capable controller
- Identify possibly common building blocks between TTE and TSN (e.g. scheduler, etc.)
- Requirements definition for TSN Test Tool supporting End System simulation, traffic generation & fault injection functionalities
- Provide architectural definition of required algorithms and designs for the HW implementation of a TSN controller
- Analyse impact on HW resources and performances for the different design choices / configurations of the TSN controller

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PHASE-1 (De-Risk activity) Main Work Areas (2/2)

- Selection of the core blocks for a TSN controller and HDL implementation, integration in a PCIe FPGA board
- Analyse requirements imposed at the Ethernet switches to support TSN networks and identify candidate COTS components for the setup of a TSN testbed
- Demonstration of the TSN PCIe FPGA board in a TSN testbed
- Definition of the roadmap for deriving a generic TTE/TSN Ethernet test and validation tool
- Production of a detailed Proposal for a subsequent Phase 2

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Project Timeline

- **Project Kick-Off**
  - Date: 2nd September 2019
- **Requirements analysis and identification of common building blocks between TTE/TSN**
  - Milestone: SRR
  - Date: 30th November 2019
- **Prototyping of TSN controller core blocks in a PCIe FPGA board**
  - Milestone: PDR/CDR
  - Date: 31st January 2019 / 31st March 2020
- **Definition of use cases and roadmap for deriving a generic TTE/TSN test and validation tool**
  - Milestone: FAR
  - Date: 31st May 2020

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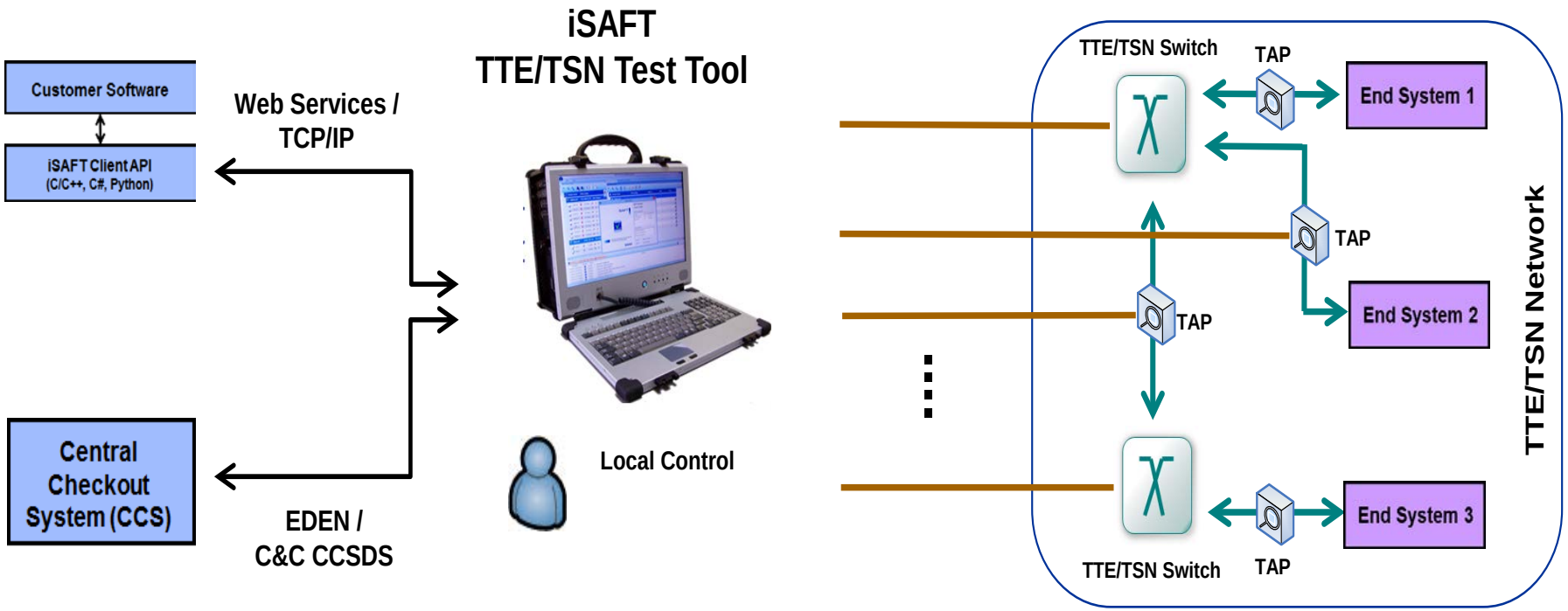
Subsequent Phase 2 activity – start second semester 2020



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