CENTRALIZED AND MODULAR ARCHITECTURE

ADCSS - Wednesday, November 12th, 2019

Pierre SPIZZI, CNES

AGENDA

DARWIN

- DARWIN HISTORY AND GOALS
- AVIONIC AND ELECTRICAL ARCHITECTURE
- HYPERION
- BOMO
- DARWIN DEMONSTRATION
- CONCLUSION

AGENDA

- **DARWIN HISTORY AND GOALS**
- *AVIONIC AND ELECTRICAL ARCHITECTURE*
- *HYPERION*
- *BOMO*
- *DARWIN DEMONSTRATION*
- *CONCLUSION*

DARWIN DEFINITION

DARWIN is a CNES internal demonstrator

- “Low-cost” products
- COTS components
- “New-space”
- Modularity

It addresses 2 different goals:

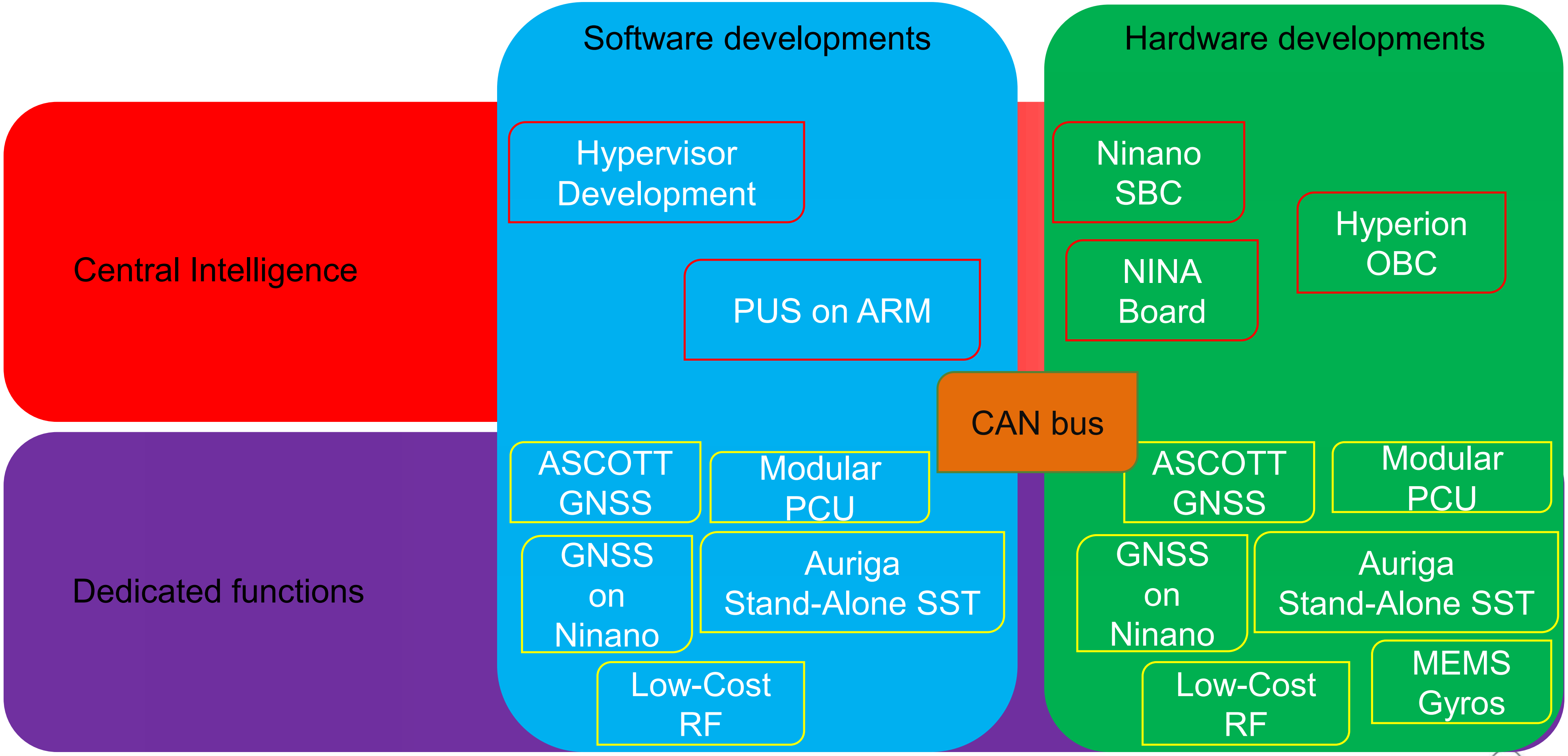
- Avionics functions integration in the OBC (uses of SoC)
- Modular and distributed electrical architecture

DARWIN ON THE ORIGIN OF SPECIES

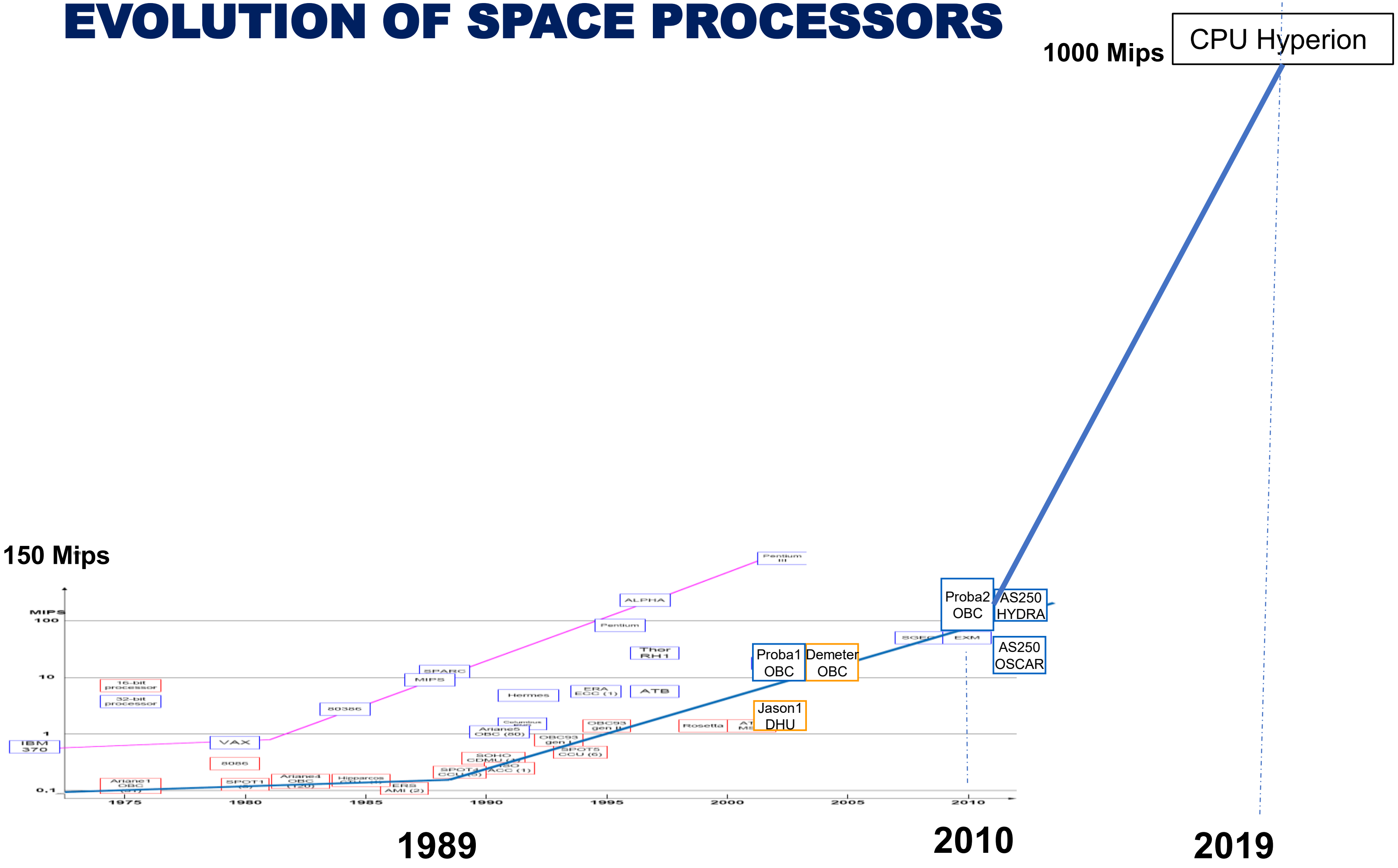
The project stemmed from 3 observations:

- A lot of R&D projects carried out separately in many fields of avionics but never brought together
- New SOCs now available are much more capable than traditional space hardware
- Cost (+ Mass & Power & Volume) are increasingly important in space industry

DARWIN - R&D BUILDING BLOCKS



EVOLUTION OF SPACE PROCESSORS



Zynq7xxx

GR712 ~150MIPS

AT697 ~100MIPS

SCOC3 ~60MIPS

ERC32 ~10MIPS

LENA ~4MIPS

T805 ~2MIPS

MA31750 ~2MIPS

DARWIN - AROUND OBC CENTRALIZATION

3Kg
15-20W
176*170*116mm

GNSS

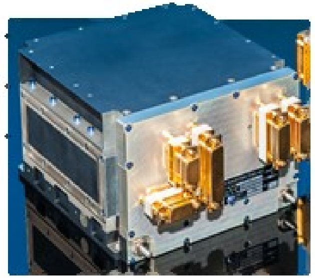
1Kg
3W
120*160*40mm

TMTC

3Kg
7W
220*120*143mm

OBC

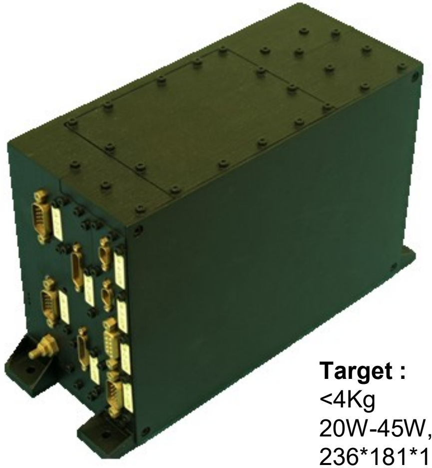
Mémoire de masse



400g
3W
150*170mm

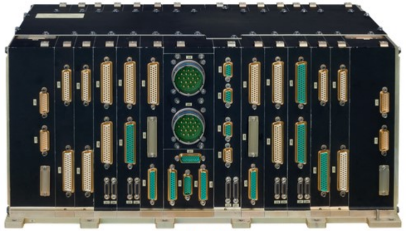
Star tracker - processing

HYPERION



Target :
<4Kg
20W-45W, Typ 22W
236*181*122mm (redundant version)

DARWIN - MODULAR AND DISTRIBUTED ELECTRICAL ARCHITECTURE

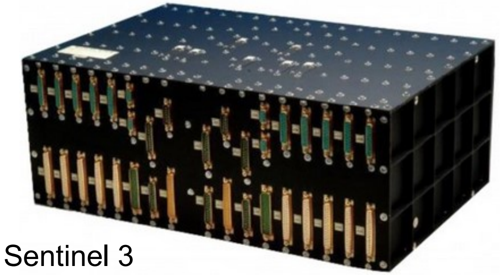


Crisa PCDU

Sentinel 2-A

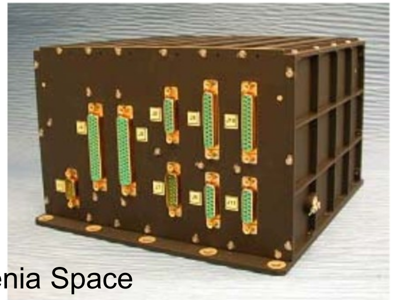
PCDU are usually massive units :

- accommodation inside platforms is difficult
- specific hardware required for thermal management (heat pipe, heat spreader…)
- High concentration of connectors
  - harness routing on connectors faces is



Sentinel 3

- low modularity
- significant recurring prices



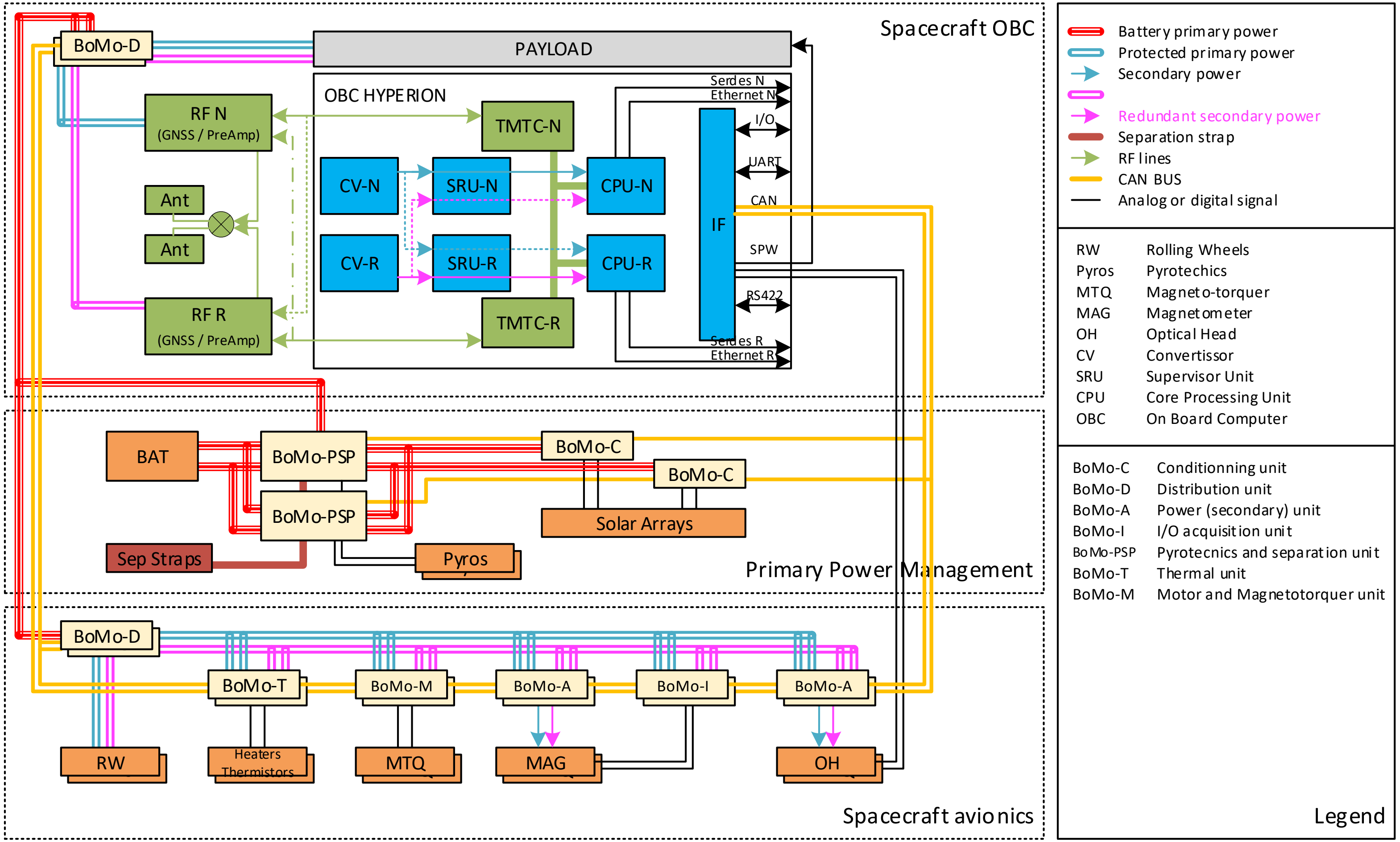
- **A solution is to implement a modular and distributed architecture**

Thales Alenia Space
Myriade PCDU

AGENDA

- *DARWIN HISTORY AND GOALS*
- **AVIONIC AND ELECTRICAL ARCHITECTURE**
- *HYPERION*
- *BOMO*
- *DARWIN DEMONSTRATION*
- *CONCLUSION*

AVIONIC AND ELECTRICAL ARCHITECTURE

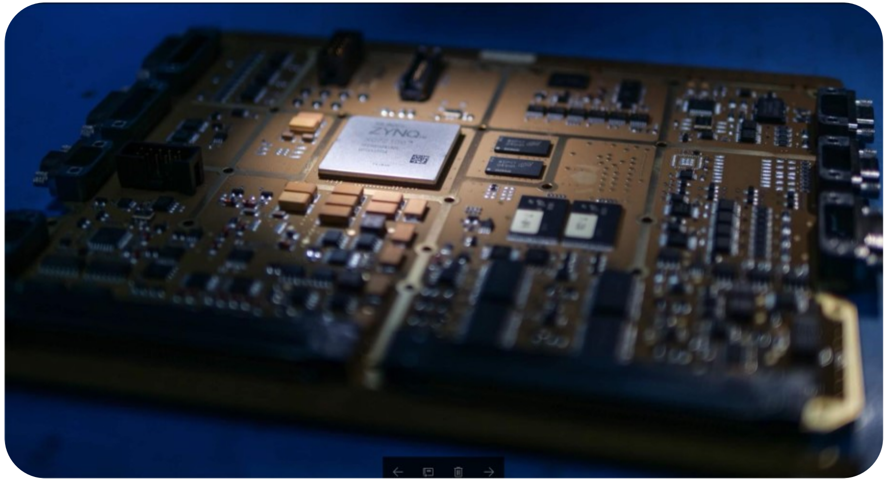


AGENDA

- *DARWIN HISTORY AND GOALS*
- *AVIONIC AND ELECTRICAL ARCHITECTURE*
- **HYPERION**
- *BOMO*
- *DARWIN DEMONSTRATION*
- *CONCLUSION*

HYPERION

- COTS based architecture
- Automotive grade components
- Latchup free or localy protected
- Cumulated dose up to 5kRads (goal up to 10kRads)



- Developped by STEEL ELECTRONIQUE Company

HYPERION

CV:

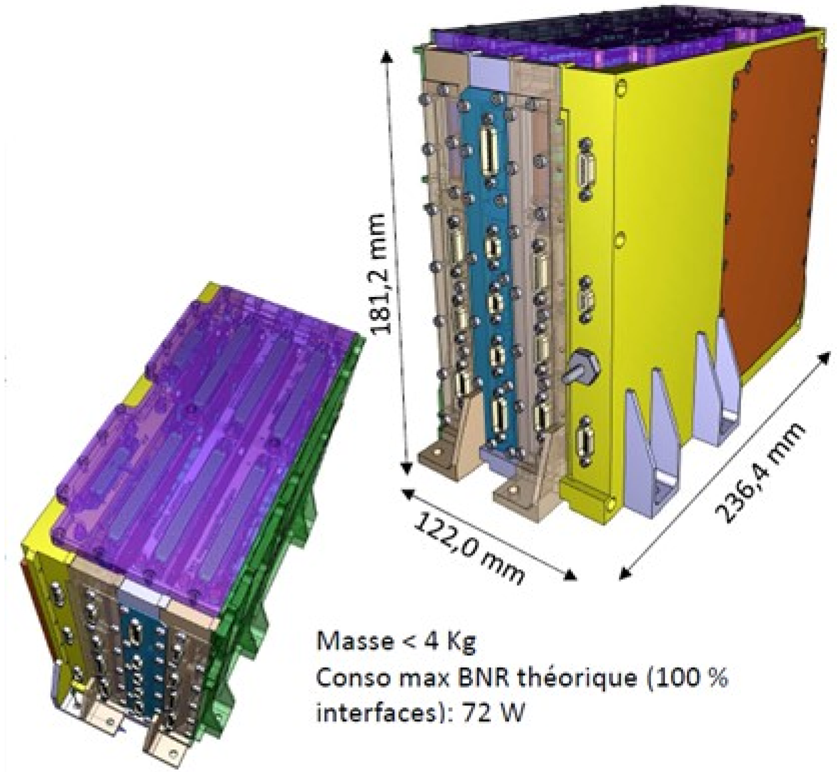
- [22,42]V Primary power
- PmaxRéel = 35W et Ptyp=20W
- Electrical architecture of converter in cold redundancy
- Autonomous switching as last « watchdog level »

CPU/COMUX:

- Zynq based architecture in cold redundancy
- ATMEGA based supervisor unit
- Shared Context memory between redundancies
- Many communications interfaces available

RF BOARD (Option under advisement):

- GNSS and TMTC handling (developped by SYRLINKS Company)



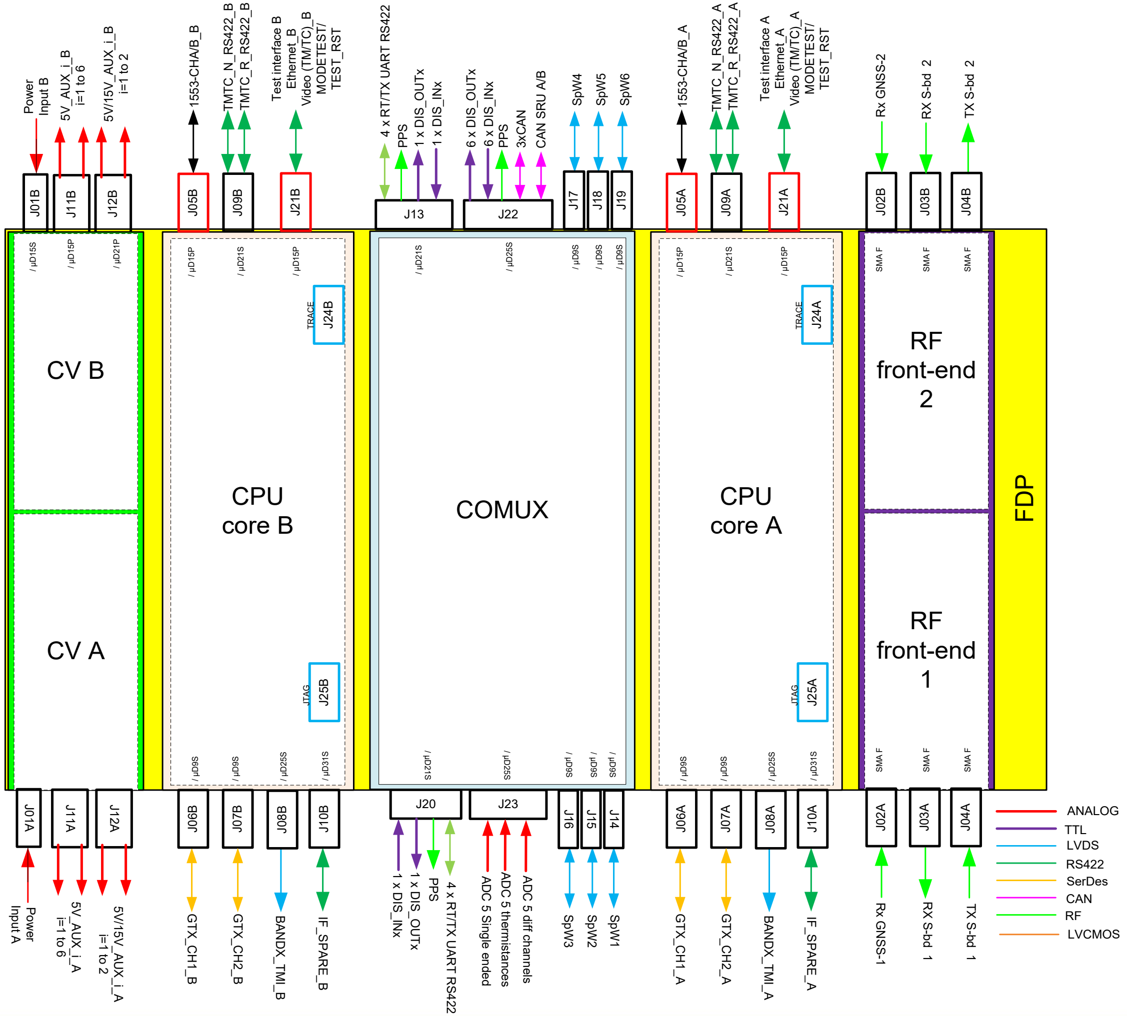
HYPERION

CPU A ou B:
1 x 1553 A/B
1 x TMTC RS422 N/R
1 x IF TEST (Vidéo, Ethernet)
7 x SPARE RS422 Full-D
1 x TMI-X (LVDS)
2 x GTX Lane
1 x Trace
1 x JTAG

COMUX :
6 x SpW
3 x Bus CAN CPU
2 x Bus CAN SRU
15 x ANALOG IN
8 x UART RS422 Full-D
3 x PPS RS422
8 x BLD IN
8 x BLD OUT

CV A ou B:
1 x BNR 28 V
5 x sorties 5V (7.5 W)
2 x sorties 5V ou 15V (7.5 W)

RF:
2 x S-Band
2 x GNSS



HYPERION

Advantages:

- Functions centralization
- Reduction of accommodation constrains and harness routing
- Reduction of mass
- Low cost solutions for new space projects (goal /2 with OBC Myriade)
- Redundancy strategy handled
- Big number of interfaces

Drawbacks:

- Reliability as a best effort

Actual status : EM under test / EQM at end of 2020

AGENDA

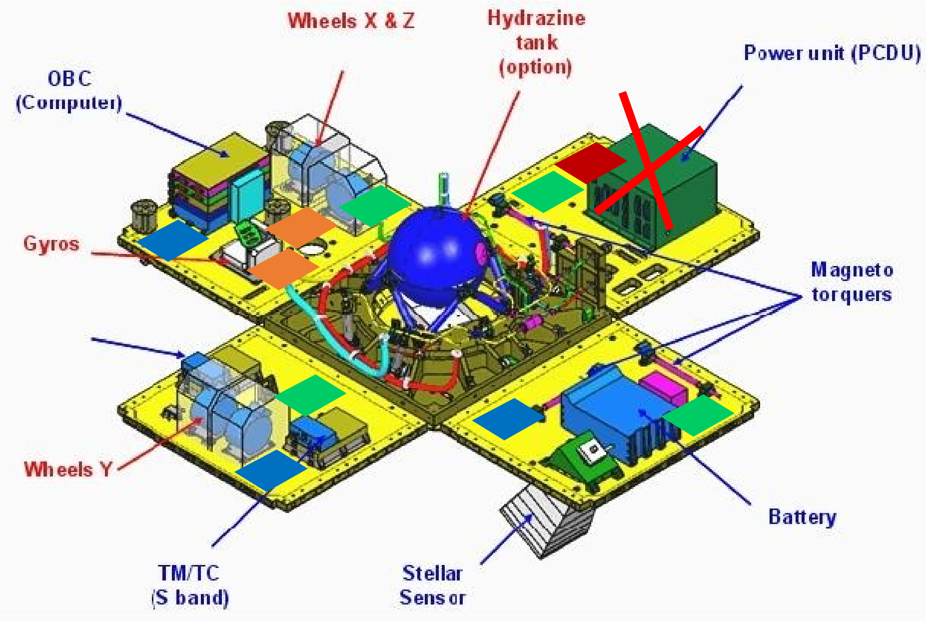
- *DARWIN HISTORY AND GOALS*
- *AVIONIC AND ELECTRICAL ARCHITECTURE*
- *HYPERION*
- **BOMO**
- *DARWIN DEMONSTRATION*
- *CONCLUSION*

BOMO REPRESENTATION

How to use Modules? Example of Myriade Platform

Before

After



PYRO / SEP PASSIVATION

POWER COND

DISTRI

HEATER CONTROL and ACQ

Myriade Platform - CNES

BOMO

GENERAL:

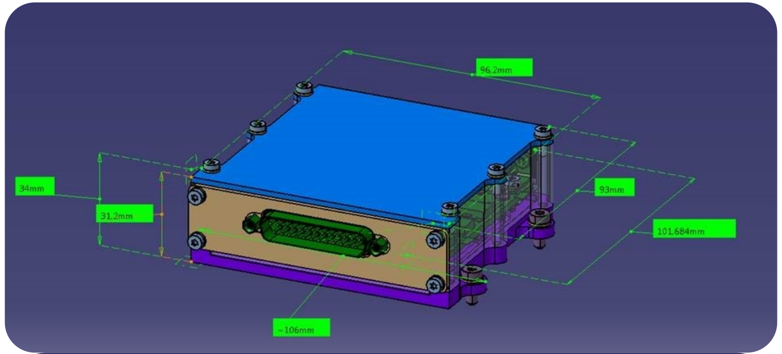
- COTS based architecture
- Standard mechanic
- No failure propagation to other terminals

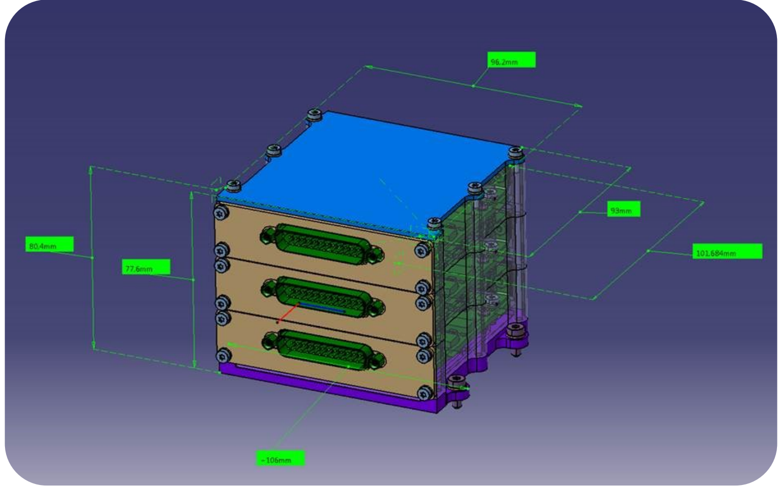
CORE:

- Primary power between 22V and 38V
- PIC18LF4685 Core processor
- CAN BUS interface
- FUSE protected

SPECIFIC:

- Handling separated functions of former PCDU





- Developped by EREMS Company

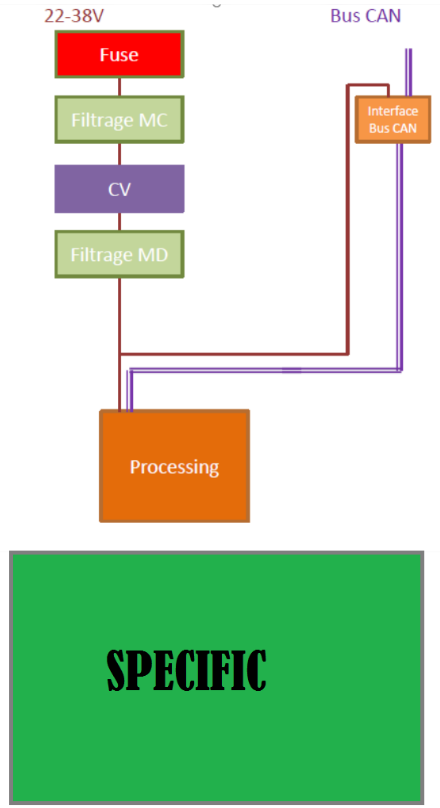
BOMO

<u>3 under developpement</u>

- BoMo-C: Solar array DET Conditioning boxes (handling 7 DET of 2,5A each)
- BoMo-D: Power distribution boxes to deliver primary power to secondary through current limiter circuitry (goal : 10 lines)
- BoMo-PSP: Handling 4 pyrotechnic device (SA), as well as separation module from launcher and passivation system at S/C end of life

<u>Others to be developed</u>

- BoMo-IO : Acquisition and drive of up to 12 I/O (TBC)
- BoMo-T: Thermal control boxes allowing the drive of 4 heaters and the acquisition of up to 8 thermistors (TBC)
- BoMo-A: Power conversion boxes allowing to deliver secondary regulated voltages (+/-15V, +/-12V, 5V) (TBC)
- BoMo-P: Pyrotechnic boxes handling up to 10 pyrotechnic system (TBC)
- BoMo-M: MTQ or Motor drive boxes handling up to 3 inductive subsystem (MTQ or Motor phases)



BOMO

Quality:

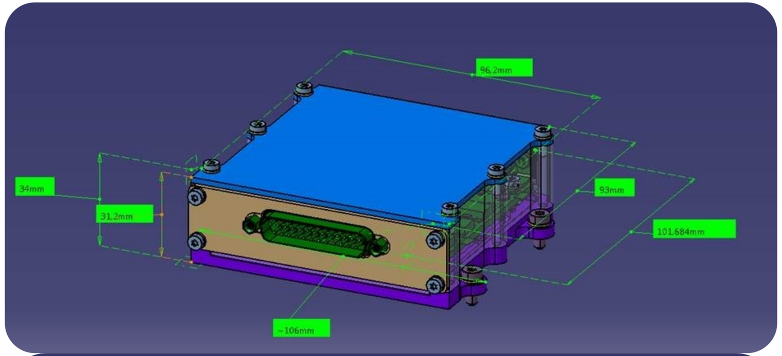
- Automotive grade

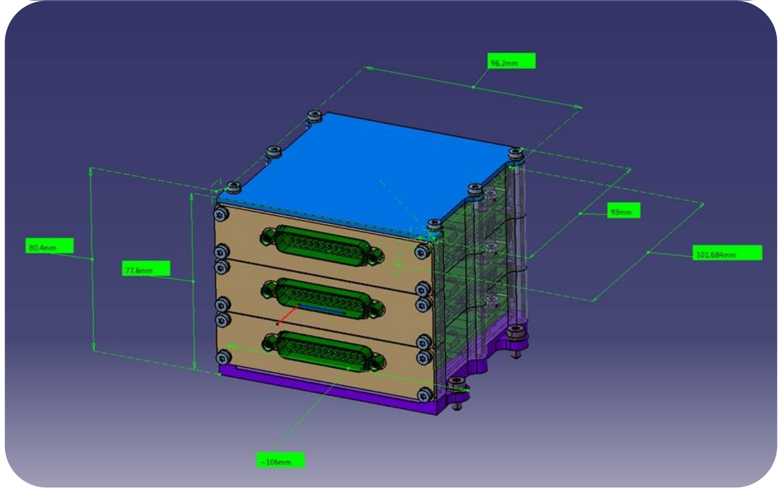
Radiations & Effects:

- Latchup free or localy protected
- Cumulated dose up to 10kRads

Planning:

- 3 first BOMO (C, D, PSP) expected at end of 2019





BOMO

Advantages:

- Flexibility of platforms designs
- Reduction of accommodation constrains and harness routing
- Reduction of mass
- Low cost solutions for new space projects (goal /2 with PCDU Myriade)
- Modules could be used in simplex chain or in redundant architecture pending SPF analysis.

Drawbacks:

- Need of redundancy management at spacecraft level if SPF are forbidden in the project

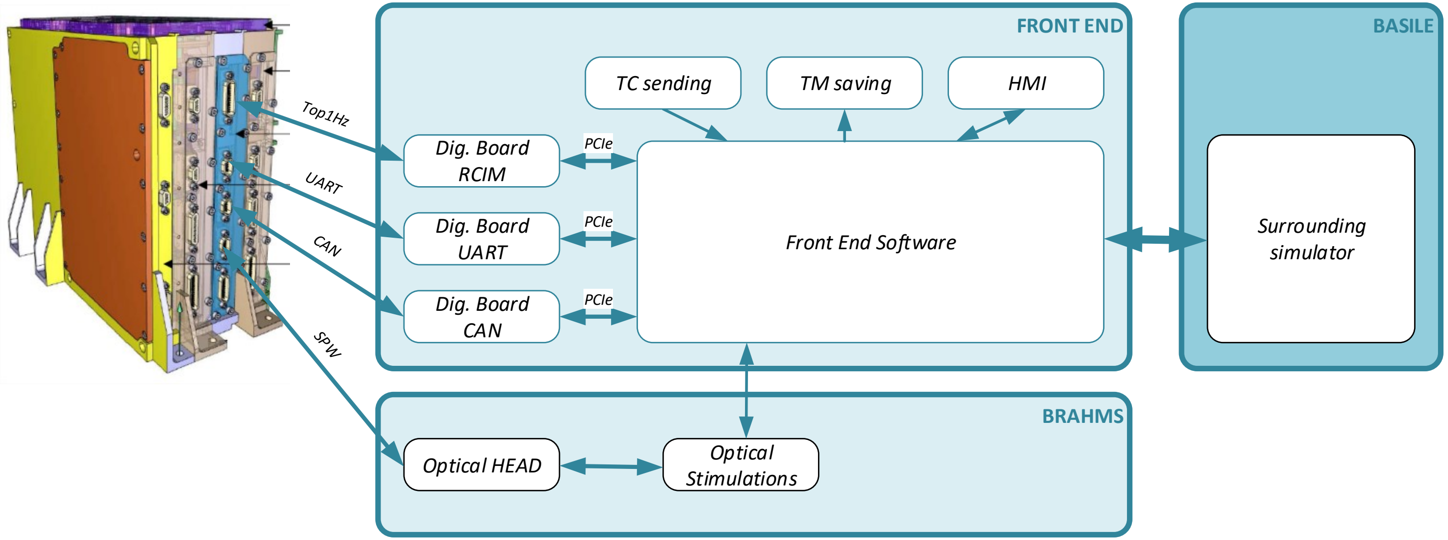
AGENDA

DARWIN

- *DARWIN HISTORY AND GOALS*
- *AVIONIC AND ELECTRICAL ARCHITECTURE*
- *HYPERION*
- *BOMO*
- **DARWIN DEMONSTRATION**
- *CONCLUSION*

DARWIN DEMONSTRATION

- AOCS closed loop
  - Wheels, MTB, SST
- Myriade based model MNO
- Representative Flight SW
- Representative Flight HW

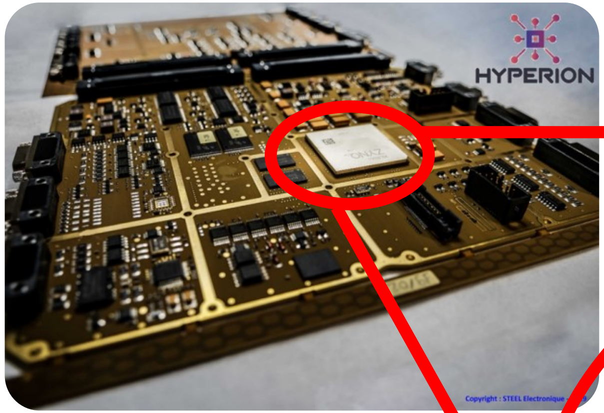


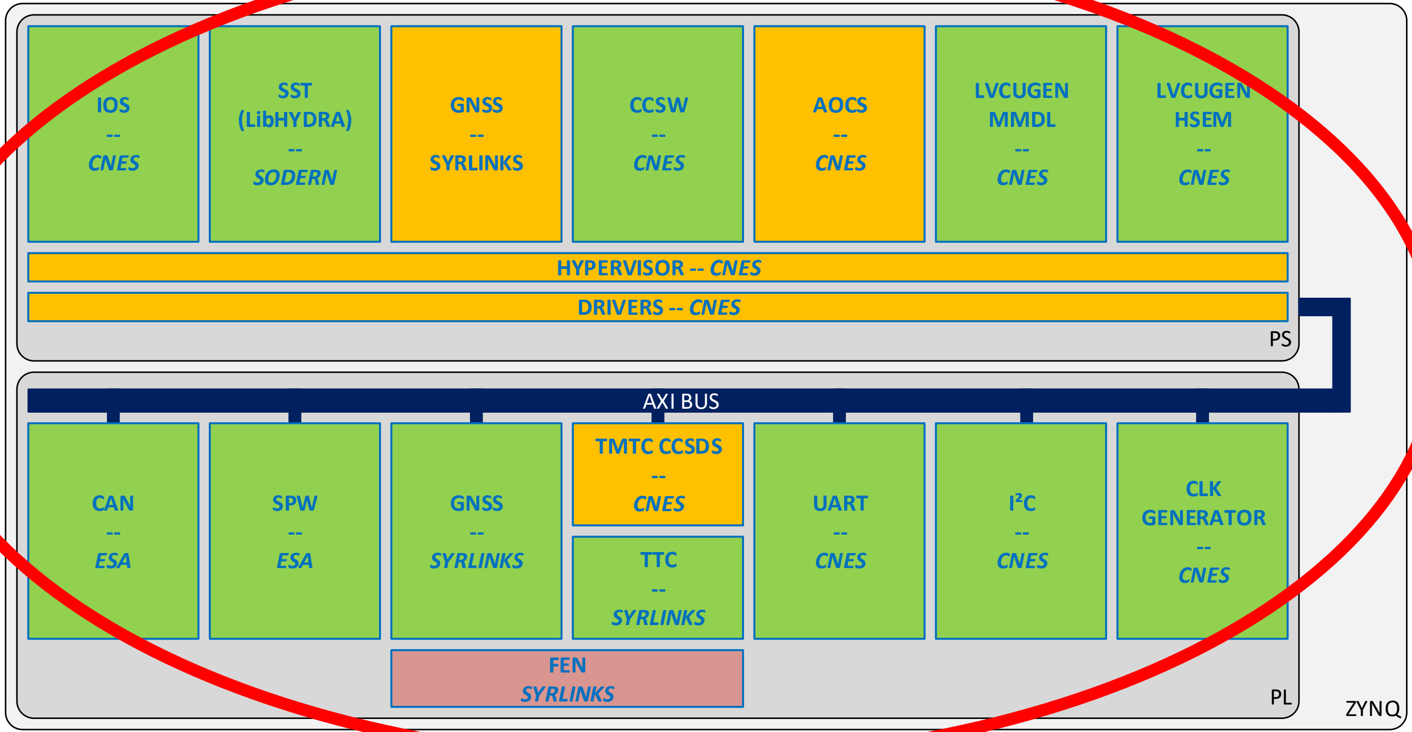
<u>Results:</u>

- Comparison of performances between classical OBC and DARWIN OBC
- Processor performances and ressources
- PL ressources
- Consumption and thermal dissipation

- Development Model with SmallSat OBC « Ninano » from STEEL ELECTRONIQUE Company
  - Smaller Chip → Smaller design

DARWIN SoC ARCHITECTURE





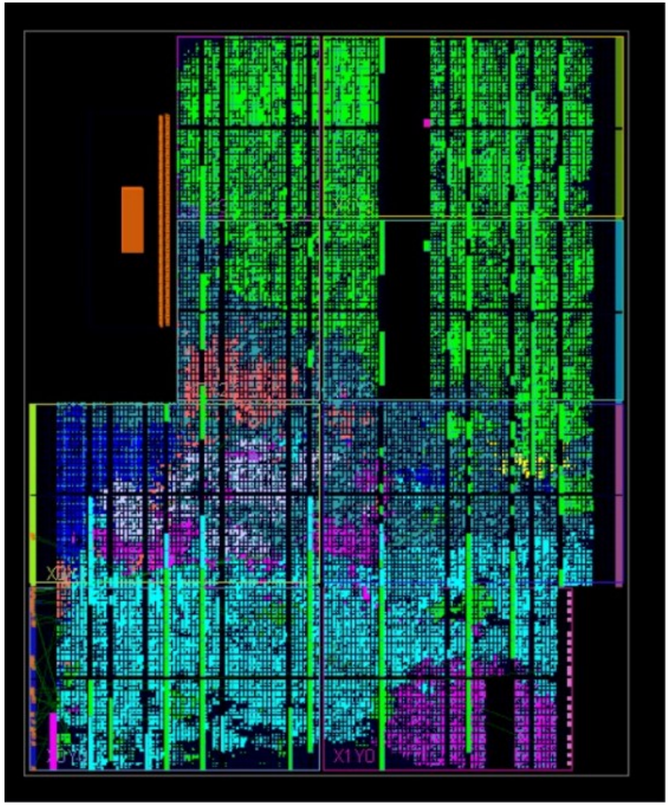
DARWIN OBC RESSOURCES – PL

- Developement Version
  - ZYNQ 7030 (NINANO Board)

- NINANO design
  - 1 CAN
  - 1 UART
  - 1 SPW
  - 1 I²C
  - 1 GNSS
  - 1 TMTC

- HYPERION design (7100 Zynq)
  - 3 CAN
  - 8 UART
  - 5 SPW
  - 1 I²C
  - 1 GNSS
  - 2 TMTC

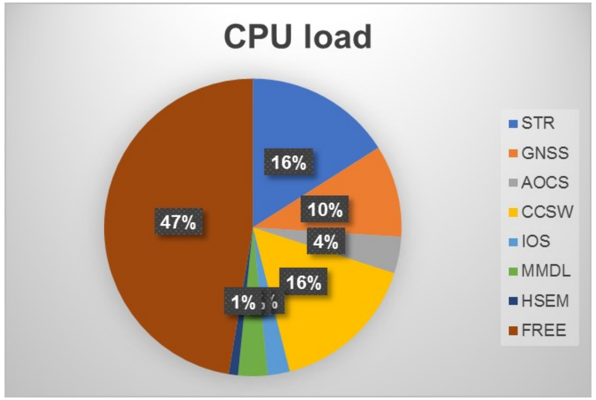
→ Estimation 50% LUT 30% FF 30% BRAM

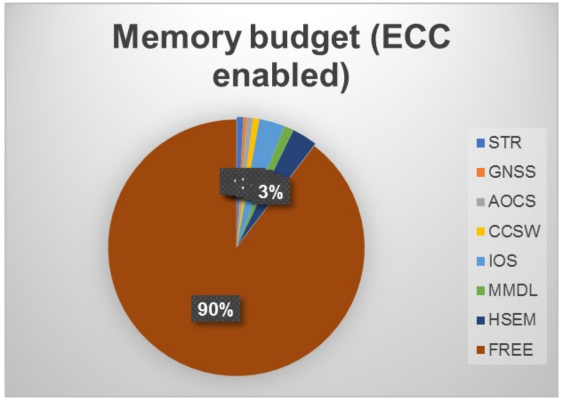


Ninano Design

DARWIN OBC RESSOURCES – PS

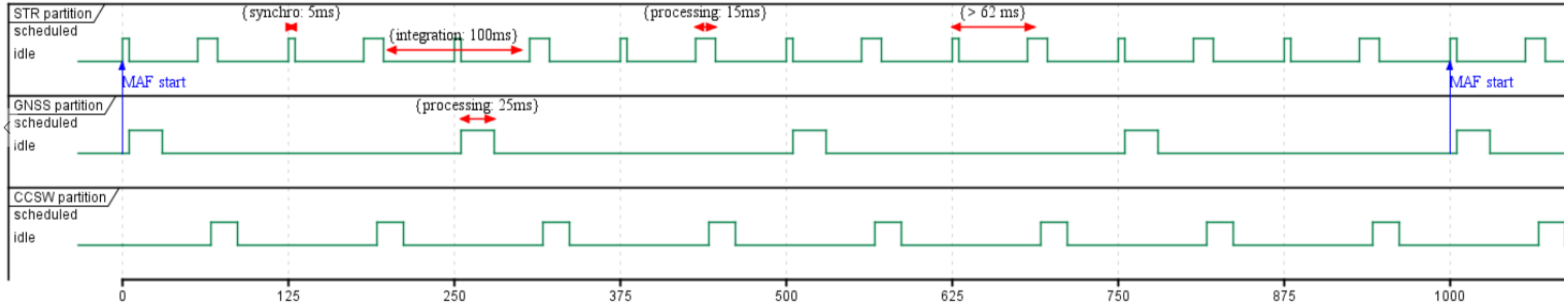
- Estimations of CPU load is:





- Time Partitionning (main contributors)

DARWIN Scheduling



DARWIN – CURRENT STATE

- Tested
  - Standalone IPs
  - Generic TMTC format using generic Database
  - Test end-to-end from TC sending until TM receiving through actuation
  - SST partition with SST in tracking mode
- Currently validating AOCS SW
- Yet to be tested
  - Closed AOCS loop
  - Test of HYPERION

AGENDA

CONCLUSION

YET TO BE DONE:

- Complete demonstration on closed loop AOCS (end of November)

TO GO FURTHER…

- TMTC encryption
- Demonstration with HYPERION and BOMO
- « FLATSAT »

CONCLUSION

CONSIDERATIONS:

- IP Integration from various companies
- IP protection
- Responsability following integration (Validation, Anomalies)
- Strategic components procurement to aim « low-cost » products
- Lowering « space quality » expectations for the new-space market?

THANK YOU FOR YOUR ATTENTION

Contact information :
Pierre.spizzi@cnes.fr

DARWIN - AROUND OBC CENTRALIZATION

OBMU(100% redundnant)

Gyro

TMTC

demodulator,digitizer

amplification, antenna

SST (Hydra)

Processing unit

Optical Head

GNSS

Processing unit

antenna

OBC (TMTC + GNSS + SST processing)

BTCU (Thermal acquisition unit + gyro)

TMTC (amplification, antenna)

SST (Optical Head)

GNSS (antenna)

GOAL:

High reliability Version

⇒ ~35kg
⇒ ~70W

⇒ ~25kg
⇒ ~40W

Medium/low reliability version

⇒ ~15kg
⇒ ~30W

DARWIN SoC ARCHITECTURE

- Zynq-7000 devices
  - ARM Cortex-A9 processors integrated
  - 28nm based programmable logic