Open Instruction Set Architectures (ISA) in Space

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Why Using an Open ISA in space?

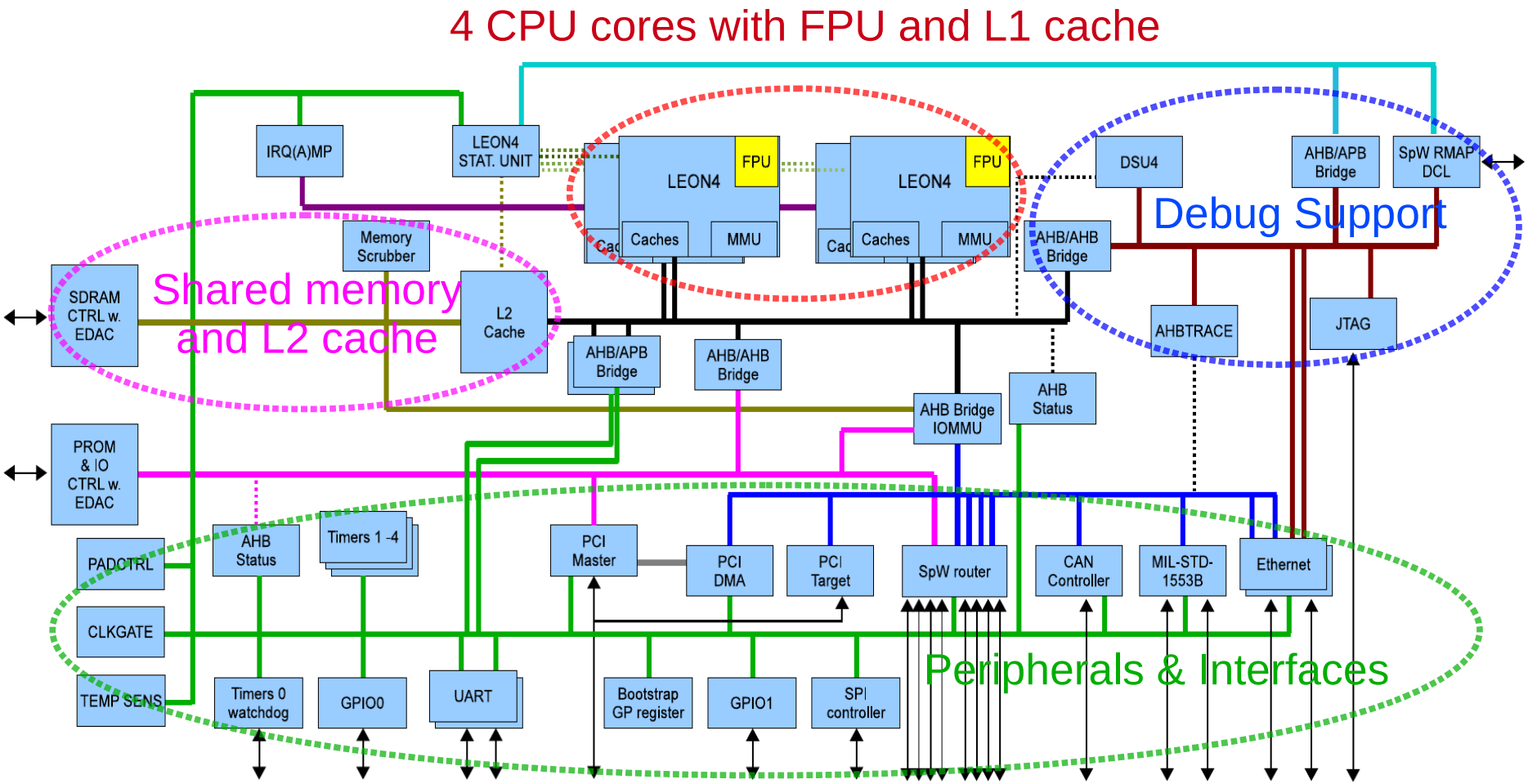
- What is an ISA?
  - **I**nstruction **S**et (and) **A**rchitecture: abstract model of a computer – **not an IP**
  - Open ISA = non proprietary, free to use for everybody
  - Note: **“Open ISA” ≠ “open source IP core”**
- Free of licence fees / royalties
  - But probably higher cost for development and verification of IP
  - Still saves a lot of hassle for licence negotiation
- No export restrictions (most likely...)
- Can be modified
  - In space: low-level modifications for radiation mitigation (pipeline restart...)
  - For unmodifiable COTS-IP or -chip: core- or chip-level redundancy, lockstep
  - Instructions can be modified or added
  - ASIP = Application-Specific Instruction-set Processor
- Examples: OpenRISC, SPARC, RISC-V, MIPS (open as of 2019!)

Choice of SPARC for Space – a Success Model!

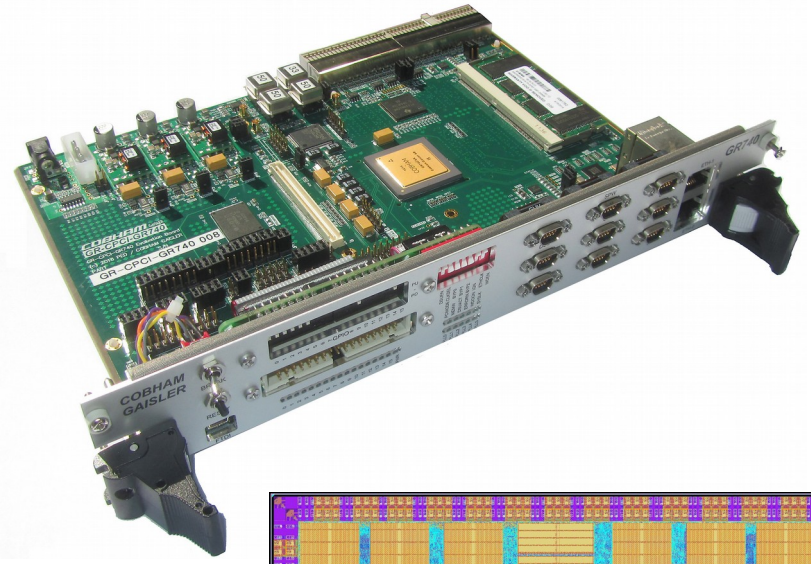
- Keynote Jiri Gaisler, ADCSS 2017 https://indico.esa.int/event/182/timetable
- Why did ESA choose SPARC (25 years ago...)?
  - → Free and open Standard, allowing for customised implementations
  - → Industry and academia backing: commercial products (Sun, Fujitsu)
  - → Stable specification, low complexity, GNU tool chain
- Market penetration – estimated sales > 10000 (FM / PFM):
  - → Microchip (Temic/Atmel): ERC32 (TSC691/2/3/5): 5000
  - → Microchip LEON2 based: AT697, AT7913, AT7991: 1500
  - → Cobham Gaisler (UT699/700, GR712RC, RTAX): 2000
  - → Leon ASICs (SCOC3, MDPA, COLE, DST, TTE): ????
  - → LEON IP (Gaisler, LGPL, ESA) on many space FPGA: ????

- SPARC is on all recent ESA satellites and on Vega and Ariane 5 and 6
  - → Commercial telecom satellites (SCOC3, AGGA4)
  - → It has flown to the back side of the moon (AT697, Chang'E4)
- Is SPARC/LEON becoming obsolete? – No, it is still used and maintained
  - → Still LEON IP users (LEON2 in 65 nm for Ariane-6 TTEthernet)
  - → Compilers up to date: GCC 7.2.0 (2017, Aug → December)
  - → LLVM CLANG 4.0.0 (2018)
  - → RTEMS-SMP 5.1 (2017), qualification in progress

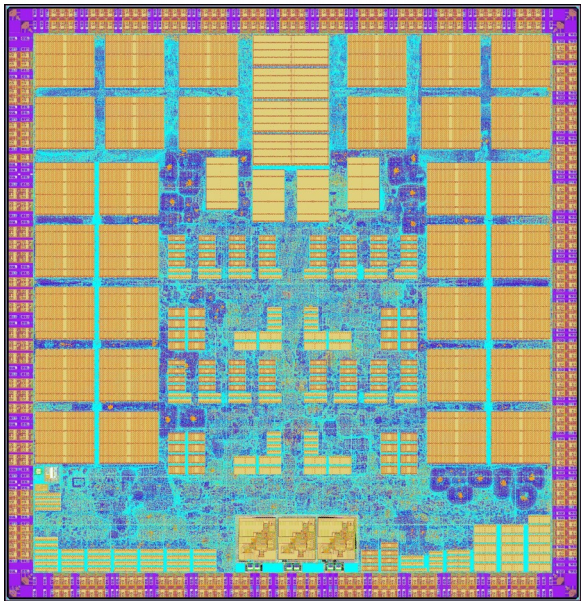
GR740 – Quad-Core, 65 nm, 250 MHz

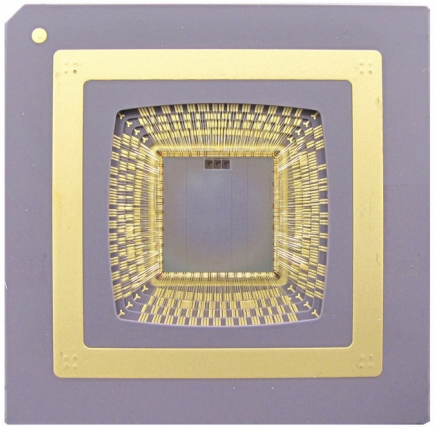


GR740 Development Status

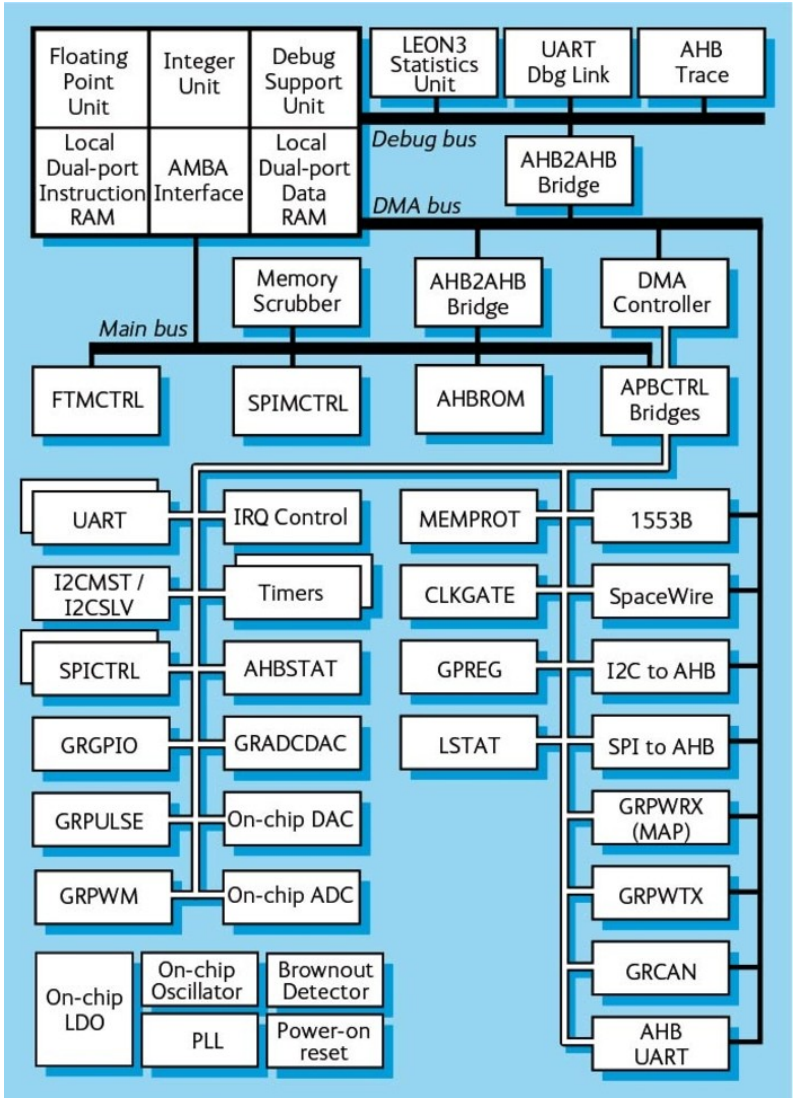


- → Prototypes and evaluation boards (2016)
- → Design updates and fixes (2017)
- → Flight silicon manufactured (Q1/2018)
- → Functional and Radiation Validation (2018)
- → Flight assembly (OPM, new package design)
- → Qualification in progress, Q3/2020
- → **GR740 User Day: 28. November 2019, ESTEC**

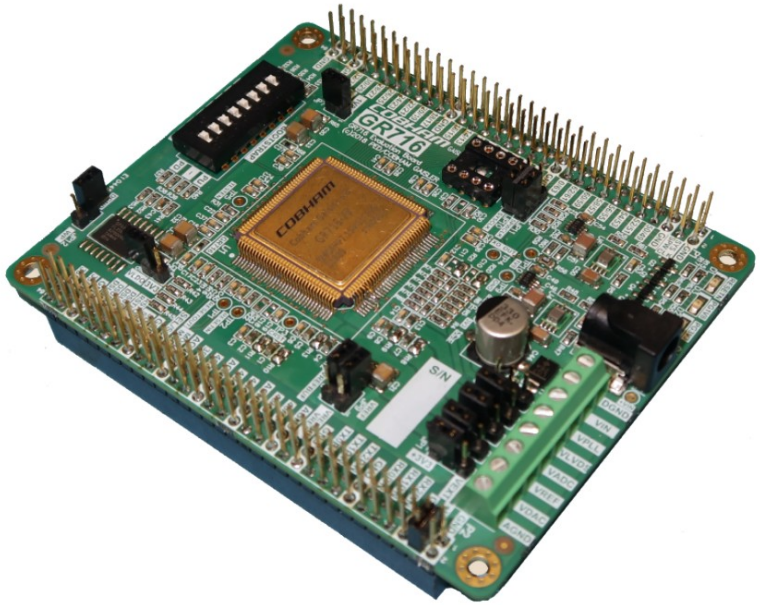




GR716 Status

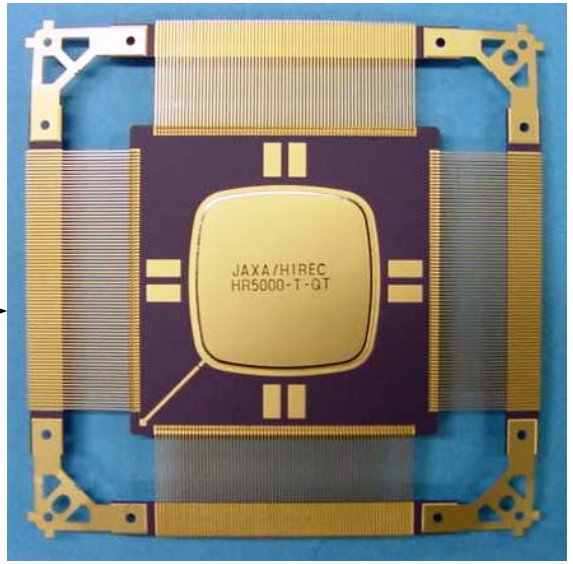


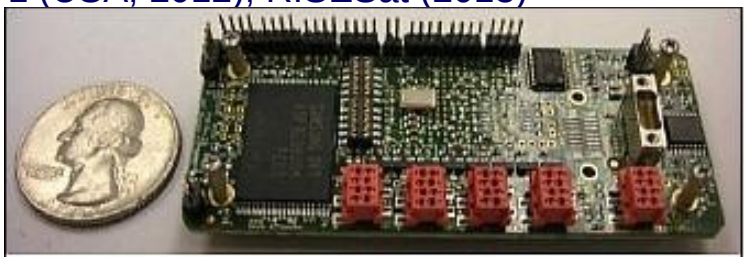
- GR716 Status
  - → Development completed
  - → Prototypes and board available
  - → Radiation testing done (report pending)
- Industrialisation planned (funding?)
  - → Revision GR716B with new features
  - → Qualification in Ceramic QFP132
  - → Package variants (MCM with NVM?)



History: RISC-1, MIPS, DLX, OpenRISC

- RISC-1: Berkeley, David Patterson / Carlo Sequin (1980 - 1984)
  - → Register Windows, Commercialised as SPARC by Sun
- MIPS: Stanford, John Hennessy (1981 - 1985)
  - → Microprocessor without Interlocked Pipeline Stages, single cycle
  - → Used as proprietary IP until 2019 (owners: Imagination, Wave)
  - → Used by JAXA for space microprocessors
- DLX ("Deluxe"): Hennessy / Patterson (1990's)
  - → Modernised MIPS, for teaching only
  - → Data forwarding, instruction reordering
- OpenRISC: Started 1999 (Rev 1.3 6/2019), https://openrisc.io/
  - → OR1200 (LGPL) https://github.com/openrisc/or1200, 2000 -2015
  - → MOR1K (OHDL) https://github.com/openrisc/mor1kx, active 2019
  - → Commercially used e.g. by Flextronic in Samsung TV's
  - → Space usage: OBClite, ÅAC Microtec (Ångström / Clyde Space)
  - → Flown on TechEdSat-1 (USA, 2012), RISESat (2013)
- RISC-V: Berkeley (2010)
  - → https://riscv.org/
  - → Rev. 2.2 (6/2019)
  - → BSD licence
  - → No reg windows
  - → Flexible extensions





ÅAC OBCLite

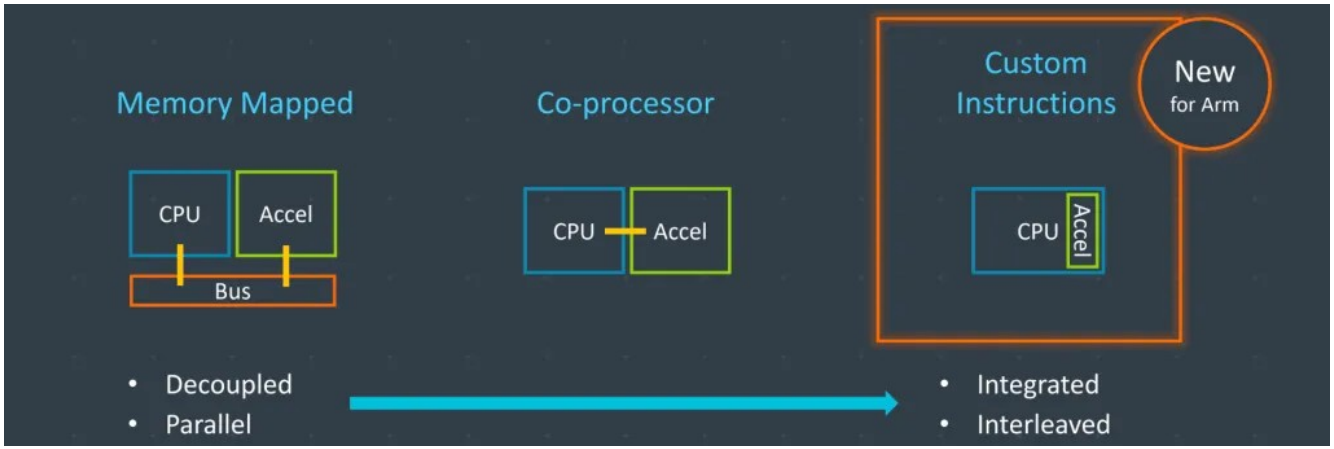
TechEdSat-1

Name	Description	Status
Base		
RV32I	Base Integer Instruction Set, 32-bit	Frozen
RV32E	Base Integer Instruction Set (embedded), 32-bit, 16 registers	Open
RV64I	Base Integer Instruction Set, 64-bit	Frozen
RV128I	Base Integer Instruction Set, 128-bit	Open
Extensions		
M	Standard Extension for Integer Multiplication and Division	Frozen
A	Standard Extension for Atomic Instructions	Frozen
F	Standard Extension for Single-Precision Floating-Point	Frozen
D	Standard Extension for Double-Precision Floating-Point	Frozen
G	Shorthand for the base and above extensions	N/A
Q	Standard Extension for Quad-Precision Floating-Point	Frozen
L	Standard Extension for Decimal Floating-Point	Open
C	Standard Extension for Compressed Instructions	Frozen
B	Standard Extension for Bit Manipulation	Open
J	Standard Extension for Dynamically Translated Languages	Open
T	Standard Extension for Transactional Memory	Open
P	Standard Extension for Packed-SIMD Instructions	Open
V	Standard Extension for Vector Operations	Open
N	Standard Extension for User-Level Interrupts	Open
H	Standard Extension for Hypervisor	Open

- General Purpose Processor
  - → RV32IMAFD = RV32G (= SPARCV8?)
  - → 32 int + 32 float registers (no windows!)
  - → Load-Store (reg2reg arithmetics only)
  - → SPARC-like 20+12 lui (sethi) mechanism
  - → No branch delay slot, little endian
- Numerous extensions (draft!)
  - → C – Compressed (= Thumb, Leon-REX?)
  - → B – Bit Manipulation (requested by user)
  - → Hypervisor / SIMD / Vector
- IPs and chip implementations (examples)
  - → Opensource IP (Rocket, BOOM, PULPino…)
  - → Commercial IP (Syntacore, Andes…)
  - → SiFive (IP + 4+1-core 1.5 GHz, 28 nm)
  - → Greenwaves (8+1 core 250 MHz, 55 nm)
  - → Alibaba XuanTie (2.5GHz 16-core, 12 nm)
  - → NVIDIA replacing Falcon controller by RISCV

Competitor's Answer in 2019

- ARM is opening for custom instructions
  → The IP and ISA are still proprietary, custom instructions in a "container"
  https://www.arm.com/why-arm/technologies/custom-instructions
  https://staceyoniot.com/why-arm-opened-up-its-instruction-set-and-what-it-means-for-iot/



- MIPS going open source after sale to Wave
  https://www.mips.com/mipsopen/

- IBM OpenPower (2013), PowerISA open-sourced in 2019
  https://openpowerfoundation.org/the-next-step-in-the-openpower-foundation-journey/

→ A success story for RISC-V ...

This session

- Leveraging the Openness and Modularity of RISC-V in Space
  - NPI Research cooperation
  - Speaker: Mr Stefano Di Mascio (TU Delft)
- Introduction of Fault-Tolerant Concepts for RISC-V in Space (ESA TRP/ITI contract)
  - ESA ITI R&D contract, evaluation, TMR and fault injection of (LowRisc) RISC-V IP
  - Speaker: Mr Jan Andersson (Gaisler), Luis Aranda (Aries)
- The RISC-V Klessydra Orbital Lab project
  - PULPino implementation for space
  - Speaker: Mr Luigi Blasi (university of Rome)
- New arithmetic extensions for LEON2-FT (ESA GSTP contract)
  - FPU, and SIMD / Vector operations, will be available as ESA IP-core
  - Speaker: Mr Daněk Martin (DAITEQ)

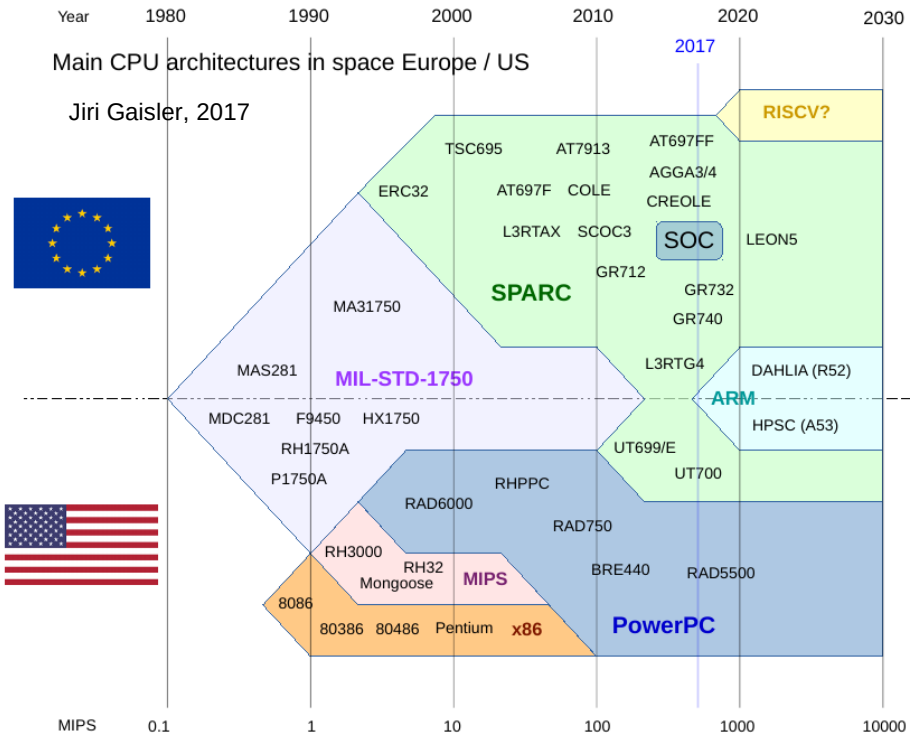
Conclusion

The SPARC open ISA: 25 years in space, ~10000 Flight Models

- → Synergy with academia and commercial use of SPARC – in the past
- → **SPARC is not dead**: GR740 and GR716 new ESA supported processors
- → Huge effort on SW ecosystem done (compilers, OS, hypervisor)
- → SPARC will be our work-horse for many years to come

Several other open and proprietary RISC ISA's have been used in space

- → None of them has been as successful in space as SPARC



What NEXT???

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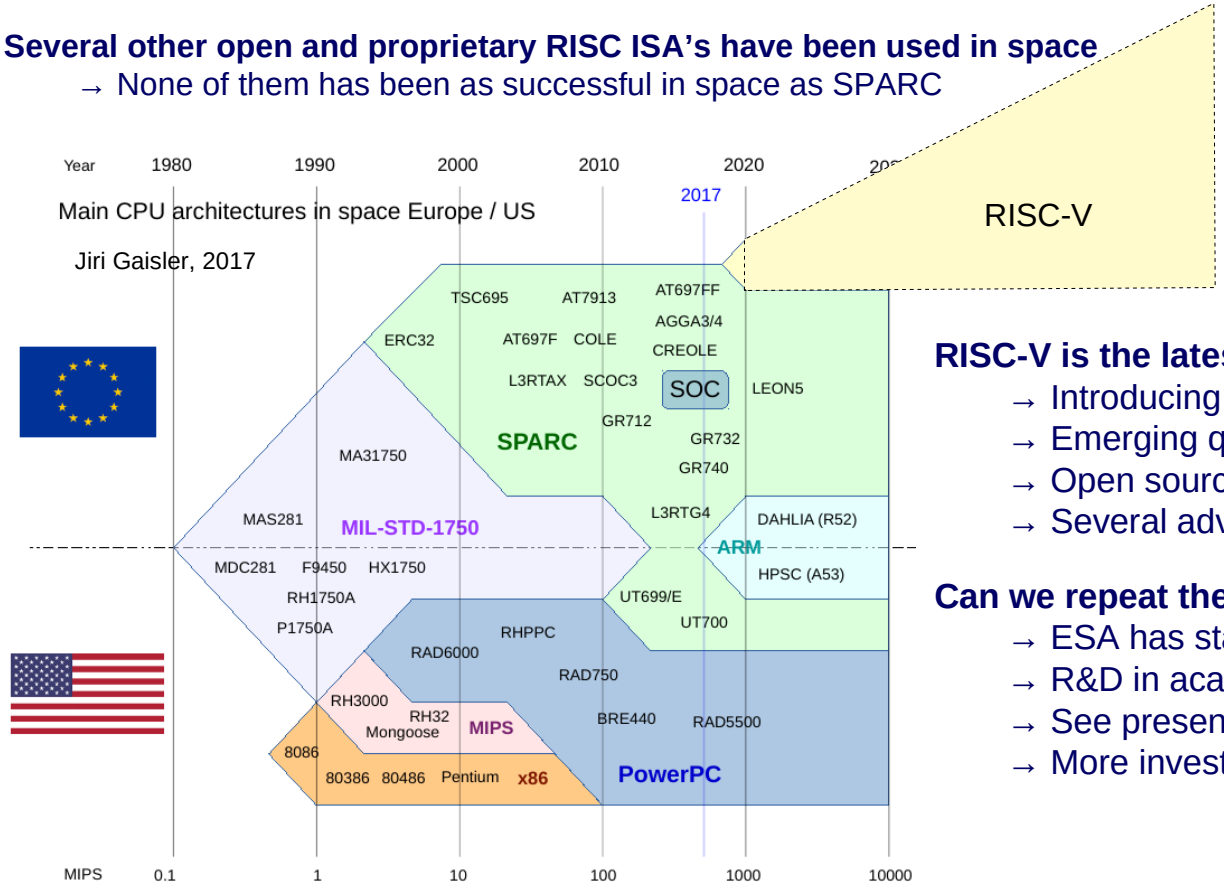

RISC-V is the latest branch of the Berkeley RISC tree

- → Introducing flexibility to the instruction set
- → Emerging quickly in academia and commercially
- → Open source and commercial IPs available
- → Several advanced commercial chips

Can we repeat the success of "SPARC in space"?

- → ESA has started RISC-V R&D at a small scale
- → R&D in academia, EU H2020 activity
- → See presentations of today
- → More investment is needed (industry, lobbying)