LEON5 Processor Core

Release in December 2019

COBHAM

Primary goals:

- SPARC V8 32-bit compliant processor core
- Improved performance over LEON4
- **Superscalar – dual issue**
- Goal is to have modes with deterministic, or bounded timing performance
- Reduction of configuration options
- **Hardware support for virtualization**
- SEU tolerance
- **Leverage existing software** support, maintain binary compatibility with LEON3 and LEON4

Primary feature set:

- **SPARC V8e**
- AHB and AXI4 bus support
- HW support for virtualization
- Local RAM (TCM)
- Copy-back cache (subject to performance evaluation in combination with multi-ported memory controllers with striped ports)
- Little endian support

Target technologies:

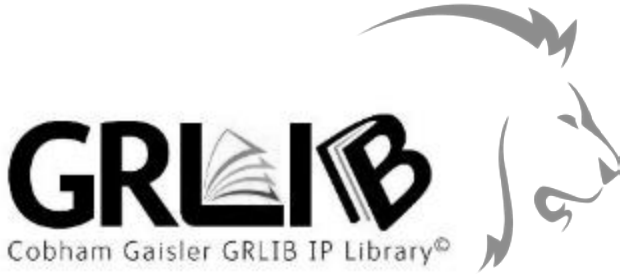
- ASIC implementations for space applications
- High-end space FPGAs: Kintex Ultrascale

Target applications:

- General purpose payload processing
- Mixed platform and payload applications

Complemented by:

- New DDR2 and DDR3 SDRAM controller (FTADDR23), specifically targeted for space applications
- Multi-port L2 cache extensions allowing bandwidth extensions from L1 to off-chip memory devices



RISC-V Processor Core

Release in December 2019

COBHAM

Primary goals:

- RISC-V 64-bit compliant processor core
- **Superscalar – dual issue**
- Fault Tolerance - Error Correction Codes (ECC)
- **Cybersecurity** (proprietary solutions)
- Enabled for RTCA/**DO-254** (Design Assurance Guidance for Airborne Electronic Hardware)
- Enable ISO 26262/**FUSA** certification (Road vehicles – Functional safety)
- **Leverage** foreseen uptake of **RISC-V software** and tool support in the commercial domain
- **Compatible with GRLIB IP Core library**

Primary feature set:

- **RISC-V RV64GC**
- AHB and AXI4 bus support

Supportive activities

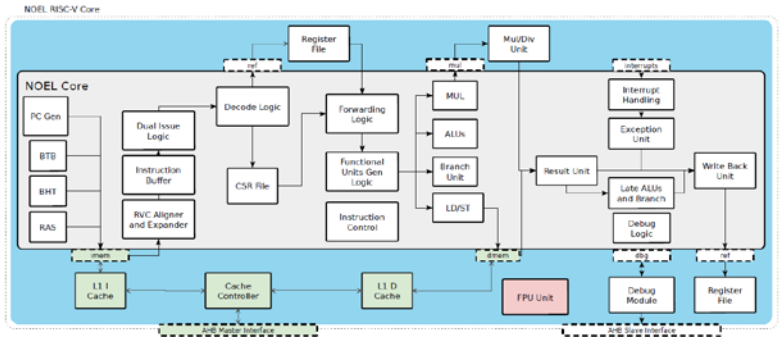
- RISC-V Foundation Membership in 2019
- RISC-V PhD position at University of Delft with ESA

Target technologies:

- ASIC implementations for space applications
- High-end space FPGAs: Kintex Ultrascale

Target applications:

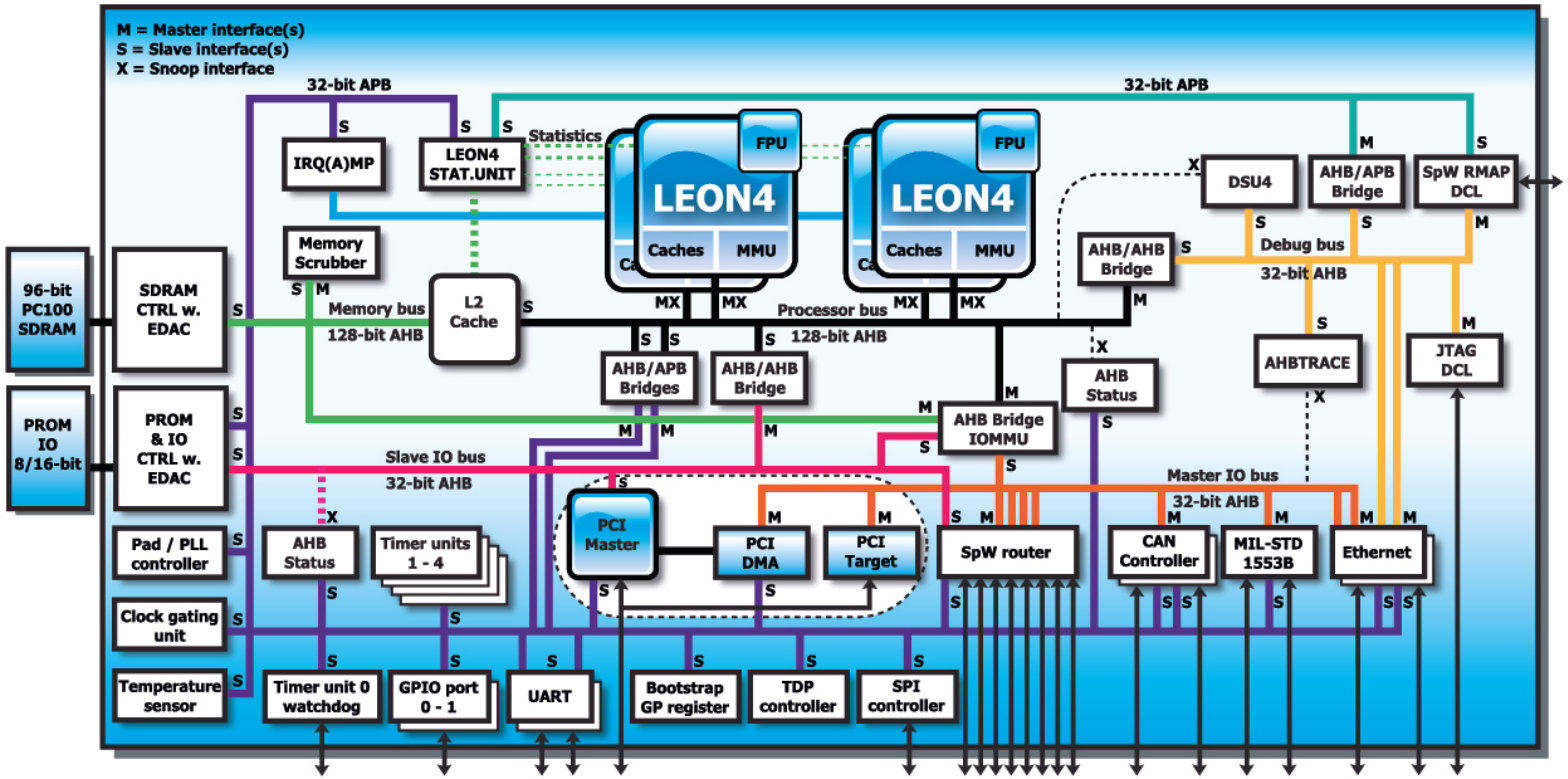
- General purpose payload processing
- Mixed platform and payload applications
- With future DDR4 SDRAM controller, specifically targeted for space applications



GR740 - Quad-Core LEON4FT - architecture

GR740 – designed for multi-processing

- Quad-core LEON4FT with dedicated FPU and MMU
- 32KiB L1 caches per core connected to 128-bit AHB
- 2 MiB L2 cache, 256-bit cache line, 4-ways
- 64-bit PC100 SDRAM memory I/F (+32 checkbits)
- 8-port SpaceWire router with 4 internal ports
- 32-bit 33 MHz PCI interface
- 2x 10/100/1000 Mbit Ethernet
- Debug links: Ethernet, JTAG, SpaceWire
- MIL-STD-1553B, CAN 2.0B, 2 x UART, SPI master/slave, GPIO, Timers & Watchdog



SPARC Compliant
SCD V8

QML Qualification ongoing

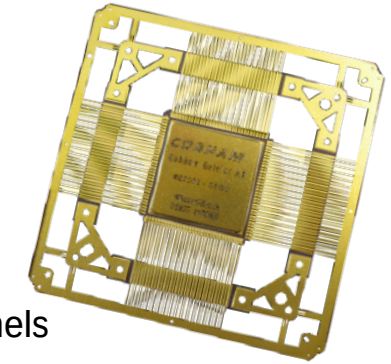
Expected completion 2H2020

GR740 User Day 28 November 2019, ESTEC

GR716 Single-Core LEON3FT Microcontroller

European Microcontroller development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



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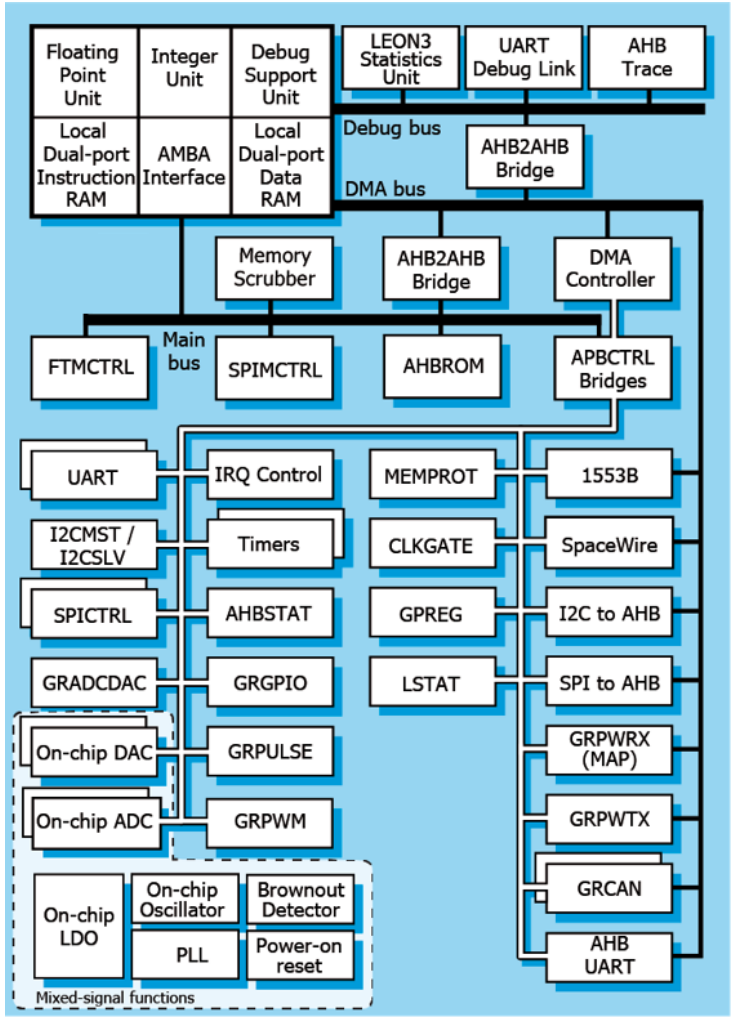
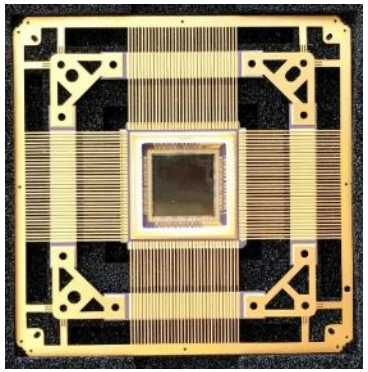


GR716 updated schedule

As of 1st November 2019

GR716	Status	Milestone	Comments
Prototype level functional test	*done*	*Q4 2018*	*completed in December*
Prototype level performance test	*done*	*Q2 2019*	*Completed in April*
Prototype level part delivery	*done*	*Q2 2019*	*Completed in April*
Evaluation board delivery	*done*	*Q2 2019*	*Completed in April*
Datasheet and User's manual released on website	*done*	*Q2 2019*	*Completed in May*
Prototype Radiation test	*done*	*Q3 2019*	*Completed in September*
Prototype with improved analogue performance	*done*	*Q3 2019*	*Available for order*
Qualification lot production		Q4 2019	Ongoing
Flight qualification complete GR716		Q4 2020	

- Qualification according to ESCC9000 by end of 2020.



GR716 Single-Core LEON3FT Microcontroller

European Microcontroller development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
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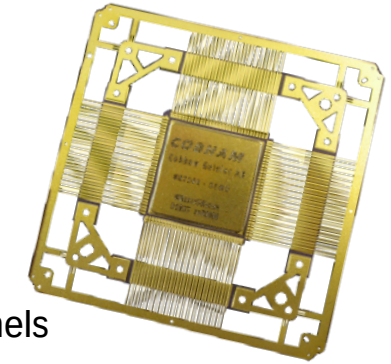

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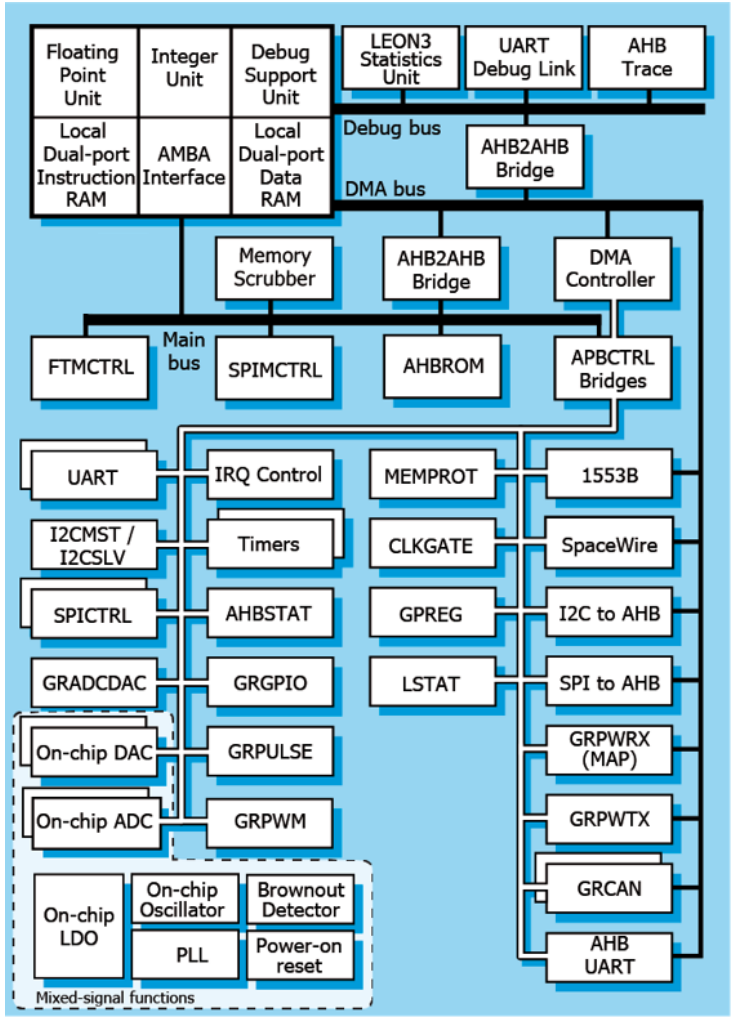
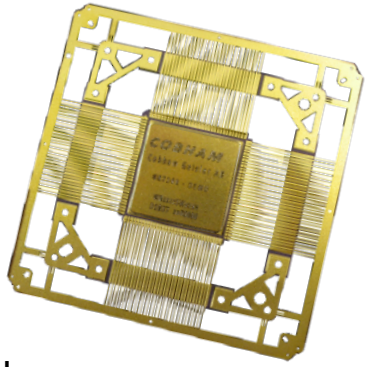


GR716B Single-Core LEON3FT Microcontroller

European Microcontroller development - Enhanced version development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- **Hardware FPGA programming and scrubber: Xilinx Virtex5, UltraScale, ...**
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



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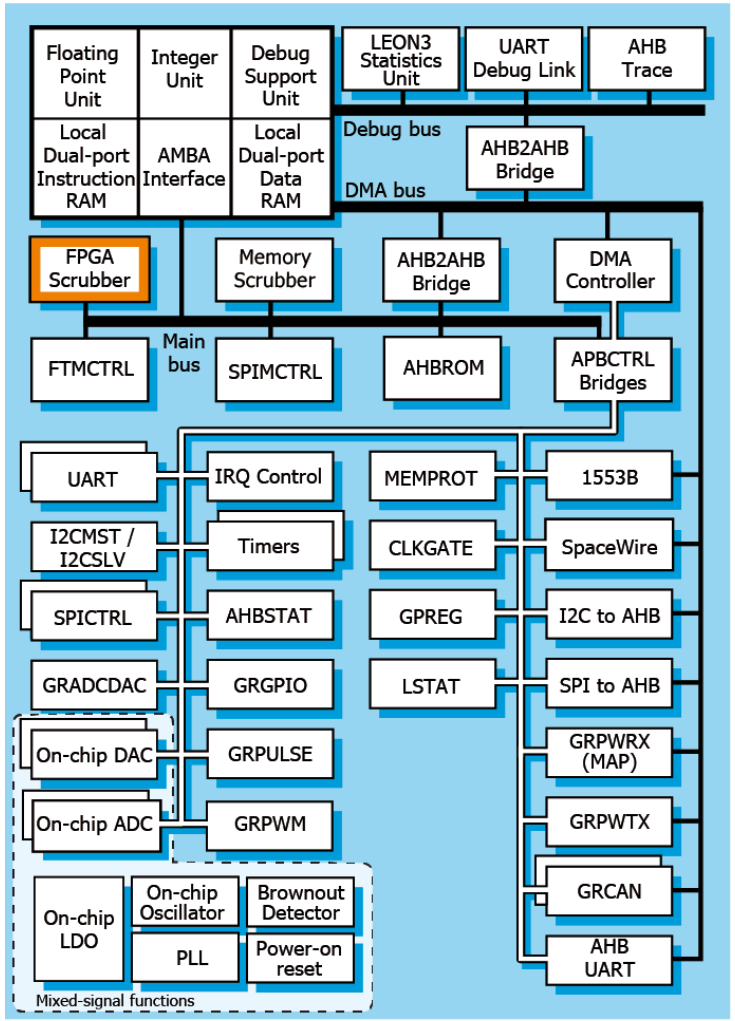

GR716B Single-Core LEON3FT Microcontroller

European Microcontroller development - Enhanced version development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, **100** MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- **Hardware FPGA programming and scrubber: Xilinx Virtex5, UltraScale, ...**
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
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- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended channels
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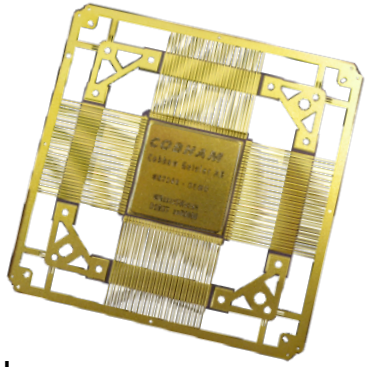
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



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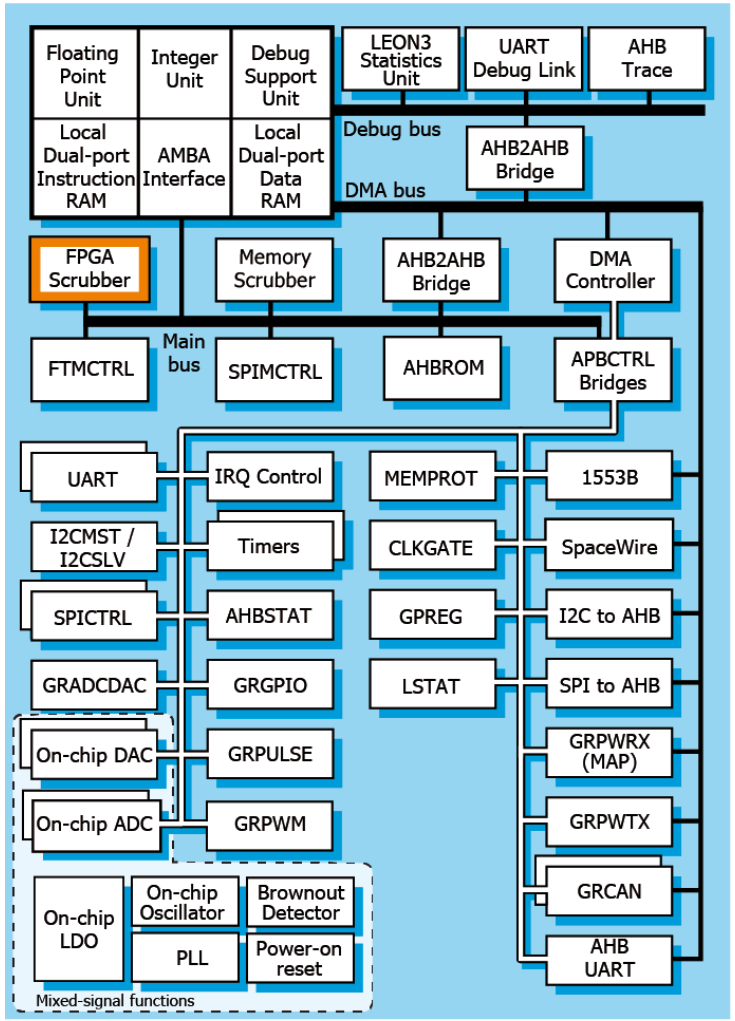
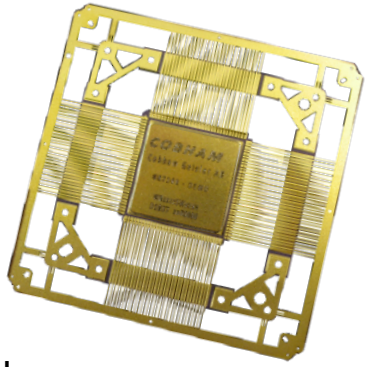


GR716B Single-Core LEON3FT Microcontroller

European Microcontroller development - Enhanced version development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, **100** MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- **Hardware FPGA programming and scrubber: Xilinx Virtex5, UltraScale, ...**
- **2-Port SpaceWire Router** with **Cold Spare LVDS** and time distribution support, **200** Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



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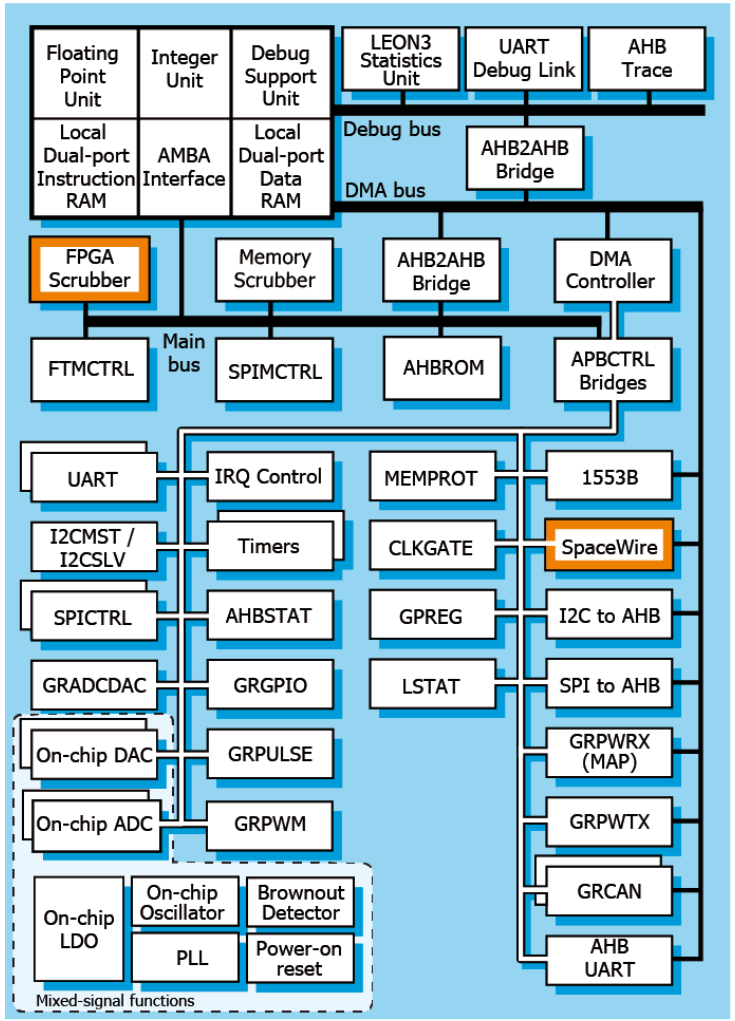
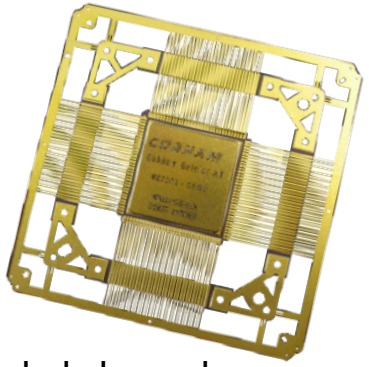
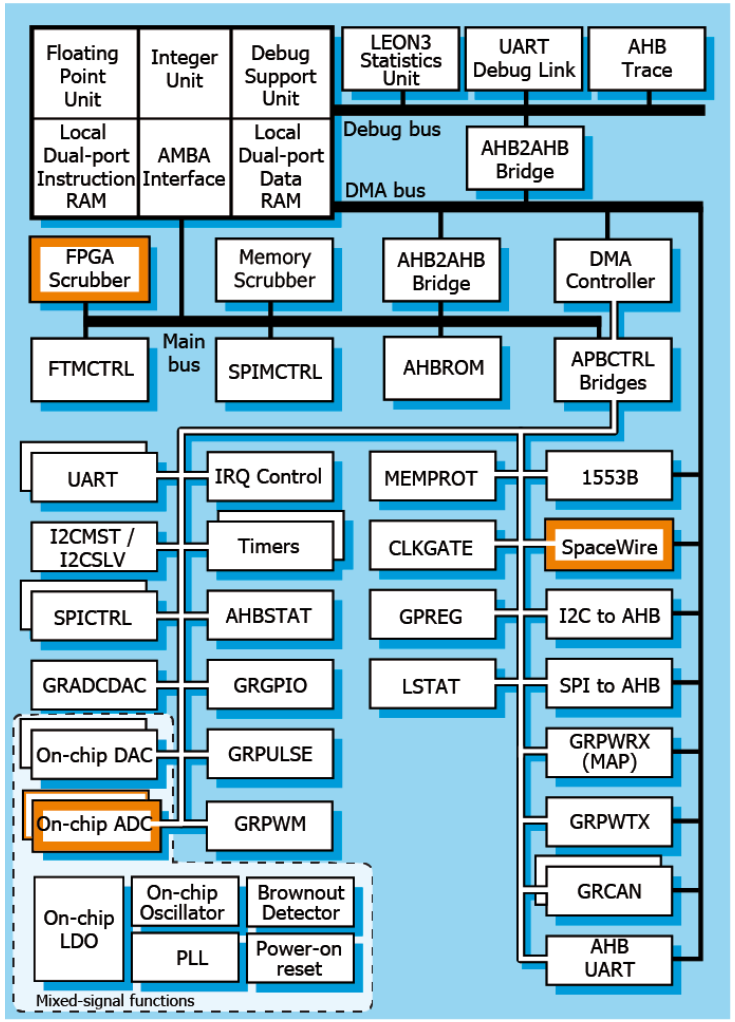


GR716B Single-Core LEON3FT Microcontroller

European Microcontroller development - Enhanced version development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, **100** MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- **Hardware FPGA programming and scrubber: Xilinx Virtex5, UltraScale, ...**
- **2-Port SpaceWire Router** with **Cold Spare LVDS** and time distribution support, **200** Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- **3x ADC 13bits resolution** @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm

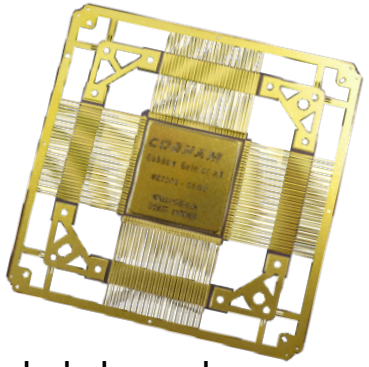


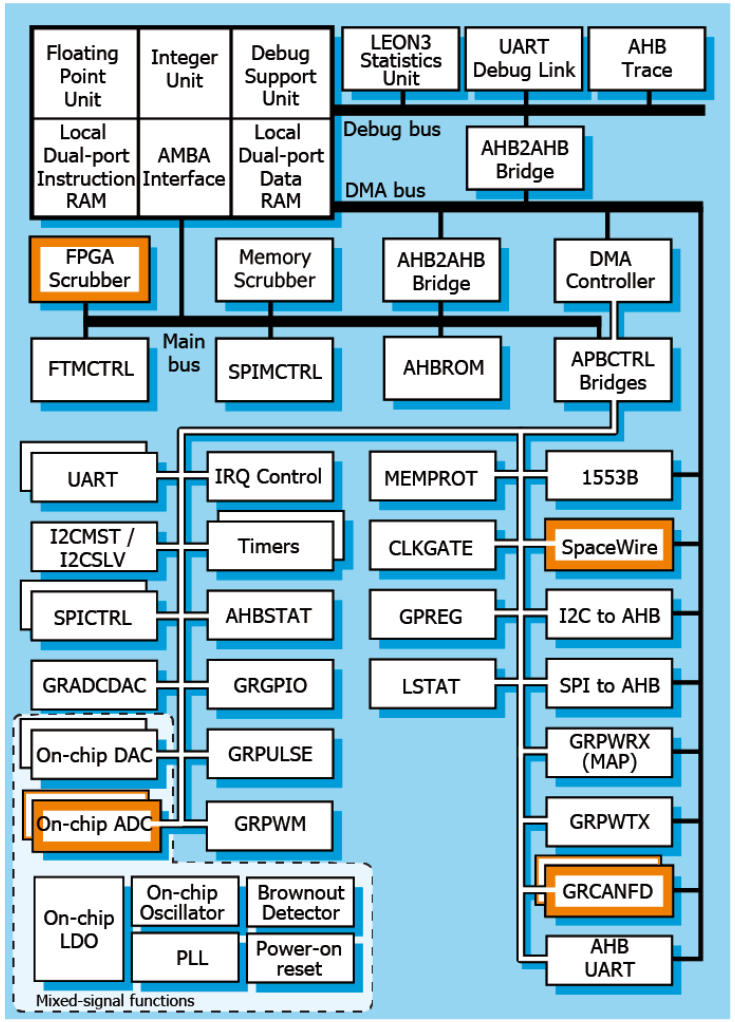


GR716B Single-Core LEON3FT Microcontroller

European Microcontroller development - Enhanced version development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, **100** MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- **Hardware FPGA programming and scrubber: Xilinx Virtex5, UltraScale, ...**
- **2-Port SpaceWire Router** with **Cold Spare LVDS** and time distribution support, **200** Mbps
- MIL-STD-1553B interface
- **2x CAN-FD** controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- **3x ADC 13bits resolution** @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm

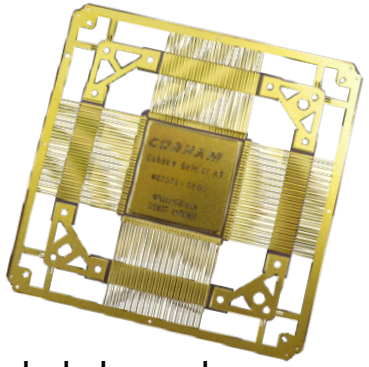




GR716B Single-Core LEON3FT Microcontroller

European Microcontroller development - Enhanced version development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, **100** MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- **Hardware FPGA programming and scrubber: Xilinx Virtex5, UltraScale, ...**
- **2-Port SpaceWire Router** with **Cold Spare LVDS** and time distribution support, **200** Mbps
- MIL-STD-1553B interface
- **2x CAN-FD** controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- **10/100 Ethernet**, UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- **3x ADC 13bits resolution** @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



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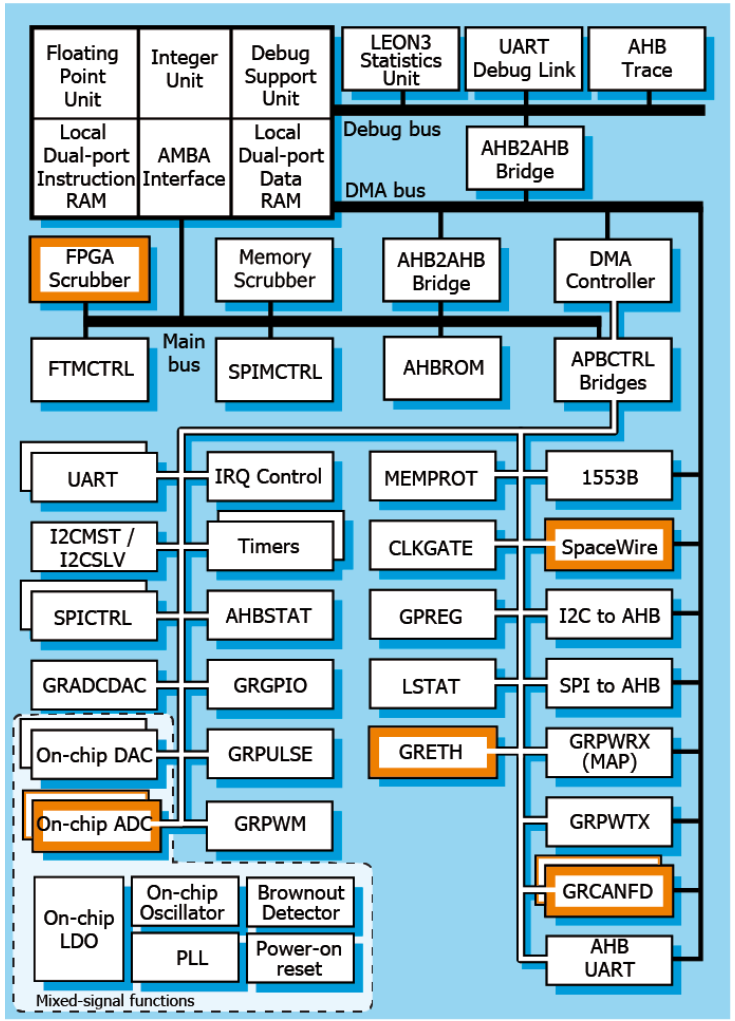
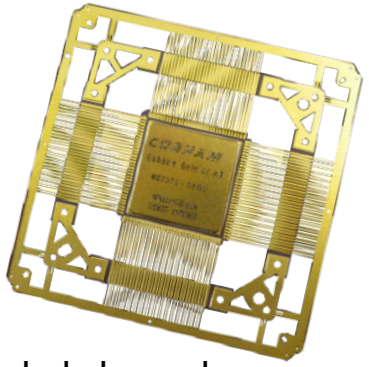


GR716B Single-Core LEON3FT Microcontroller

European Microcontroller development - Enhanced version development

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, **100** MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - **Pipelined** Floating Point Unit
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture...
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- **Hardware FPGA programming and scrubber: Xilinx Virtex5, UltraScale, ...**
- **2-Port SpaceWire Router** with **Cold Spare LVDS** and time distribution support, **200** Mbps
- MIL-STD-1553B interface
- **2x CAN-FD** controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- **10/100 Ethernet**, UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- **3x ADC 13bits resolution** @ 200Ksps, 4 differential or 8 single ended channels
- DAC 12bits @ 3Msps, 4 channels
- Mixed General-purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



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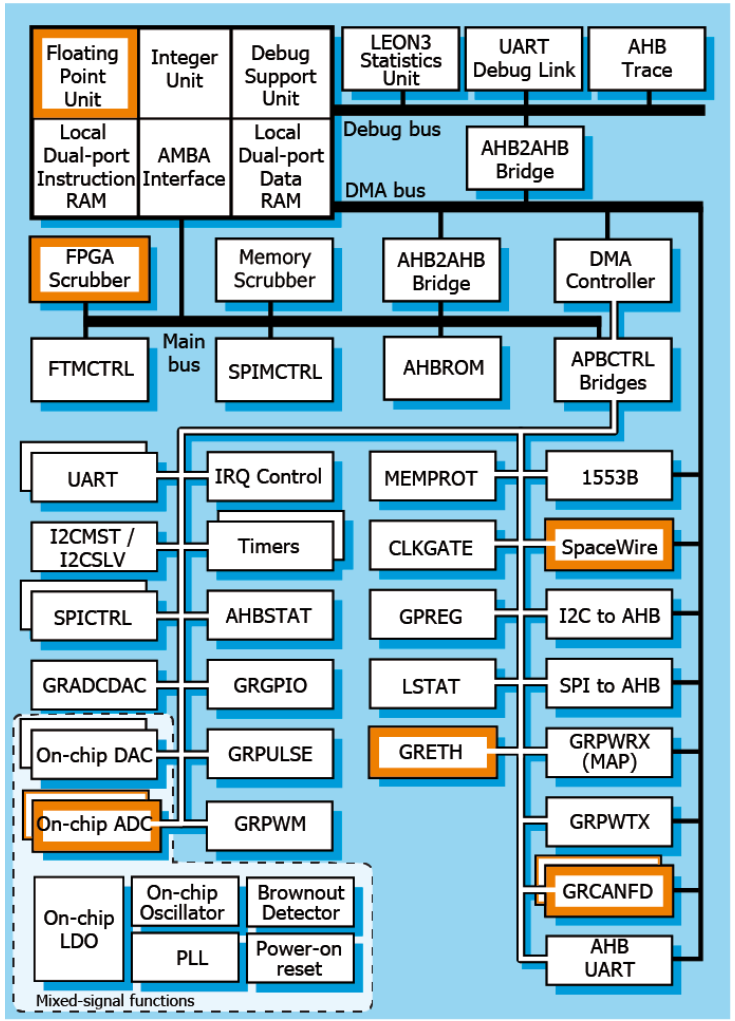
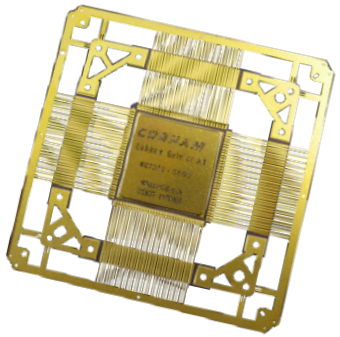
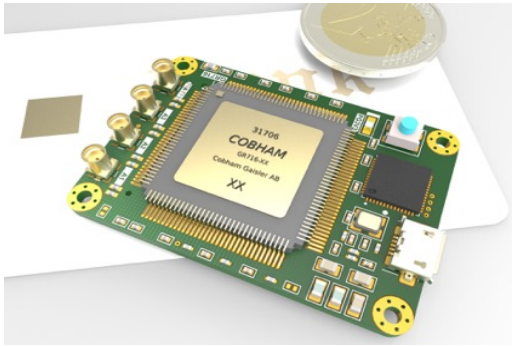
SPARC



GR716B updated schedule

- As of 1st November 2019





GR716B	Status	Milestone	Comments
Scrubber interoperability testing with Xilinx Ultrascale FPGAs	*On track*	Q4 2019	*FPGA prototyping ongoing*
Tape-out of improved LVDS test chip with Cold Spare support	*On track*	Q1 2020	
Early GR716B prototype samples	*On track*	Q3 2020	*Tape-out in June 2020*
Electrically qualified GR716B models tested in full temperature range		Q4 2020	
Evaluation board delivery		Q4 2020	*Reuse of existing evaluation boards*
Datasheet and User's manual release on website		Q4 2020	*Draft version available upon request from Q1 2020*
Flight qualification complete		TBC	

- *Flight model scheulde or qualifaction process has not yet been decided*