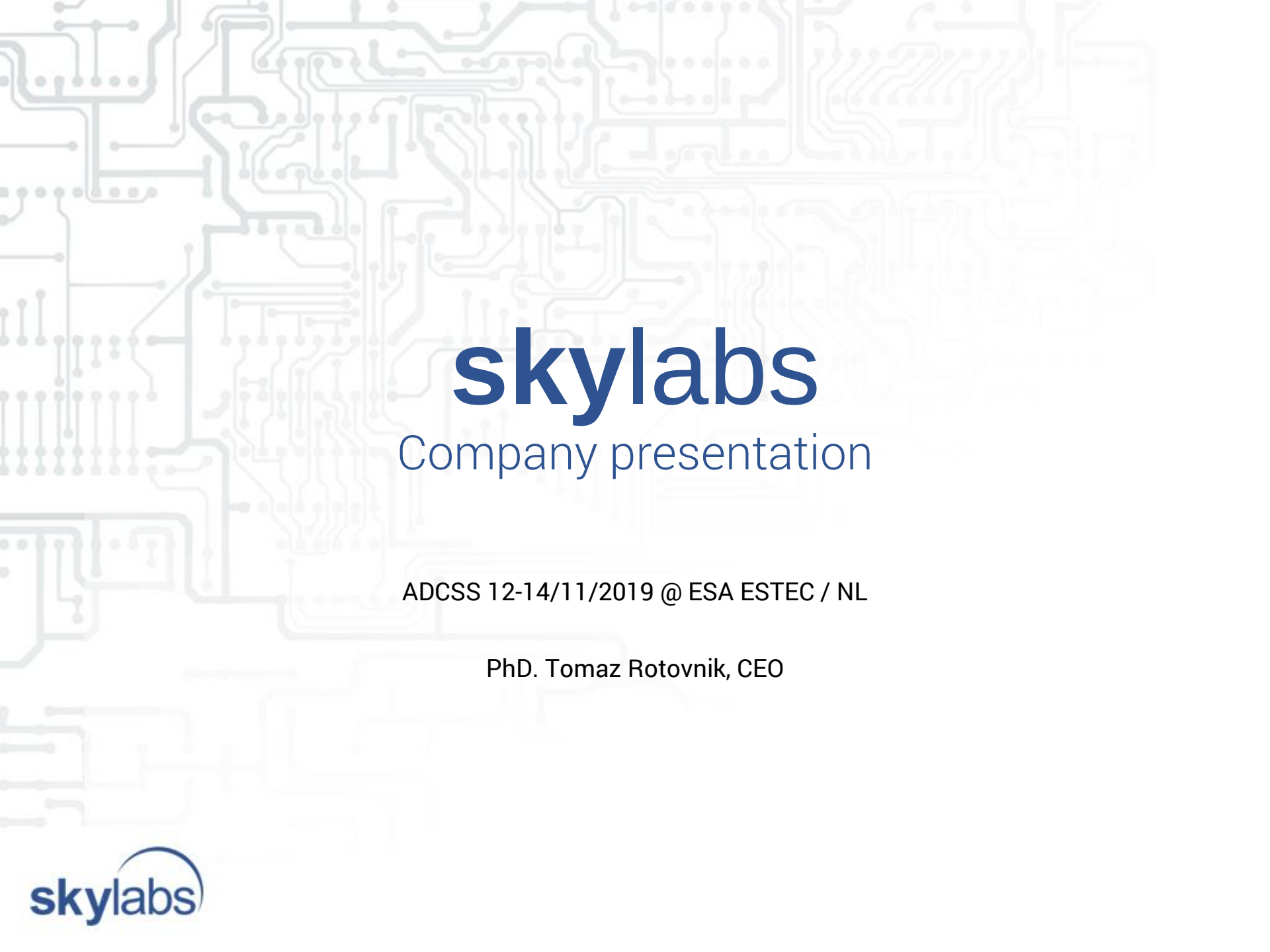


The background of the slide is a light gray, intricate circuit board pattern with various lines, dots, and geometric shapes, resembling a complex electronic design.

skylabs

Company presentation

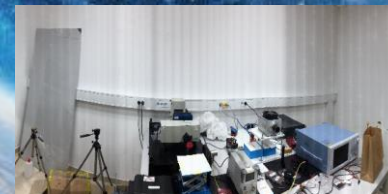
ADCSS 12-14/11/2019 @ ESA ESTEC / NL

PhD. Tomaz Rotovnik, CEO



SkyLabs at glance

- **Highly skilled electronics and software R&D engineering team**
 - Team of 17 experts
 - Embedded electronics and software development
 - Analog electronics, radio systems, and signal processing
 - Mechatronics development
 - IP Cores (digital and mixed signals)
- **Engineering development approach**
 - Miniaturization key aspect (following latest technology trends)
 - Hardware accelerated approach
 - Awareness of harsh space environment effect
- **SkyLabs closely cooperates with University of Maribor – Laboratory for Electronic and Information Systems**
 - Knowledge and technology transfer
 - Recruiting of highly skilled professionals
 - Core research capabilities (12 researchers)
 - TRISAT mission: First satellite developed with Slovenian know-how



SkyLabs Vision

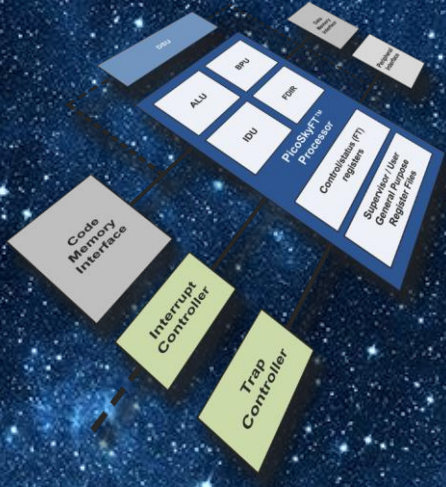
We are innovating the aerospace market with SkyLabs disruptive technologies, products and solutions to change the layout of space.



- **Quality and products assurance**
 - ISO 9001:2015 pending certificate
 - Regular ECSS trainings (inheriting into internal development and QA processes)

PicoSkyFT soft-core processor

Small footprint, radiation hardened by design processor core



Radiation testing

- Microsemi ProASIC3 test vehicle
- No unsafe SEFIs
- Internal resets CS-p: $9,46E-12 \text{ cm}^2$ (due to detected errors)
 - Protons at PSI
 - UHE at CERN
 - Neutrons at ChiplR



- **Small footprint, soft-core and fault tolerant** processor core.
- **ESA activity** (verification and radiation characterisation of the core), Tecnology identified in **THAG Dossier**
- IP Core building block for true SoC architecture implementation and **technology independent**
- **Architecture**
 - RISC 8/16-bit Harvard architecture
 - Highly deterministic operation
 - Hard real time interrupt response capabilities
 - Low memory footprint of the application code
- **Radiation hardened by design approach (SEE tolerant)**
 - Fully distinguished dual operational mode (supervisor and user mode)
 - Spatial triplication (TMR) on register level (optional temporal redundancy)
 - EDAC protected memory blocks, by Hamming scheme
- FDIR policy for mitigation techniques

Satellite platform **NANOsky I**

Complete solution out of the box

Highly miniaturized & reliable nanoscale platform with FT features



The right solution for
the emerging space market



Fault tolerant
system design



New type
of harness



Pushing the limits of
system miniaturization

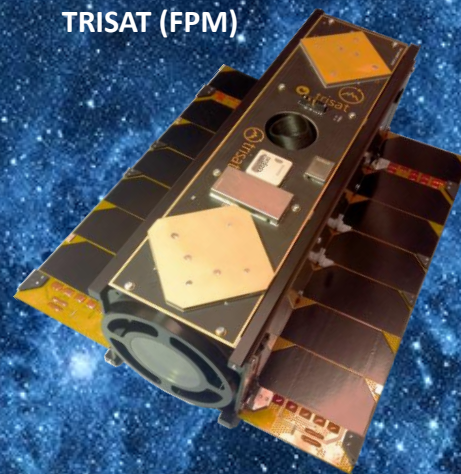


Designed for high
reliability and availability

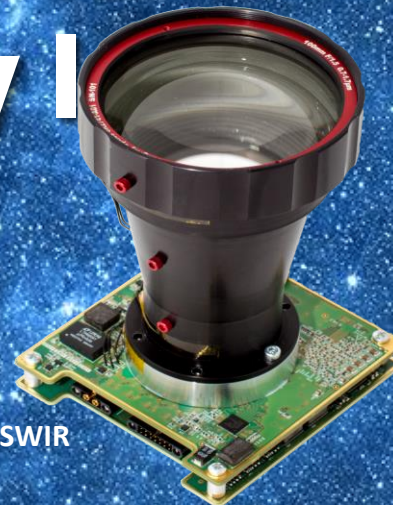


Tailor made to
clients needs

TRISAT (FPM)



NANOimager
Miniaturized
multispectral SWIR
imager



NANOobc
On-board
computer



NANOlink
S-Band SDR
transceiver



NANOcomm
UHF/VHF
transceiver



NANOeps
Electrical
Power System



SEE immunity, innovative error mitigation techniques, sophisticated three-level FDIR policy, redundancy on all critical functions and thoughtful component selection ensure robustness, high reliability and availability of the platform

picoRTU system

- Distributed RTU system
 - Enabled by PicoSkyFT technology
 - Four modular units fulfils any mission needs.
 - SWaP optimized
 - ECSS compliant user interfaces
 - Analog: TSM, ASM, diff. ASM, SS
 - Digital: BSM
 - High power: HPC
 - Comm: CAN, RS422, UART
- Targeting small satellite missions
 - 4 modules design
- PCB design technology
 - High Density Interconnect
 - PCB stack-up: ML10
 - Board size: 95x95 mm
- Enclosure design
 - Compatibility with PCB verified with 3D models
 - SLS prototyping
 - 9-axis CNC milling



picoRTU EM



picoRTU modular structure

Thank you

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