SEFUW: SpacE FPGA Users Workshop, 5th Edition

Tuesday 17 March 2020

Design Flow - Newton 1 and 2 (11:40 - 13:00)

time	[id] title	presenter
11:40	[3] Getting Started with OSVVM, VHDL's #1 Verification Methodology	LEWIS, Jim
12:10	[6] Using Static RTL Analysis to Accelerate Space FPGA Verification	Mr ADAM TAYLOR, adam
12:35	[22] A UML Profile for VHDL FPGA Designs.	Mr OTTACHER, Harald

Wednesday 18 March 2020

Design Flow - Newton 1 and 2 (11:50 - 13:00)

time	[id] title	presenter
11:50	[42] FPGA continuous integration	MANNI, Florent
12:10	[19] UVVM usage is exploding. A brief introduction and all the new stuff for this standardised VHDL verification methodology.	Mr TALLAKSEN, Espen
12:40	[31] Accelerating the Journey from C/C++ to Hardware	Mr SARAIS, Pantelis