

CoRA-SAGE: The lessons learnt from AOCS/GNC algorithms deployment in TASTE

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Abstract

Compact Reconfigurable Avionics (CoRA) is a co-engineering activity involving AOCS&GNC, software engineering and on-board data handling whose aim is to prototype an in-flight reconfigurable avionics system. In this context, SAGE (CoRA-SAGE) is a multidisciplinary activity aimed to implement AOCS&GNC functional chains with a large suite of space sensors and actuators in parallel with the Model Based Avionics Design (MBAD) activity and the Reconfigurable Data Handling Core (RDHC) activity. CoRA-SAGE has been responsible of developing the AOCS/GNC exercised in the reconfigurable avionics and the ground support equipment, including simulated units and a piece of flight hardware used to test the overall CoRA system.

CoRA-SAGE selected Space Rider reusable servicing vehicle as strawman test configuration. Space Rider is a unique ESA mission with several application scenarios including Earth Observation, telecommunication, science and demonstration missions. Space Rider orbital and re-entry phases requirements allows to stress the need to fit very different AOCS/GNC modes in the on board computer. From the full set of the Space Rider mission, SENER has included in CoRA-SAGE the Fine Pointing Mode (FPM), Safe Mode (SM) and Re-Entry Mode (REM), which are representative of the AOCS/GNC modes present in any space mission. CoRA-SAGE EGSE provides the electrical interfaces to the AOCS components, combined with the simulation of the spacecraft environment and behaviour in order to verify the functionality of the AOCS/GNC and the stimulation of the hardware unit selected, an AURIGA star tracker which is operative in one of the orbital modes. CoRA-SAGE EGSE provides a mixture of simulation and sensor stimulation capabilities, including:

- Simulation of AOCS components for flight software verification and to support incremental integration, i.e., simulation of absent components
- Simulation of spacecraft environment and dynamics for open and closed loop testing of AOCS algorithms
- Characteristics that cannot be provided by the real devices, such as simulation of erroneous behaviour due to device failure or degradation
- Integrated external developed models as part of the simulation environment
- Real sensors (e.g. star tracker, etc.) so that they can generate representative data for the test scenarios used for AOCS verification
- Interfaces of the spacecraft on-board buses
- Interfaces of stimulated AOCS components (sun acquisition sensor, gnss, imu, flush air data system, reaction wheels, reaction control system)
- Optical ground support equipment of the star tracker HW unit

The architecture of the CoRA-SAGE system is depicted in Figure 1.

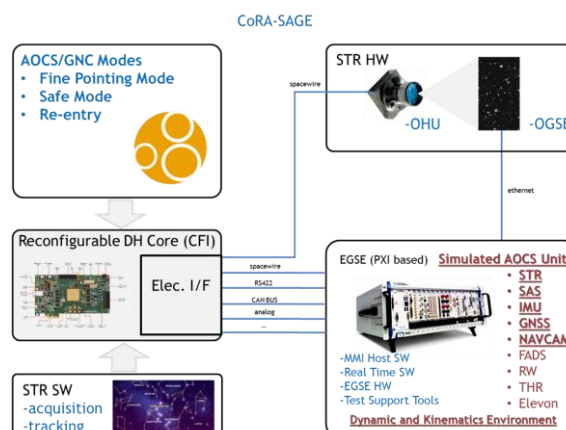


Figure 1: CoRA-SAGE Architecture

The design of the selected AOCS/GNC modes is modular and allows to reconfigure the AOCS/GNC functions partitioning between hardware and software implementations, hence allowing the implementation of the same algorithm both in FPGA or in the processor and following a Model Based approach. The design and performance assessment were conducted in Matlab/Simulink while the verification and deployment have been done via TASTE. The use of these tools, and specially TASTE, have facilitated the interaction with the other CoRA teams to specify and implement the AOCS/GNC software/hardware in the Data Handling Core. From CoRA-SAGE point view, TASTE served to capture the AOCS/GNC modes architecture in the same environment in which the algorithms were finally deployed with the rest of the CoRA system and to centralize the interfaces of the AOCS/GNC modes and sub-functions. Within the CoRA-SAGE team, TASTE allowed the creation of a constantly updated and exchangeable database for the variable names, variable length and data type easing the communications between of the AOCS/GNC and software teams. Moreover, this approach has been paramount to verify the AOCS/GNC deployment.

CoRA-SAGE team decided to verify the AOCS/GNC modes incrementally. First, in the Functional Engineering Simulator (FES), the transformation of the algorithms to use fixed-point representation was done. Secondly, Open Loop tests were designed and executed directly in TASTE (with an internally available emulated GR740 processor), prior to the Closed Loop tests conducted with the CoRA-SAGE EGSE and the COTS-Bread Board (preliminary BB procured by RDHC to test CoRA-SAGE before having available all CoRA elements) and the whole CoRA system acceptance tests. The open loop tests verification in TASTE paved the way to deploy successfully the AOCS/GNC modes both on the COTS-BB and on the Elegant-BB (definitive BB designed for CoRA). Indeed, no flaw due to the AOCS/GNC modes functioning was detected during the overall system verification conducted after the verification of AOCS/GNC modes through open loop tests via TASTE. The TASTE features for early verification and testing of the generated software (GUIs and Python scripts) were employed to verify the deployment. The objective was not testing again the full functionality, previously verified in a dedicated Matlab/Simulink Functional Engineering Simulator, but a subset of representative cases selected in order to validate the successful migration of the algorithms to the target platform.

AOCS/GNC modes code were generated automatically from Simulink, uploaded in TASTE and run in an open loop simulated environment with the inputs generated in the FES. For this, the inputs/outputs definitions automatically generated by TASTE were loaded in Simulink, according to the interface database defined within TASTE. Finally, the GUI application available in TASTE allowed iterating with the algorithms via Python external scripts feeding the AOCS/GNC modes with input reference data and verifying the integration. A sketch of the verification process is shown in figure 2.

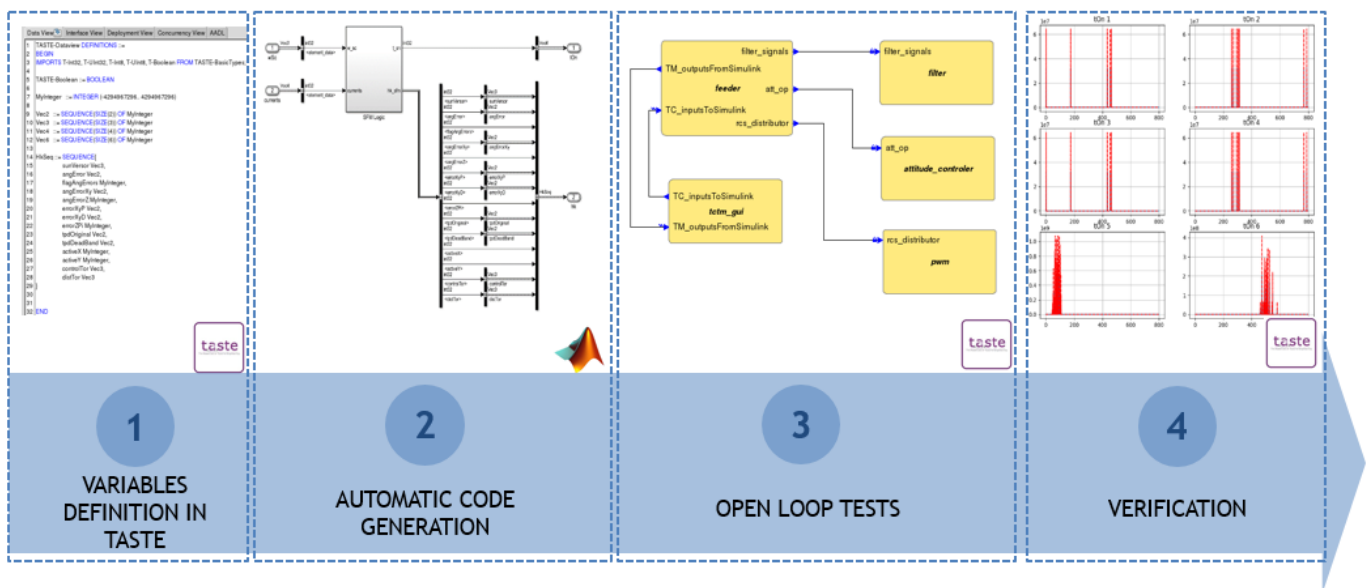


Figure 2: Verification process of CoRA-SAGE AOCS/GNC implementation

This process facilitated to achieve the consistency between AOCS/GNC algorithms and implemented software, the generation of code and the partitioning of the AOCS/GNC into elementary functions to fit the FPGA capacities. Moreover, it served to verify the AOCS/GNC algorithms deployment in the early phases of the project.